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A New Low Turn-Off Loss SOI Lateral Insulated Gate Bipolar Transistor With Buried Variation of Lateral Doping Layer

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ABSTRACT In this paper, we propose a new low turn-off loss silicon-on-insulator (SOI) lateral insulated gate bipolar transistor (LIGBT) with buried variation of lateral doping (VLD) layer. The proposed device features a VLD layer inserted in the drift region, which increases the doping dose (Q) and gradient (G) compared with Uniform P-buried (UPB) SOI LIGBT. The larger capacitance effect induced by lager Q and faster depletion leads to the lower rising anode voltage and reduced storage charge in the drift region. Therefore, a considerable low turn-off loss (E_{off}) can be obtained. It is worth to note that owing to reshaped electric field in the new structure, the excess carriers of the drift region could be removed more quickly. Furthermore, larger G of the VLD layer improves the tradeoff between breakdown voltage and turn-off loss. The results of 2-D simulation indicate that the E_{off} of the proposed device can reduce by 29.4% and 69.7% at 100 A·cm^{-2} and 200 A·cm^{-2}, respectively, when compared with UPB SOI LIGBT.

INDEX TERMS Variation of lateral doping (VLD), lateral insulated gate bipolar transistor (LIGBT), linear doping, turn-off loss, silicon-on-insulator (SOI).

I. INTRODUCTION

Lateral insulated gate bipolar transistor (LIGBT) is mainly used for the integration of power devices with control circuitry. Silicon-on-insulator (SOI) LIGBTs act as an important component in power integrate circuits due to its property of superior isolation, low leakage current and high current capacity [1]–[9]. However, the switching of the LIGBT device is associated with the removal of the stored charges in the N-base region and thus causing a high switching loss. Many efforts are widely made to reduce turn-off loss especially under inductive loading through N-type extraction path, such as SSA LIGBT, STA LIGBT, MSA LIGBT [10]–[12]. However, they suffer from large cell size, complex etching and quadruple diffusion, respectively, while inducing snapback effect and increasing forward conductive voltage in the on-state. Another effective solution is adoption of the new drift structure. For example, [13] introduces a uniform P-buried layer (UPB) in the drift region of SOI LIGBT. In the paper, the structure with buried variation of lateral doping (VLD) layer is firstly introduced into the SOI LIGBT, and its influence on accelerating turn-off process will be investigated in detail.

In this paper, we propose SOI LIGBT with buried VLD layer which sustains high breakdown voltage (BV) and a lower turn-off loss (E_{off}) without enlarging device size when compared with UPB LIGBT. As shown in Fig. 1,

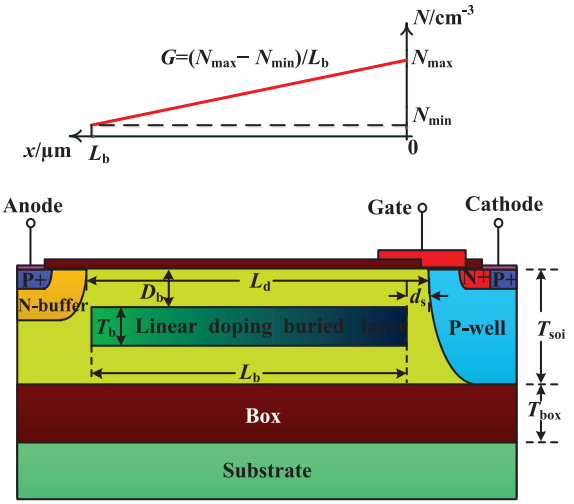

FIGURE 1. 2-D Schematic cross-sectional view of the SOI LIGBT with buried VLD layer.

a VLD layer is introduced by being implanted into the drift region. This VLD layer enables a slower anode voltage increase and fewer stored charges in the drift region. Moreover, the VLD layer enhances the extraction ability of excess carriers in the drift region so that a lower turn-off loss can be achieved. The validity of the proposed device is verified through detailed simulation results.

II. DEVICE STRUCTURE AND MECHANISM

Fig. 1 illustrates the 2-D cross-section of the SOI LIGBT with buried VLD layer. Compared with the UPB LIGBT, the P-buried layer in the proposed structure has a linear doping profile. As shown in Fig. 1, the doping profile of the buried P-type layer is determined by a linear function $N_b(x)$. The $N_b(x)$ reaches its maximum (N_{max}) and minimum (N_{min}) at the boundary close to P-well and N-buffer, respectively. Hence, the doping concentration gradient $G = (N_{max} - N_{min})/L_b$ and the doping profile $N_b(x) = N_{max} - Gx$. Since the resistance of the drift region (R_{dri}) is determined by N_d, the VLD layer has little influence on R_{dri}. Consequently, V_{on} is almost independent of the VLD layer and the influence is not discussed in the paper.

In order to demonstrate the turn-off mechanism of the proposed LIGBT, a set of optimized parameters for device is applied to Sentaurus TCAD. The key parameters are shown in Table 1. Both the proposed device and UPB LIGBT own the same parameters except Q and G. N_d, Q and G have been optimized based on triple RESURF principle [14]. Q is higher in the proposed device, because VLD layer could optimize the surface electric field [15]. As shown in Fig. 2, the inductive turn-off of the proposed device is divided into four different phases, which are represented by phase I, phase II, phase III and phase IV, respectively. Anode voltage rising stage is divided into three phases according to different slopes: phase I, phase II and phase III. Anode current falling stage is defined as phase IV, which starts when the anode

TABLE 1. Key parameters for device.

Parameters	Proposed device	UPB LIGBT
SOI layer thickness, T_{soi}	6μm	6μm
buried oxide thickness, T_{box}	3μm	3μm
N-drift length, L_d	30μm	30μm
N-drift doping concentration, N_d	1×10^{16}cm^{-3}	1×10^{16}cm^{-3}
buried VLD layer dose, Q	3.6×10^{12}cm^{-2}	2.6×10^{12}cm^{-2}
buried VLD layer doping concentration gradient, G	2.4×10^{14}cm^{-3}μm^{-1}	0
buried VLD layer length, L_b	29μm	29μm
distance between buried VLD layer and P-well, d_s	0.6μm	0.6μm
buried VLD layer thickness, T_b	2.0μm	2.0μm
distance between buried VLD layer and top of N-drift, D_b	1.8μm	1.8μm

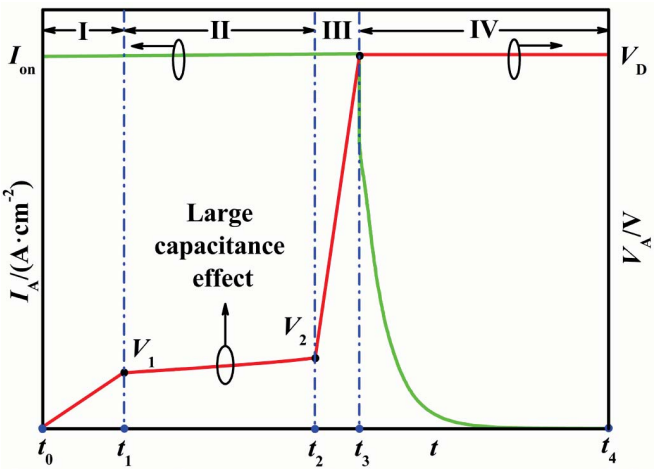

FIGURE 2. Turn-off waveforms of the proposed device.

voltage reach power supply voltage. In phase I ($t_0 \le t \le t_1$), with the increase of the anode voltage (V_A), the drift region depletion boundary expands until it contacts the right boundary of the VLD layer (AB in Fig. 3(a)), and at this moment (t_1), V_A equals to V_1. Smaller V_A and short time result in smaller phase I loss (E^I_{off}).Therefore, E^I_{off} is negligible. The unique turn-off characteristics of the proposed device are phase II and phase IV, which are largely different from UPB LIGBT. In order to qualitatively and quantitatively demonstrate the turn-off loss suppression effect of the buried VLD layer, the detailed analysis of the turn-off process would focus on phase II and phase IV in following sections.

In phase II ($t_1 \le t \le t_2$), as illustrated in Fig. 3, with the increase of V_A, the drift region depletion boundary expands from the side of AB along the outline of VLD layer to the side of A′B′. When the depletion boundary touches the side of A′B′, V_A equals to V_2. Thus, in phase II, V_A can be given by:

$$V_A = V_1 + I_{on} \cdot R \tag{1}$$

where R is the effective resistance of the drift region, V_1 is the anode voltage at the end of the phase I, and I_{on} is the

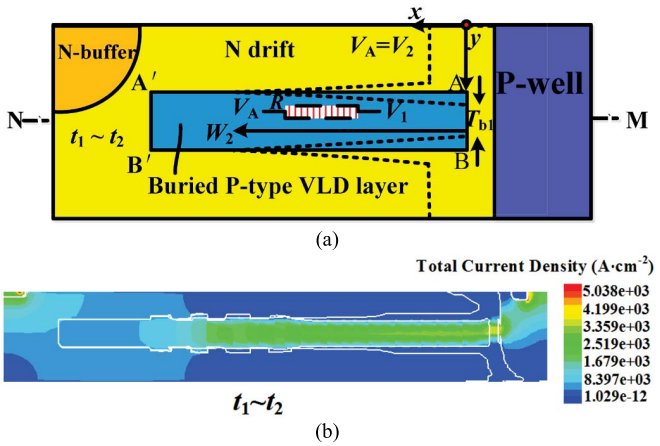

FIGURE 3. **(a) Depletion region expanding in phase II (b) Corresponding current density in phase II.**

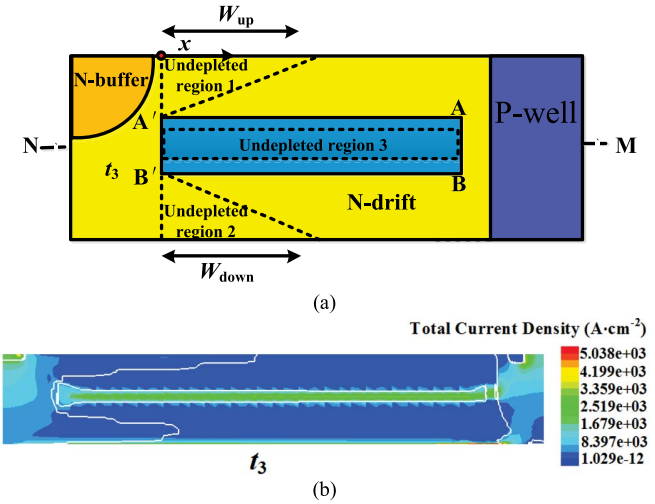

FIGURE 4. **(a) Depletion region at t_3 (b) Corresponding current density at t_3 The depletion region edges are assumed to be symmetrical with respect to the line NM for simplicity in (a).**

on-state current. $R(W_2)$ is given by:

$$R(W_2) = \int_0^{W_2} \frac{1}{q\mu_p Z} \frac{dx}{N_b(x)\left[(T_b - T_{b1})x/W_2 + T_{b1}\right]} \tag{2}$$

where q and Z are the electron charge and device width, respectively; μ_p is the hole mobility in the VLD layer; W_2 is the expanding width of the depletion region edge in Fig. 3 (a); T_{b1} is the thickness of undepleted region edge at $x = 0$ in Fig. 3 (a).

The effective output capacitance can be given by [13]:

$$C_O = \frac{qZT_{soi}\Delta p(W_2)}{1-\alpha_{PNP}} \frac{dW_2}{dV_A} \tag{3}$$

where $\Delta p(W_2)$ is excess hole profile of the proposed device in the on-state, α_{PNP} is the common base gain of PNP transistor.

Furthermore, C_O can be obtained by submitting Eq. (1) and Eq. (2) into Eq. (3):

$$\begin{aligned} C_O &= \frac{q^2Z^2T_{soi}\Delta p(W_2)}{1-\alpha_{PNP}} \frac{\mu_p N_b(W_2)T_b}{I_{on}} \\ &= \frac{q^2Z^2T_{soi}\Delta p(x)}{1-\alpha_{PNP}} \frac{\mu_p N_b(x)T_b}{I_{on}} \\ &= \frac{q^2Z^2T_{soi}\Delta p(x)}{1-\alpha_{PNP}} \frac{\mu_p (Q - GT_b x)}{I_{on}} \end{aligned} \tag{4}$$

In phase II, $dV_A/dt = I_A/C_O = I_{on}/C_O$. Therefore, larger Q leads to larger capacitance effect, and results in a smaller dV_A/dt. Consequently, in phase II, the gross anode voltage reduces, results in a smaller the phase II loss (E_{off}^{II}). It is worth to note that the buried layer is only partially depleted due to the high doping concentration near the side of AB, which is different from UPB LIGBT.

As illustrated in Fig. 4, during the phase IV ($t_3 \le t \le t_4$), carriers are recombined and removed in the undepleted regions while the anode current (I_A) is dropping. Obviously, the phase IV loss (E_{off}^{IV}) can be given by:

$$E_{off}^{IV} = V_D \cdot \int_{t_3}^{t_4} I_A dt = V_D Q_u \tag{5}$$

$$Q_u = Q_{u1} + Q_{u2} + Q_{u3} \tag{6}$$

where Q_{ui} is the charge in undepleted region i, Q_u is the total charge in the undepleted regions and V_D is the power supply voltage. It is assumed that the excess hole profile still obeys the carrier distribution in on-state [16]. Hence, Q_{u1} and Q_{u2} can be obtained as [16]:

$$\begin{aligned} Q_{u1} \approx{}& \frac{1}{2}qN_d D_b W_{up} A \\ &+ \frac{1}{2}\left(P_0 + P_{W_{up}}\right)qAL\tanh\left(W_{up}/2L\right) \end{aligned} \tag{7}$$

$$\begin{aligned} Q_{u2} \approx{}& \frac{1}{2}qN_d(T_{soi} - T_b - D_b)W_{up}A \\ &+ \frac{1}{2}\left(P_0 + P_{W_{down}}\right)qAL\tanh(W_{down}/2L) \end{aligned} \tag{8}$$

$$Q_{u3} \approx \frac{1}{2}qN_{A'B'}L_b A \tag{9}$$

$$W_{up} \approx W_{down} = L_b - \sqrt{\left(\frac{V_D - V_2}{V_{BR} - V_2}\right)}L_b \tag{10}$$

where A and L are the areas of depletion boundary and bipolar diffusion length, respectively. W_{up} and W_{down} are the lengths of undepleted region 1 and undepleted region 2, respectively, and they are treated as equal for simplicity. P_0, $P_{W_{up}}$ and $P_{W_{down}}$ are the hole concentrations at $x = 0$, W_{up} and W_{down}, respectively. $N_{A'B'}$ is the doping concentration of buried VLD layer that approaches to the side of A′B′ at t_3. V_{BR} is the breakdown voltage of the proposed device. Based on analysis of the phase II, a larger Q leads to a smaller V_A in phase II, and results in a smaller V_2. Consequently, lower W_{up} and W_{down} can be obtained according to Eq. (10), and E_{off}^{IV} reduces. Therefore, a larger Q leads to a smaller E_{off}^{IV}.

To summarize, the existence of the buried VLD layer increases the effective output capacitance and decreases the storage charges in the drift region, thus reducing the turn-off loss (E_{off}).

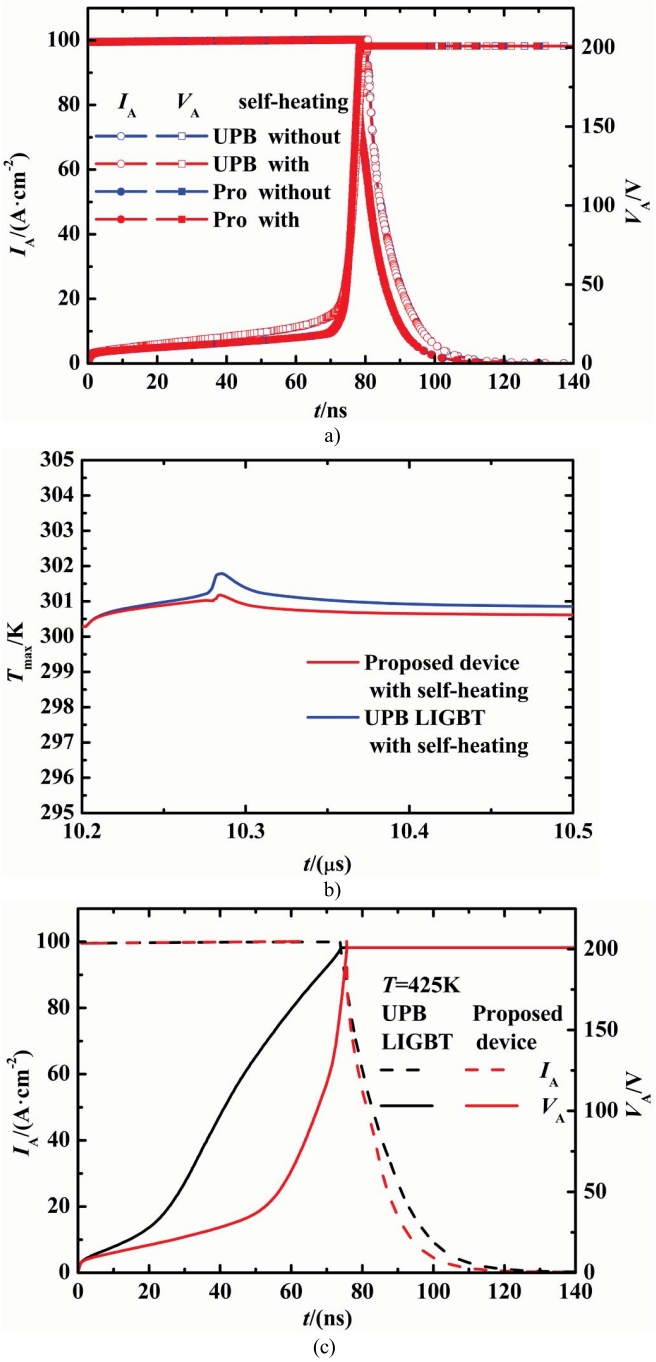

FIGURE 5. **(a) Turn-off waveforms of UPB LIGBT and the proposed device with or without self-heating effect (b) Maximum temperature of UPB LIGBT and the proposed device versus time considering self-heating effect during turn-off process (c) Turn-off waveforms of UPB LIGBT and the proposed device at 425K.**

III. RESULTS AND DISCUSSIONS

A 2D semiconductor device simulator, Synopsys TCAD, is applied to further explore the turn-off loss reduction mechanism of the proposed new device. An ambient temperature of 300K, a minority carrier lifetime of 1μs are used. The on-state current (I_{on}) is 100A/cm^2, and the forward conductive voltage (V_{on}) is about 1.13V. Besides, the power supply

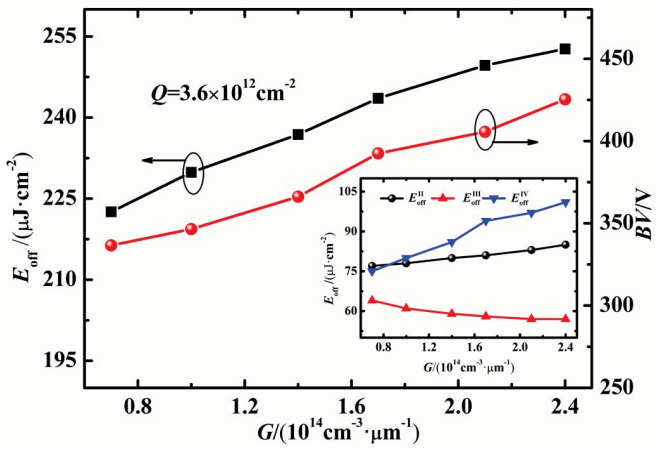

FIGURE 6. **The dependence of E_{off} and BV on concentration gradient (G) of the proposed device.**

voltage (V_D) is 200V. Furthermore, on-state gate voltage (V_G) is 15V. The simulating circuit and gate voltage sequence are shown in Fig. 10.

A. INFLUENCE OF THE SELF-HEATING EFFECT AND TEMPERATURE

Fig. 5 (a) shows the comparison of turn-off waveforms of UPB LIGBT and the proposed device with or without self-heating effect at room temperature of 300K. Simulation shows that there is almost no difference under surface-resistance of 100 cm^{2}K/W. Fig. 5 (b) shows the comparison of maximum temperature (T_{max}) considering self-heating effect during turn-off process for both UPB LIGBT and the proposed device. The results reveal that there is little variation of temperature in turn-off process. Therefore, self-heating effect is ignored when we research dynamic characteristic of UPB LIGBT and the proposed device. Fig. 5 (c) exhibits turn-off waveforms of UPB LIGBT and the proposed device at 425K. Environment temperature has great impact on dynamic characteristic of the two above devices. Turn-off losses of the proposed device and UPB LIGBT degenerate at a higher temperature of 425K due to the longer minority carrier lifetime. The proposed device can suppress the deterioration owing to faster depletion. Turn-off loss of proposed device can reduced by 73% compared with UPB LIGBT. That is to say, the proposed device is superior to UPB LIGBT at high temperature.

B. INFLUENCE OF THE DOPING PARAMETERS

Fig. 6 shows the dependence of E_{off} and BV on concentration gradient (G) of the proposed device. For $Q = 3.6 \times 10^{12}$cm^{-2}, both E_{off} and BV increase with the increase of G. One of the most distinctive features of the proposed device is G. The variation of G affects the turn-off loss significantly. As discussed above, the E_{off} is mainly composed of E_{off}^{II}, E_{off}^{III} and E_{off}^{IV}. In the phase II and phase III, the resistance of undepleted P-buried VLD layer increases with

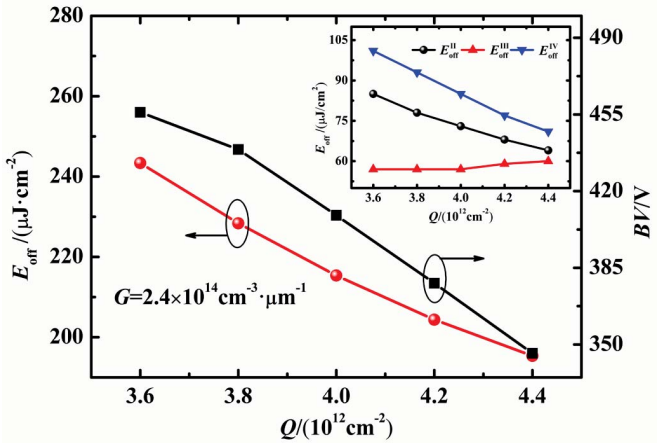

FIGURE 7. The dependence of E_{off} and BV on doping dose (Q) of the proposed device.

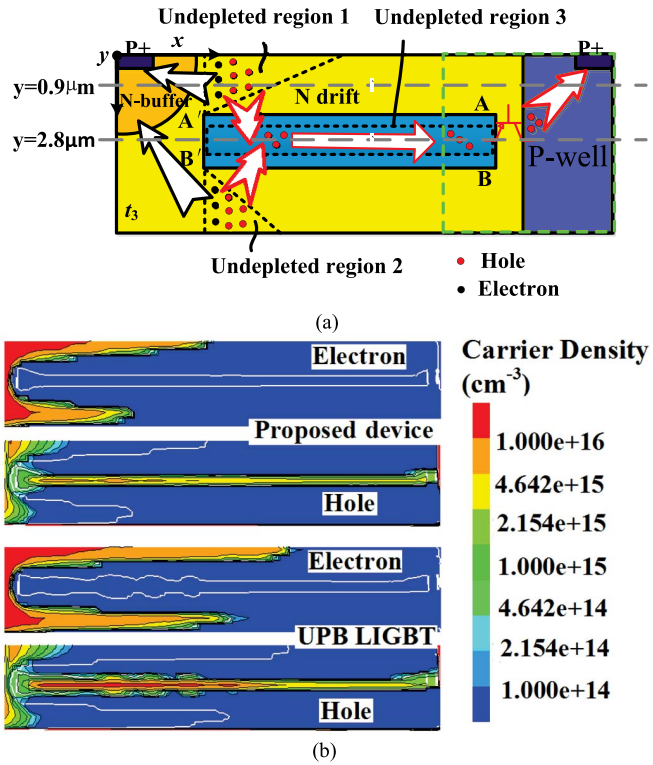

FIGURE 8. (a) The carrier movements in proposed device at t_3 (b) The comparison of carrier distribution in the proposed device and UPB LIGBT at t_3.

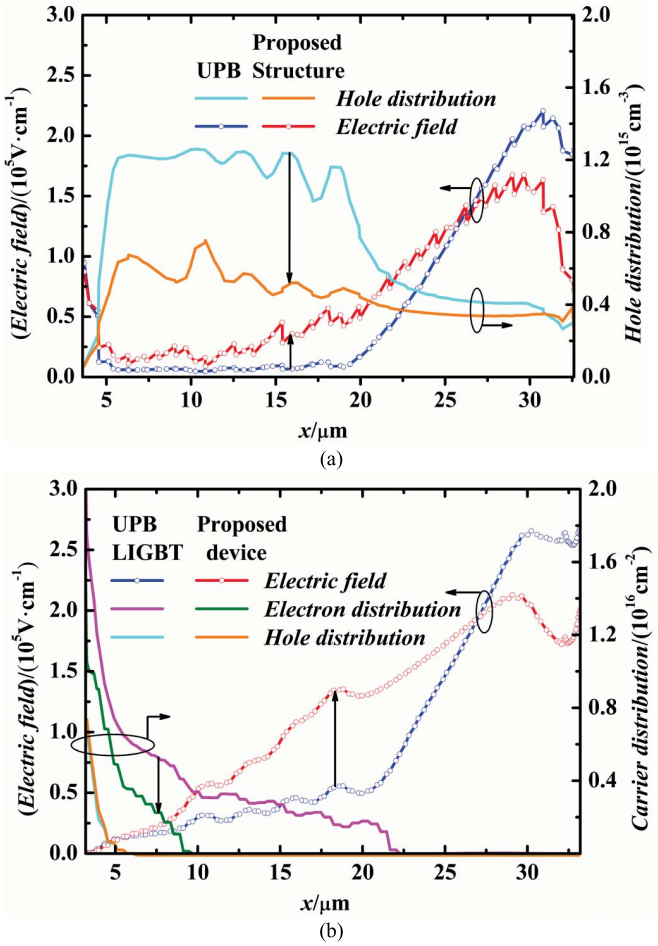

FIGURE 9. The comparison between the proposed device and UPB LIGBT at t_3. (a) The hole distribution and electric field along cutline $y = 2.8\mu$m. (b) The hole distribution, electron distribution and electric field along cutline $y = 0.9\mu$m.

a higher G, which further results in a higher V_2, E_{off}^{II} and a lower E_{off}^{III}. Meanwhile, in the phase IV, owing to the fact that the gross doping dose of the entire VLD layer is reduced, the assistant depletion effect of the buried layer is suppressed and thus increasing E_{off}^{IV}. Owing to the existence of the buried VLD layer, the surface electric field is reshaped and more even. Therefore, BV boosts with the increase of the G.

However, as shown in Fig. 7, for $G = 2.4 \times 10^{14}$cm^{-3}μm^{-1}, both E_{off} and BV decrease with the increase of Q. The E_{off} is mainly determined by E_{off}^{II} and E_{off}^{IV}. In the phase II, E_{off}^{II} significantly decreases with the increasing of Q due to a lower V_2, which has been discussed in Section II. Whereas, for the phase IV, a higher Q leads to a higher assistant depletion effect of VLD layer on the drift region, which diminishes the storage charges and thus drags E_{off}^{IV} down.

Moreover, Fig. 8 and Fig. 9 further depict the influence of embedded VLD layer on turn-off process. As shown in Fig. 8 (a), when $t = t_3$, electrons in undepleted region 1 and undepleted region 2 move through N-Buffer and are collected by the anode under the electric field. Meanwhile, the holes in these regions are swept into VLD layer and travel to the cathode. Apparently, the side of AB of the VLD layer acts as an emitter while the P-well and inner P+ region can be treated as a collector. Furthermore, the N-drift region between the P-well and VLD layer acts as a base region. Therefore, a narrow base PNP transistor is formed accordingly. Since the equivalent base region is actually very narrow, the common base current amplification factor tends to 1, which helps the holes travel into P-well. As shown in

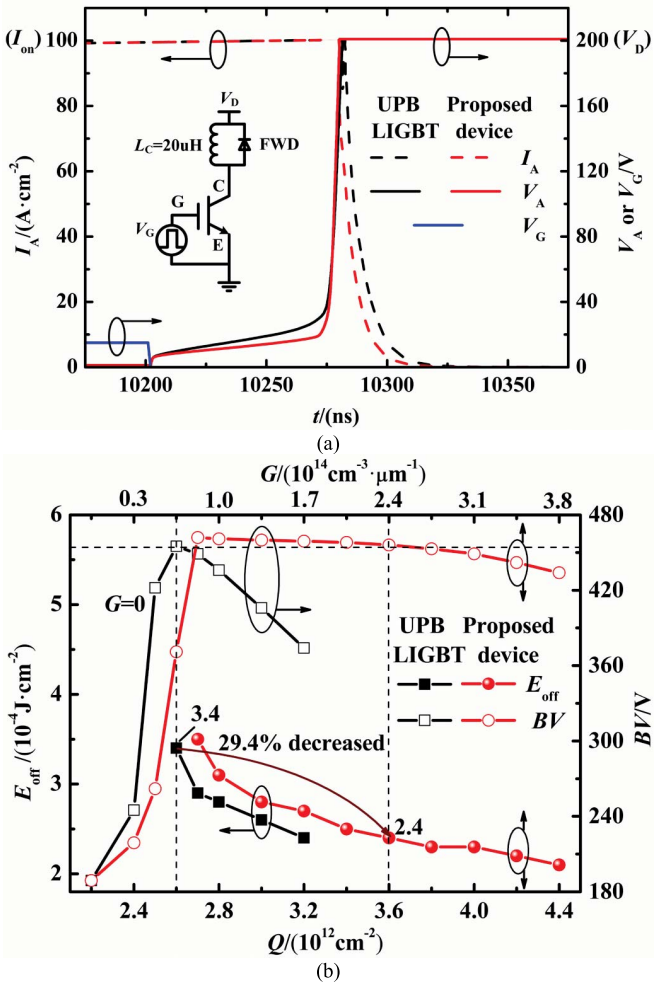

FIGURE 10. (a) Simulated turn-off waveforms and gate waveform of the proposed device and UPB LIGBT (b) E_{off} and BV of the proposed device and UPB LIGBT versus Q and G.

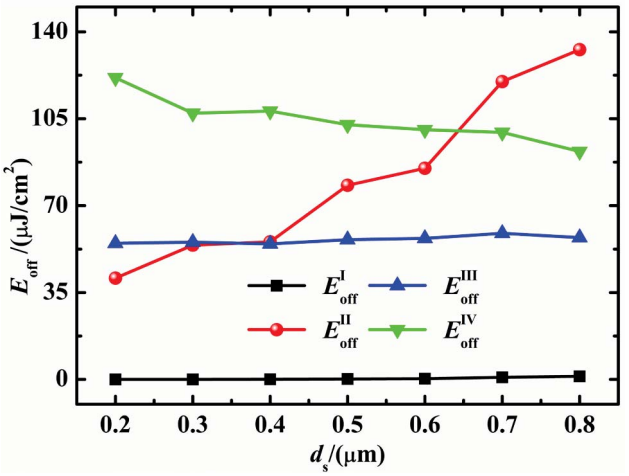

FIGURE 11. The dependence of E_{off}^{i}(i = I, II, III, IV) of the proposed device on d_s.

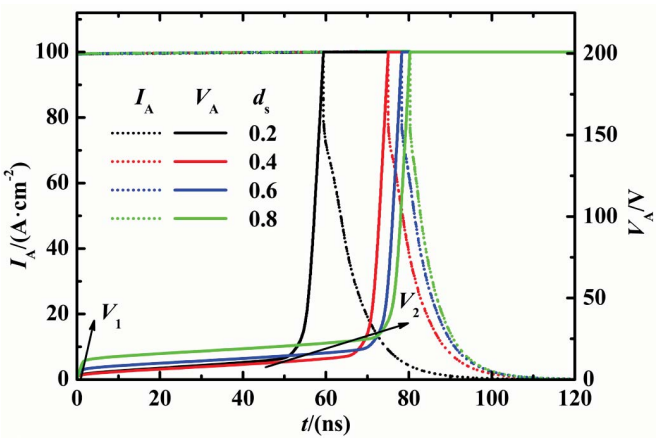

FIGURE 12. Simulated turn-off waveforms of the proposed device with different d_s.

Fig. 8 (b), the distribution of 2-D carrier density indicates that the depletion region in the drift region of the proposed device is shrunk due to the buried VLD layer compared with that in UPB LIGBT, which results in a smaller E_{off}^{IV}. Due to G, the buried VLD layer also reshapes the electric field distribution in the drift region. As shown in Fig. 9, the electric field rises in the area with higher carrier concentration. Therefore, the carriers can obtain a higher energy and speed of traveling to the corresponding electrode, which promotes the extraction of the excess carriers.

Fig. 10 (a) shows simulated turn-off waveforms of the proposed device and UPB LIGBT with parameters in table 1. With the increase of Q, E_{off}^{II} and E_{off}^{IV} significantly reduce. Fig. 10 (b) shows E_{off} and BV of the proposed device and UPB LIGBT versus Q and G. With the increase of Q and G, both BV curves first increases and then decreases. However, BV curve of the proposed device has the larger optimization range of Q. With the same BV, the proposed device achieves a 29.4% lower $E_{off}(2.4\times10^{-4}\text{J}\cdot\text{cm}^{-2})$ than that of UPB SOI LIGBT ($3.4\times10^{-4}\text{J}\cdot\text{cm}^{-2}$).

C. INFLUENCE OF THE DEVICE PARAMETERS

Fig. 11 illustrates the E_{off} as a function of d_s. For L_b = 29μm, with the increase of d_s, E_{off}^{II} significantly increases. The increase of d_s leads to the increase of the depletion edges expanding distance in phase I. Consequently, V_1 and V_2 increase, and result in a higher E_{off}^{II}, which is shown in Fig. 12. The depletion assistant effect is weakened with the increase of d_s. If d_s is too small, it would induce more carriers stored in the drift region. Consequently, E_{off}^{IV} decreases. As a result, a smaller or larger d_s would lead to a higher E_{off}. Taking process into consideration, d_s of 0.6μm is used for the device optimization.

The sensitivity of the E_{off}, E_{off}^{II}, E_{off}^{III} and E_{off}^{IV} as a function of L_b are depicted in Fig. 13. E_{off} is mainly determined by E_{off}^{IV}. As L_b increases from 25μm to 29μm, the assistant depletion effect is enhanced, and thus the storage charge in the drift region reduces. And larger L_b results in stronger ability of storage charge extraction. Consequently, E_{off}^{IV} decreases, as shown in Fig. 13. As

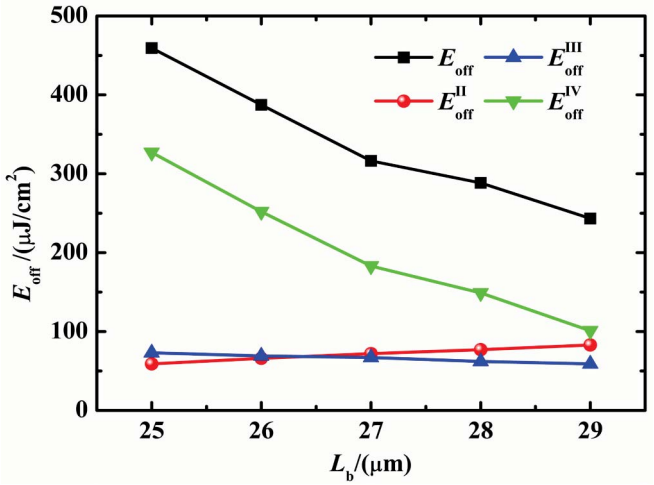

FIGURE 13. The dependence of turn-off loss of the proposed device as a function of L_b.

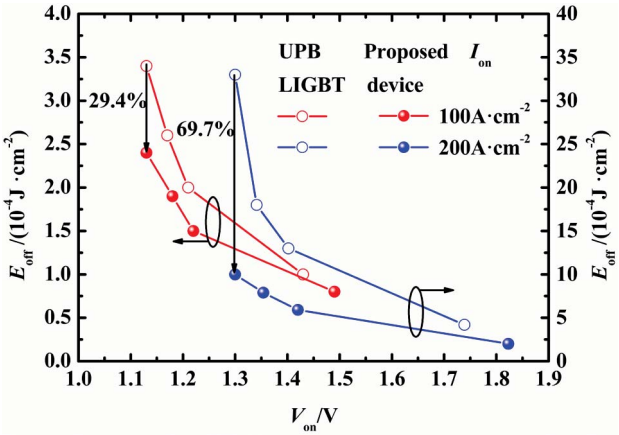

FIGURE 14. Tradeoff between E_{off} and V_{on} of the proposed device and UPB LIGBT at 100A·cm^{-2} and 200A·cm^{-2}, respectively.

a result, larger L_b will lead to smaller E_{off}. Therefore, L_b of 29μm is used for the device optimization, which is close to L_d.

D. TRADEOFF OF E_{OFF} AND V_{ON}

Fig. 14 shows that the proposed device behaves much better tradeoff between E_{off} and V_{on} than the UPB LIGBT under different on-state current. The E_{off} of the proposed device falls by 29.4% compared with that of the UPB LIGBT at 100A·cm^{-2}. However, the E_{off} of the proposed decreases by up to 69.7% compared with that of the UPB LIGBT at 200A·cm^{-2}. Fig. 15 shows the simulated turn-off waveforms of the proposed device and UPB LIGBT at 200A·cm^{-2}. Obviously, for UPB LIGBT, the capacitance effect becomes weaker at larger I_{on}. However, the turn-off characteristic of the proposed device is less influenced by larger I_{on}. Therefore, the proposed device has greater advantage for low E_{off} over the UPB LIGBT while turning off at larger I_{on}.

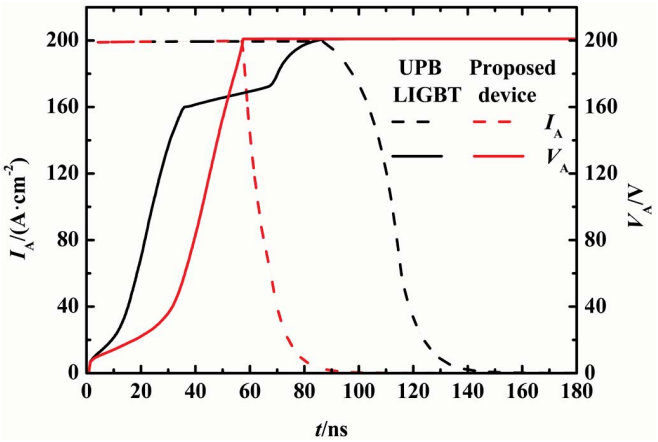

FIGURE 15. Simulated Turn-off waveforms of the proposed device and UPB LIGBT at 200A·cm^{-2}.

IV. CONCLUSION

In order to improve the tradeoff between the turn-off loss and breakdown voltage, a new low turn-off loss SOI LIGBT with buried VLD layer is proposed in this paper. By embedding a P-type VLD layer into the drift region, a partially depleted drift region and a larger effective output capacitance can be obtained, and resulting a lower E_{off}^{II} in phase II. Furthermore, E_{off}^{IV} decreases due to the less stored charges in shrunk depletion region. Therefore, the E_{off} can be improved significantly during turn-off process. Moreover, the buried VLD layer is also beneficial to excess carriers extraction and the optimization of breakdown voltage. The influences of VLD layer on BV and E_{off} are investigated in detail. The results of 2D simulation indicate that the proposed device can achieve a 29.4% lower turn-off loss and a 69.7% lower turn-off loss at 100A·cm^{-2} and 200A·cm^{-2}, respectively, when compared with SOI UPB LIGBT. Among various solutions to achieve high performances for SOI LIGBT, the buried VLD technique exhibits the more excellent balance between BV and E_{off}.

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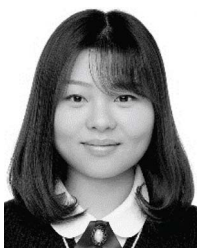

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