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# Proton Conductor Gated Synaptic Transistor Based on Transparent IGZO for Realizing Electrical and UV Light Stimulus

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**ABSTRACT** Synaptic transistors mimicking the biological synapse's short term plasticity and short-term memory property were demonstrated using the amorphous indium–gallium–zinc oxide channel in combination with the nanogranular $SiO_2$ as the gate oxide. The lowest energy consumption was ~1.08 pJ per pulse activity and the operating voltage was within 100 mV. The device's plasticity and memory characteristics can be explained by the movement of protons in the insulating layer. The proton relaxation was revealed by two ways of dual sweeping: continuous and discontinuous sweepings. We observed that the excitatory postsynaptic current (EPSC) rose as the voltage decreased anomaly during the backward sweeping process. In the electrical stimulus, both the short-term potentiation and depression were observed for this proposed device. The amplitude of the EPSC changed with the pulse number following a saturating exponential function. For the electrical stimulus under constant illumination, the UV light wavelength, intensity and duration time were found to have little effect on the paired pulse facilitation. While in the light stimulus, the light frequency promoted the paired pulse facilitation and had more effect on the synapse's plasticity than the other light pulse parameters including intensity, numbers and width.

**INDEX TERMS** Synaptic transistor, transparent oxide, IGZO, nanogranular $SiO_2$, UV light.

## I. INTRODUCTION

The human brain has a huge advantage of handling a complicated problem over the conventional computers because of the complex neural network that consists of about 100 billion neurons connected by biological synapses [1]. Extensive researches have been carried out to study the mechanism of biological synapses and mimic their functions using electronic devices in hope to realize the parallelism, structural plasticity and robustness of a human brain [2], [3]. Many kinds of two-terminal devices, such as memristors, resistive switches and proton-conducting devices [4]–[7] and three-terminal devices, such as ionic/electronic, proton conductor oxide and organic materials devices [8]–[14], have been used to simulate the biological synapses. Three-terminal synapse transistors can realize the transmission by the semiconductor channel and the learning by adjusting the interaction between the channel and the insulating layer simultaneously, but the two-terminal devices cannot. The EPSC values vary as the gate signal changes in the width, frequency and amplitude, which is similar to how the brain controls the neurons responding to environmental change. Some synaptic transistors have been reported to mimic the human brain to learn and remember by tuning the stimulus' pulse property or being given a series of rehearsals [15], [16].

Amorphous indium–gallium–zinc oxide (α-IGZO) is a transparent conducting oxide with excellent electron transport properties. It has an energy bandgap of around 3.3 eV and can be easily formed at room temperature [16], [17]. IGZO-based synaptic transistors are very promising to realize energy-efficient synaptic operations [18], [19]. Aixal *et al.*

found that the $SiO_2$ dielectric films deposited at room temperature by plasma-enhanced chemical vapor deposition (PECVD) method had a special microporous structure with a huge electric-double-layer capacitance, making it possible to realize synaptic plasticity [20]–[22]. Recently, synaptic transistors with $HfO_x$ insulating layer/IGZO channel layer or nanogranular $SiO_2$ insulting layer/Si channel layer have been fabricated and realized the LTD [16] or the short-term potentiation (STP)behavior [20], but not simultaneously. However, the mechanism of the memory property hasn't been analyzed in detail in the aforementioned $SiO_2$-based synaptic transistors researches that have largely ignored the proton relaxation in the $SiO_2$. Moreover, as moderate UV exposure can enhance the brain's learning, object recognition and memory ability by promoting a novel glutamate biosynthetic pathway in the brain [23], it is urgent now to study the UV light effects on the synaptic transistors in detail [24], [25].

In this work, a synaptic thin film transistor combining nanogranular $SiO_2$ with IGZO was fabricated. Both the STP and the short depression (STD) were observed. It was shown that the amplitude of the EPSC changes with the pulse number following a saturating exponential function. In addition, the ionic charge relaxation in the nanogranular $SiO_2$ was revealed by two ways of dual sweeping: continuous and discontinuous sweepings. Furthermore, in addition to the gate, source and drain terminals, UV light was found to be another effective controlling terminal of the synaptic transistor in the light stimulus. The frequency of the light pulse had an obvious effect on the synaptic transistor's plasticity and promoted the paired pulse facilitation (PPF) and the EPSC gain. In this work, the device was made to work under 0.1 V, the drain to source voltage ($V_{DS}$) was 1 mV and the energy consumption was ~1.08 pJ per pulse activity.

## II. DEVICE FABRICATION AND EXPERIMENTAL SETUP

The proton conductor gated synaptic transistors were fabricated on p-type Si wafers. First, microporous $SiO_2$ film of thickness 65 nm and 1 μm were deposited at room temperature using the ORION III PECVD system [16], [26]. At a pressure of 250 mTorr and an RF power of 100 W, reactive gases $SiH_4$, $O_2$, and Ar passed through the chamber at flow rates of 60 sccm, 10 sccm, and 10 sccm, respectively. Secondly, a 40-nm-thick α-IGZO film was deposited on the $SiO_2$ film by RF sputtering via a LAB-18 system at room temperature. During the IGZO deposition process, the concentration of $O_2$, pressure and RF power were 2%, 5 mTorr and 180 W, respectively [27]. Then, the active regions of the device were patterned by the UV lithography followed by a diluted hydrochloric acid (HCl) solution etching. Lastly, the source and drain electrodes were formed by lifting-off a 140 nm Mo metal layer by the LAB-18 with 250 W power in a 5 mTorr Ar atmosphere. The typical channel width and length were 80 μm and 10 μm, respectively. The device's electrical properties were measured by a semiconductor parameter analyzer Keithley B1500A at room temperature. The surface topography of the nanogranular $SiO_2$ was observed by a scanning electron microscope (SEM). The cross-section of the fabricated device was investigated using a high-resolution transmission electron microscopy (HRTEM, FEI Talos F200). A UV LED source with full intensity of 158.62 mW/cm$^2$ and three different wavelengths (365 nm, 395 nm and 405 nm) was used to illuminate the synaptic transistors in the light-related measurements.

Fig. 1(a) depicts the bottom-gate top-contact structure of the nanogranular $SiO_2$/IGZO synaptic transistor. Fig. 1(b) shows a typical SEM image of the surface of 65-nm-thick nanogranular $SiO_2$on Si substrate. The microporous structure is observed clearly. Fig. 1(c) illustrates a cross-sectional HRTEM image of the nanogranular $SiO_2$/IGZO synaptic transistor with a 65 nm gate oxide layer and Fig. 1(d) shows the zoom-in image. The thicknesses of the IGZO and $SiO_2$ are measured to be around 40 nm and 65 nm, respectively. The In, Ga, Zn, and O elements are uniformly distributed in the channel layer, as shown in Fig. S1, in the supplementary material. Moreever, it is interesting to note that the In element is precipitated from the IGZO layer and becomes crystallized at the $SiO_2$/IGZO interface, as shown in Fig. S2, in the supplementary material.

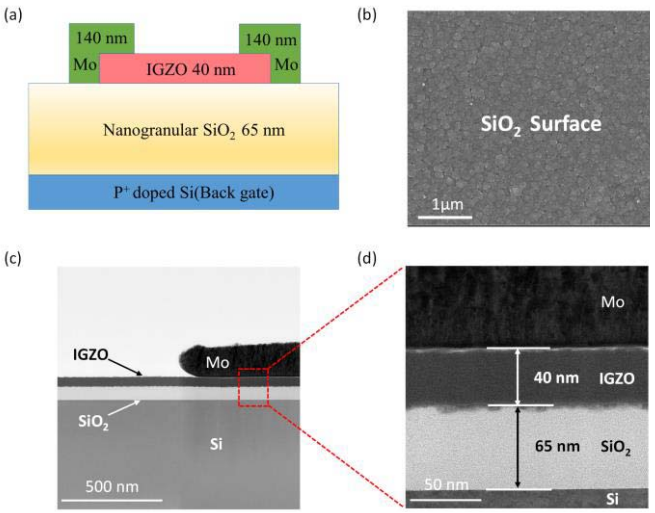


**FIGURE 1. Schematic and microstructure images of the fabricated transistor. (a) Schematic diagram of the proposed nanogranular $SiO_2$/IGZO synaptic transistor. (b) The SEM image of the nanogranular $SiO_2$ surface. (c) The cross-sectional TEM image of the fabricated synaptic transistor. (d) The enlarged TEM image of the area marked by the red rectangle in Fig. 1(c).**

## III. RESULTS AND DISSCUSSION

Different from a conventional transistor, a synaptic transistor has a memory capability that the threshold voltage is affected by the mobile charges in the insulting layer. As shown in the Fig. 2(a), the threshold voltage of the backward sweeping becomes smaller than that of the forward sweeping. The interval between the forward and back sweeping is 10 s. The threshold voltage is defined as the gate voltage at which the drain current reaches 10 nA [28]. For the current-voltage

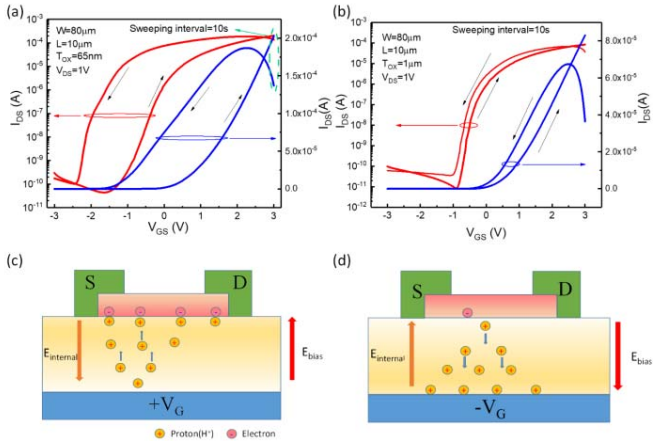


**FIGURE 2. Transfer curve of the fabricated transistor with different polarity gate bias. (a, b) Dual sweeping I-V data of the nanogranular $SiO_2$/IGZO synaptic transistor with (a) 65-nm-thick gate oxide and (b) 1-μm-thick gate oxide at $V_{DS}$ = 1 V, the red line for the logarithmic coordinates and the blue line for the linear coordinates. The forward and backward sweeping directions are indicated by arrow heads on the curves. (c, d) Schematic of electric-double-layer structures when the voltage applied on the bottom gate is (c) positive and (d) negative.**

(I-V) sweeping, the gate voltage ranges from −3 V to 3 V with the drain to source voltage ($V_{DS}$) fixed at 1 V. The forward and backward sweeping directions are indicated by the arrow heads on the curves. The red line is shown in logarithmic coordinates and the blue line in linear coordinates. The device with a 65 nm gate oxide film shows a clear anticlockwise hysteresis due to the mobile ionic charges. The calculated memory window, i.e., the change of threshold voltage, is up to 1.48 V. The drain current on/off ratio and subthreshold swing of the device are $4.3 \times 10^6$ and 120 mV/decade, respectively. Fig. 2(b) shows the dual sweeping transfer curves of another device with 1-μm-thick gate oxide. The measured memory window width is 0.165 V, much smaller than that of the device with a 65 nm-thick gate oxide. The anticlockwise hysteresis of the devices can be explained as follows. When a positive gate voltage is applied to the bottom gate, electrons will be induced in the IGZO channel as the mobile protons drift to the interface and accumulate, as shown in Fig. 2(c). Hydrogen dissociated from $SiH_4$ during the PECVD process can enter the nanogranular $SiO_2$ matrix as $Si–OH^+$ and formed the protons [18]. When a negative gate voltage is applied, the protons will be pulled away from the interface, as shown in Fig. 2(d). As the electric field strength is inversely proportional to the oxide thickness under a constant gate voltage, less protons drift to the insulator/channel interface inside the 1-μm-thick gate oxide in comparison to the 65-nm-thick one. As a result, the memory window of the device with a 1μm gate oxide is narrower than that of the device with a 65 nm gate oxide. In this paper, all the measurements referred below are based on the 65 nm-thick nanogranular $SiO_2$ device unless specially stated.

To find whether the protons move away from the insulator/channel interface to their equilibrium position, two different sweepings were used: continuous sweeping and discontinuous sweeping. In a continuous sweeping, the gate voltage was swept from −3 V to 3 V (forward) and back to −3 V (backward) without any interval. Whereas for the discontinuous sweeping, there is a 10 s break. As shown in Fig. 3(a), the starting drain current reduced in the magnitude and the drain current first rose as the gate voltage during the discontinuous sweeping. During the interval, the protons will move to their equilibrium positions naturally, which is called the protons relaxation and it makes the electrons in the channel reduces. That's why the starting drain current of backward sweeping is smaller than the ending drain current of forward sweeping. As the gate voltage is swept back, the electric field pushes more protons to the interface when the gate voltage is still positive. Thus, the current increases as the gate voltage decreases until the impact of voltage reduction surpasses the impact of protons induction on the channel. As shown in Fig. 3(b), the gate leakage is within 3 nA during the two different sweeping process. Fig. 3(c) shows that the nanogranular $SiO_2$ based synaptic transistor has a good stability after three times of the discontinuous sweeping with an interval of 30 s by using a new fresh device to measure. The dependence of the memory window on the gate sweeping range is shown in Fig. 3(d). For the device with a 65-nm-thick gate oxide, the memory window is 0.14 V within a sweeping rang of −4 V to 1 V and changes to 1.43 V within a sweeping rang of −4 V to 4 V. The larger the $V_{GS}$ is, the more protons accumulate near the nanogranular $SiO_2$/IGZO interface.

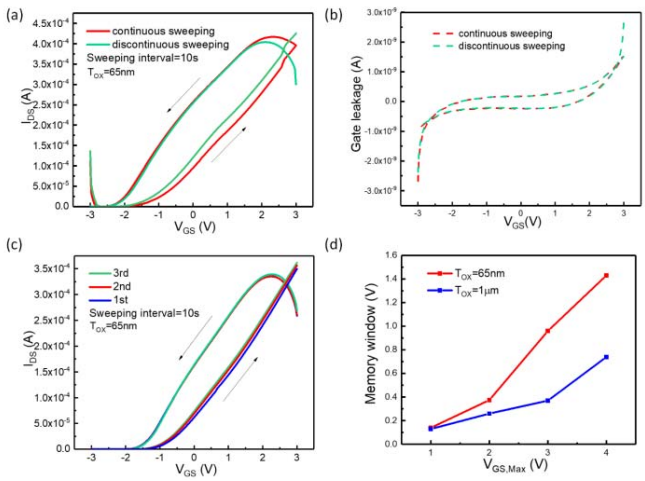


**FIGURE 3. Electrical performance of the fabricated transistor. (a) Comparison of the I-V curves between the discontinuous sweeping and continuous sweeping for the 65-nm-thick gate oxide device. (b) The gate leakage during the continuous and discontinuous sweeping. (c) Three times of discontinuous I-V sweeping for the 65-nm-thick gate oxide device. (d) The relation between the threshold voltage change (i.e., memory window) and the gate voltage sweeping range. All the measurements are with $V_{DS}$ of 1 V.**

Fig. 4(a) depicts the analogy between a biological synapse and a nanogranular $SiO_2$ based synaptic transistor: the bottom gate is similar to the presynapse, the protons in the

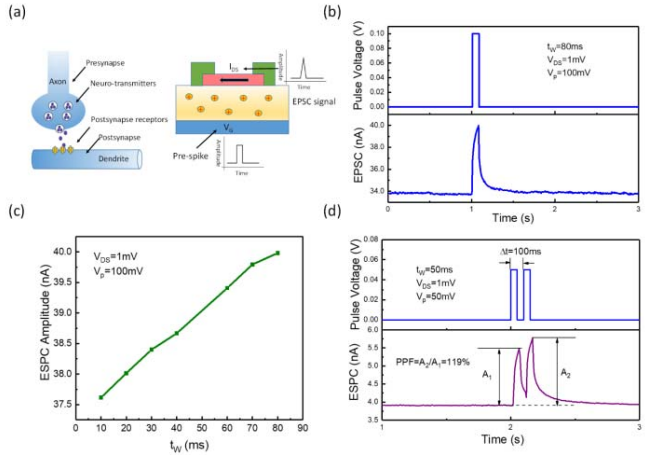


**FIGURE 4. Excitatory postsynaptic current triggered by electrical pulses. (a) An analogy between the biological synapse and the artificial synaptic device in this work. The post-synapse's strength is decided by the amount of the neuro-transmitters for the biological synapse while the strength is affected by the protons in the insulator for the synaptic transistor. (b) EPSC (bottom panel) triggered by a presynaptic spike (100 mV, 80 ms) (top panel). The EPSC is measured with $V_{DS}$ of 1 mV. (c) The relation between the EPSC amplitude and the presynaptic spike width, measured with a pulse voltage of 100 mV and $V_{DS}$ of 1 mV. The amplitude of the pulse voltage is defined as $V_P$. (d) A pair of presynaptic pulses and the EPSC triggered by the pulses, with a pulse width of 50ms, pulse voltage of 50 mV, $V_{DS}$ of 1 mV and pulse interval of 100 ms. $A_1$ and $A_2$represent the amplitudes of the first and second EPSC, respectively.**

insulator are equivalent to the neuro-transmitters in the synapse cleft, and the source electrode /channel/ drain electrode corresponds to the postsynapse. To verify the device's synaptic function, a pre-spike pulse (100 mV, 80 ms) was applied on the bottom gate with a $V_{DS}$ of 1 mV, as shown in Fig. 4(b). The pulse width and voltage amplitude are defined as $t_W$ and $V_p$, respectively. The EPSC through the channel is from 33.8 nA to 39.8 nA at the end of the spike, after which the current decays slowly due to the proton relaxation described by an exponential relation [3]. The calculated energy dissipation of a single spike event is ~3.18 pJ, which is much lower than that of the reported nanogranular $SiO_2$-based proton conductor gated synaptic transistors(~160 pJ) [16] and zinc oxide based synaptic devices (~35 pJ) [9]. The energy dissipation per spike is calculated by $E = I_{peak} \times t_W \times V_{DS}$, where E is the energy dissipation per spike, $I_{peak}$ is the spike peak current, $t_W$ is pulse width and $V_{DS}$ is the drain to source voltage. Fig. 4(c) shows that the EPSC amplitude increases with the presynaptic spike width, measured with a $V_{DS}$ of 1 mV and $V_p$ of 100 mV. As the spike width ($t_W$) varies from 10 ms to 90 ms, the EPSC amplitude changes from 37.6 nA to 40 nA correspondingly. The number of the protons accumulated at the IGZO/$SiO_2$ interface is positively related to the time of gate spike and the number of the electrons induced in the IGZO channel increases as the pulse width linearly before the protons get saturated. So that the ESPC amplitude increase with the spike width linearly. This linearity may help build an analytical model of the ESPC amplitude with gate spike input parameters in a single spike activity. Another important property widely concerned with the synaptic transistor is the paired pulse facilitation (PPF) in which the EPSC triggered by the second pulse will be enhanced by the first pulse due to the memory effect [29]. A pair of pulses were added to the bottom gate with the pulse width of 50 ms, pulse voltage of 50 mV, interval of 100 ms and $V_{DS}$ of 1 mV. As shown in Fig. 4(d), the PPF ($A_2/A_1$) reaches 119%, where $A_1$ and $A_2$ represent the amplitudes of the first and second EPSC, respectively.

To observe the PPF effect better, a train of 10 pulses was taken to investigate the PPF phenomenon with the $V_{DS}$ of 1 mV, pulse width of 80 ms and pulse interval of 100 ms. As shown in Fig. 5(a), the current pulse EPSC was larger than the previous one, which corresponds to the short-term potentiation. The amplitude of the tenth EPSC signal and the amplitude of the first post synaptic signal were defined as $A_{10}$ and $A_1$ and their ratio reaches 180%. It could be found that when the $V_p$ was reduced to 50 mV, the least energy consumption of a single spike even dropped to 1.08 pJ, calculated by $E = I_{peak} \times t_W \times V_{DS} = 13.5nA \times 80ms \times 1mV = 1.08pJ$. As explained above, the protons near the insulator/channel interface will relax to their equilibrium positions. However, there is a relaxation time and part of the protons induced by the prior pulse still exists near the interface, which results in an enhanced EPSC when the next pulse comes. The short-term depression of the synaptic device was also observed. As shown in Fig. 5(b), the EPSC reduced as the pulse train went, measured with a $V_p$ of −50 mV because the proton reduced near the interface under the negative gate voltage. This measurement was taken with a device after proton accumulation. As shown in Fig. 5(c), 5(d), the amplitude of the spike current changed with the pulse number can be described using a saturating exponential function:

$$A_N = A_0 + r \bullet \exp(-\frac{N}{N_0}) \quad (1)$$

where $A_N$ represents the Nth amplitude of the spike current, N is the pulse number in the pulses train, $A_0$ is the final current which the EPSC is expected to reach, r is a constant current increment and $N_0$ is a constant. Fig. 5(e) describes the relation between the excitatory post synaptic current and the pre-spike frequency. Five groups of ten constant $t_W$ (50 ms) pulses were applied on the device successively with different frequency (2, 2.5, 3.3, 5, 10 Hz) with a $V_p$ of 100 mV and $V_{DS}$ of 1 mV, 5 mV. The EPSC potentiation was positively correlated to the pre-spike frequency as indicated in Fig. 5(f). The current gain, defined as $A_{10}/A_1$, increases with the pre-spike frequency, but is not affected by the amplitude of $V_{DS}$. This indicates that the structure fabricated has a potential to be used as a high-pass filter for information transmission.

Up to now, most reported synaptic transistors have been stimulated with electrical signals while few have concerned the light stimulus, which may have a much wider bandwidth and no RC delay for signal transmission [30]. It is urgent now to study the light effects on the electrical transistors

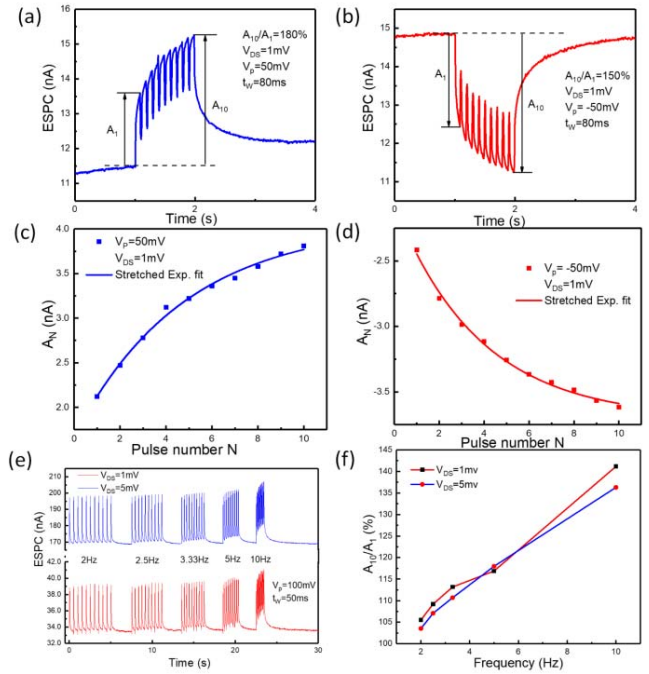


**FIGURE 5.** **Excitatory postsynaptic current triggered by a pulse train. (a) The EPSC measured with the synaptic transistor using 10 presynaptic pulses (50 mV, 80 ms) train with pulse interval of 100 ms. (b) The EPSC measured using 10 presynaptic pulses (−50 mV, 80 ms) train with pulse interval of 100 ms. (c), (d) The relationships between the EPSC amplitude and the gate spike pulse numbers, measured with (c) a positive pulse voltage $V_p = 50mV$, (d) a negative pulse voltage $V_p = -50mV$, extracted from Fig. 5(a), 5(b). Results from analytical model using a saturating exponential function are also plotted. (e) The EPSC with a constant pulse width of 50 ms where frequency is varied from 2 to 10 Hz at $V_{DS} = 1$ mV, 5 mV. (f) The EPSC versus pre-spike frequency where $A_{10}$ represents the amplitude of the 10th EPSC signal and $A_1$ represents the amplitude of the first post synaptic signal, extracted from Fig. 5(e).**

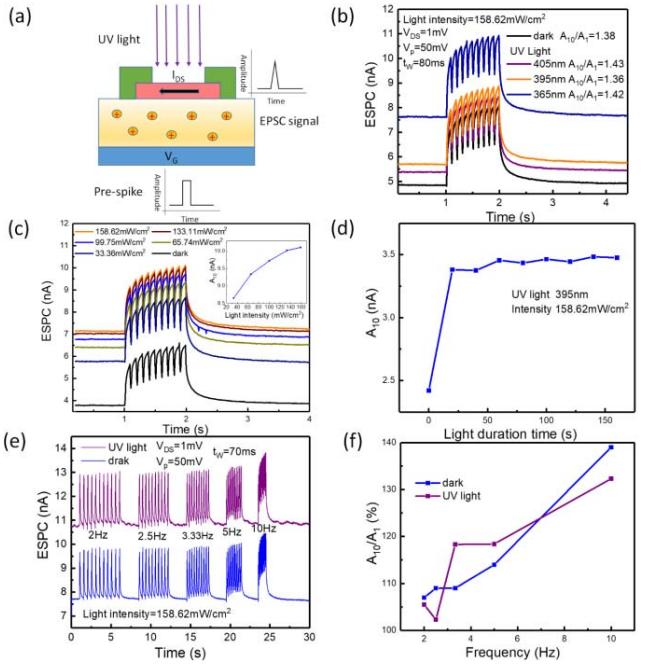


**FIGURE 6.** **Excitatory postsynaptic current by electrical pulses under the light illumination. (a) Schematic of the ultraviolet light illuminating the synaptic transistor. (b) The device's response to different wavelengths UV light using a ten pulse pre-spikes, measured with a pulse voltage of 50 mV, pulse width of 80 ms, $V_{DS}$ of 1 mV and light intensity of 158.62mW/cm$^2$. (c) The EPSC signal under different light intensity and the inset figure depicts the relation between the $A_{10}$ and the light intensity. Each intensity measurement is taken after 180 s illumination for the device to achieve steady state. (d) The tenth amplitude of the EPSCs signal versus the light illumination duration time with a 395 nm UV light and full intensity (158.62 mW/cm$^2$). (e) The EPSC signals with different frequency pulses under the 395 nm full intensity UV light. (f) The relation between the EPSC gain ($A_{10}/A_1$) and the frequency under the 395 nm full intensity UV light.**

in detail [31]. Another reason to explore the transistor's response to the UV light is that the biological synapse responds to the UV stimulus and moderate UV exposure contributes to the brain's improved learning, object recognition and memory ability [23].

In this work, the UV light is used as the assisting terminal to study the impact of the electrical stimulus and then the light is employed as the control terminal to investigate its influences on the synapse transistors. The band gap of the α-IGZO is about 3.36 eV and the synaptic transistor proposed in this paper should respond to the ultraviolet light. An ultraviolet LED (full intensity of 158.62 mW/cm$^2$) was used to illuminate the synapse, depicted in Fig. 6(a). UV light sources with three different wavelengths (365 nm, 395 nm and 405 nm) were used to measure the synapse sensitivity to wavelength and the results are shown in Fig. 6(b). The synapse's weight was strengthened by the UV light and the drain current increased most responding to the UV light of 365 nm from 4.85 nA to 7.61 nA with a $V_{DS}$ of 1 mV, $V_p$ of 50 mV and $t_W$ of 80 ms. In the electrical stimulus, constant UV light illumination can promote the device's conductance around 56%, but does not impact the EPSC gain, which remained at about 1.40 for the three kinds of wavelengths. Fig. 6(c) shows that the EPSC signal increases with the light intensity and the inset figure depicts the relation between the tenth amplitude of the EPSC and the light intensity. As the intensity increases, the EPSC grows fast first and then gradually levels off. Each light intensity measurement is taken after 180 s illumination for the device to achieve steady state. The response of the synapse to the light illumination time is shown in Fig. 6(d) and is similar to its response to the light intensity. Fig. 6(e), 6(f) show that the UV light does not influence the synapse transistor's relation between PPF index and the electrical pulse' frequency. The light wavelength, intensity and duration time show little effect on the synapse's plasticity with a constant illumination in the electrical stimulus. Next, the UV light will be an independent control terminal without electrical spikes to study the light's impact on the synapse transistor's plasticity.

In order to study the light terminal's influence on the synapse' plasticity, a light pulse was applied on the channel surface. As shown in Fig. 7(a), the EPSC increased rapidly after the light was turned on and decayed slowly after the light was turned off. Unless otherwise stated, the following

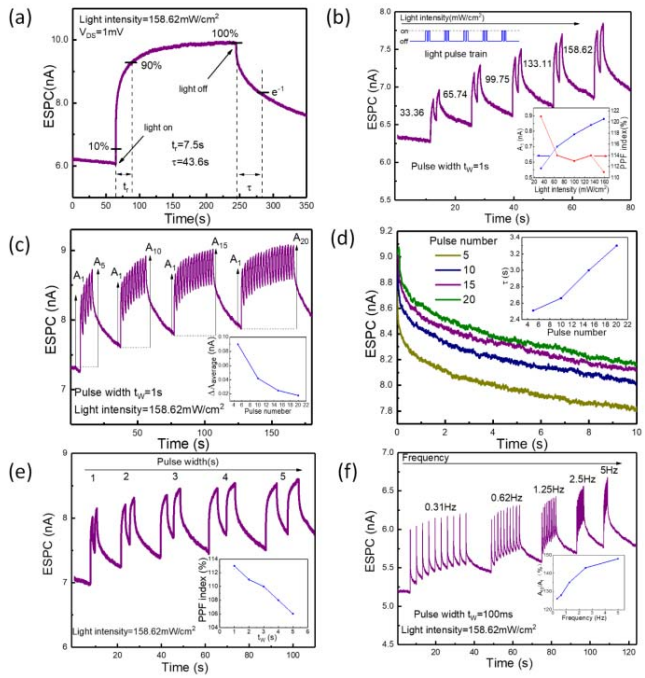


**FIGURE 7. Excitatory postsynaptic current triggered by light pulses. (a)The synapse's response to the UV light using the light as the control terminal with the gate floating, $V_{DS}$ of 1 mV and light intensity of 158.62mW/cm$^2$. (b) The EPSC spikes triggered by the ten light pulse train with five kinds of light intensity with pulse width of 1 s. The figure inset of (b) depicts the relation between the $A_1$, PPF ($A_2/A_1$) and light intensity. (c) The EPSCs triggered by light pulses train with different pulse number (5, 10, 15, 20), measured with light intensity of 158.62 mW/cm$^2$ and pulse width of 1 s. The figure inset of (c) depicts the relation between the average spike amplitude change and the section's pulse number. (d) The channel EPSC signal decays after applying different numbers of light pulse sections, extracted from Fig. 7(c). The inset of Fig. 7(d) depicts the relation between the retention time and the section's pulse number. (e) The EPSCs triggered by light pulses train with five sections of different pulse width, measured with a light intensity of 158.62 of mW/cm$^2$. The figure inset of (e) depicts the relation between the PPF and pulse width. (f) The EPSCs triggered by light pulses train with different pulse frequency, measured with light intensity of 158.62 mW/cm$^2$ and pulse width of 100 ms. The figure inset of (e) depicts the relation between the EPSC gain and pulse frequency.**

measurements were using the full intensity 395 nm UV light with the gate floating and $V_{DS}$ of 1 mV. The time for the current to rise from 10% to 90% of the whole dynamic range ($t_r$) was measured to be 7.5 s. The decaying characteristic after the light was turned off can be described by Equation (2) [30]:

$$I = (I_0 - I_{int}) \cdot \exp\left[-\left(\frac{t - t_0}{\tau}\right)^{\beta}\right] + I_{int} \qquad (2)$$

where $I_0$ is the current recorded immediately after the light pulse, $I_{int}$ is the device's current before any light illumination, $t_0$ is the time when the UV light is turned off, $\tau$ is the retention time, and $\beta$ is an index between 0 and 1. After 180 s UV light illumination, the EPSC rose from 6 nA to 10 nA and $\tau$ was 43.6 s. The current growth rate became smaller as the illumination time extended. The PPF effect was observed in the light stimulus, where a four-section train of pair pulses with different light intensity was applied on the synapse transistor, as shown in Fig. 7(b). One probable explanation of the synapse's plasticity is due to the inherent persistent photoconductivity (PPC) characteristic of the amorphous IGZO and the neutralization of ionized oxygen vacancies may take a long period, leading to the current decaying slowly after the light off [25]. As shown in the inset figure of Fig. 7(b), $A_1$ increased with the light intensity from 0.56 nA to 0.88 nA while the PPF ($A_2/A_1$) slightly decreased with the intensity. Fig. 7(c) describes the relation between the EPSC and the pulse number by using a four-section pulse train with 5, 10, 15, 20 pulses, respectively. The inset figure shows that the average amplitude-change decreased with the pulse number. Fig. 7(d), extracted from the Fig. 7(c), shows that the EPSC decayed with time after each light pulse section was finished. It is worth noting that the $\tau$ increases with the pulse number from 2.51 s to 3.30 s as the pulse number rises from 5 to 20, as shown in the inset of Fig. 7(d). Although the growth rate is small, after a 180 s illumination, $\tau$ can rise to 43.6 s according to Fig. 7(a). The ability to expand the feature time by adding pulse width and number is very important for synapse learning because this means that the STM (short term memory) to the LTM (long term memory) transition can be achieved by a series of rehearsal just like human learning and remembering activity. As shown in Fig. 7(e) and the inset figure, the PPF index slightly decreased with pulse width, measured with pair-pulse train with $t_W$ of 1 s, 2 s, 3 s, 4 s, 5 s, respectively. Fig. 7(f) describes the EPSC triggered by a ten-pulse train with five kinds of frequency. When the frequency was 0.31, 0.62, 1.25, 2.5, 5 Hz, the EPSC gain ($A_{10}/A_1$) was 126%, 128%, 135%, 143%, 148%, respectively, with a maximum of 17.5% increase. The higher the frequency is, the shorter the off-period of UV light is and more carriers accumulate in the channel layer. The important finding is that the frequency has more obvious effect on the synapse's plasticity than the other light pulse parameters including intensity, numbers and width.

## IV. CONCLUSION

In summary, a nanogranular $SiO_2$-based proton conductor sgated thin film synaptic transistor using IGZO was proposed in this paper. The synaptic transistor mimicked the biological synapse's short term plasticity and short term memory property. In addition to realizing electrical control of the synaptic transistor, the UV light is found to be another effective control terminal and this is important for the synaptic device to sense the light. However, fabricating a synaptic transistor network and system to realize the complex functions are existing challenges. It is promising to investigate the synaptic transistor's plasticity with multiple presynaptic inputs and using organic wearable insulator. Nevertheless, the work here shows that the nanogranular $SiO_2$/IGZO structure is attractive for the potential applications in synaptic electronics.

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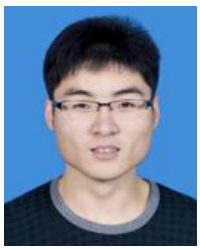

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