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Origin of High Mobility in InSnZnO MOSFETs

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ABSTRACT The origins of higher mobility characteristics of In-Sn-Zn-O (InSnZnO) MOSFETs than those of conventional In-Ga-Zn-O (InGaZnO) MOSFETs were investigated. Comprehensive analyses of temperature and surface carrier concentration (N_s) dependence of mobility revealed the aspects of potential profile around mobility edge (E_c) in InSnZnO MOSFET. Incorporated Sn atoms were found to increase the potential fluctuation around E_c at low N_s compared to conventional InGaZnO MOSFET, but enhance the overlapping of electron orbitals of cations with In atoms, which results in mobility improvement by band transport.

INDEX TERMS Oxide semiconductor, mobility, InSnZnO, InGaZnO, and BEOL.

I. INTRODUCTION

Recently, In-Ga-Zn-O (InGaZnO) channel MOSFETs in Si CMOS back end of line (BEOL) process have attracted much attention as a key device for CMOS extensions [1]-[5]. InGaZnO MOSFETs have unique characteristics such as low-temperature process (< 400°C), extremely low offstate current ($< 10^{-22}$ A/mm) and high breakdown voltage $(V_{BD} > 40 \text{ V})$ thanks to its large bandgap energy (~ 3.1 eV). Various applications such as embedded memories and high voltage I/Os by using InGaZnO BEOL transistor have been proposed [2]-[4]. However, conventional InGaZnO (In:Ga:Zn=1:1:1) shows low mobility $(5 \sim 15 \text{ cm}^2/\text{Vs})$, which limits the applications [1], [4]. Among oxide semiconductor materials, In-Sn-Zn-O (InSnZnO) has been reported to show higher mobility ($\sim 30 \text{ cm}^2/\text{Vs}$) than InGaZnO, but the origin of higher mobility is not clear [6], [7]. Several groups have investigated the carrier transport mechanism by the Hall measurements using InGaZnO and InSnZnO films with various carrier concentrations [6], [8], [9]. However, it is difficult to separate impacts of defect density in the films because the carrier concentration has been controlled via introducing oxygen vacancy (V_0) by hydrogen annealing process.

In this paper, we comprehensively investigated a temperature dependence of mobility for different oxide semiconductor channel MOSFETs by controlling surface carrier concentration (N_s) with gate voltage, and revealed impacts of incorporated Sn atoms on the mobility edge and the origin of high mobility in InSnZnO MOSFETs.

II. EXPERIMENT

Figure 1 (a) shows a cross-sectional transmission electron microscope (TEM) image of the fabricated oxide semiconductor channel MOSFETs. Bottom-gated and top-contact MOSFETs were fabricated. The channel length (L) is defined as a distance between source and drain (S/D) contact holes.

Figure 2 (b) shows a device fabrication process. Tungsten film was deposited on a thermally grown SiO₂ layer on Si substrate by sputtering method as a gate electrode and was patterned by photolithography. As a gate insulator, SiO₂ film with a thickness of 40 nm was formed by plasma enhanced chemical vapor deposition (PECVD). Next oxide semiconductor channel with a thickness of 15 nm was deposited by sputtering method at room temperature and patterned by photolithography. In addition to conventional InGaZnO (In:Ga:Zn=1:1:1), InSnZnO, In-Sn-Ga-O (InSnGaO) and Incomposition-rich InGaZnO were prepared in order to clarify the roles of each atom to mobility. Each composition ratio of the oxide semiconductor channel except for the conventional InGaZnO was adjusted so that the intrinsic carrier concentration was low ($< 10^{17}$ cm⁻³) and the threshold voltage (V_{th}) of all MOSFETs shows almost the same value ($V_{\rm th} \sim 0$ V). Also all oxide semiconductor films in this work were confirmed to be amorphous by TEM images. After an interlayer of SiO₂ film with a thickness of 150 nm was deposited by PECVD, S/D contact holes were opened. Then molybdenum film was deposited by sputtering and patterned to make S/D electrodes. Maximum process temperature during fabrication process was 350°C.









FIGURE 2. (a) Temperature dependence of I_d - V_g characteristics and (b) mobility characteristics of InGaZnO MOSFET measured from 300 K to 10 K. As the temperature is reduced, I_{on} decreases and V_{th} and S.S. increase and mobility decreases.

After the fabrication, N_s dependence of mobility was evaluated by split *C-V* method at the various temperatures from 300 K to 10 K. The channel length and the channel width were 50 μ m and 50 mm, respectively.

III. CARRIER TRANSPORT IN INGAZNO MOSFETS

Figure 2 (a) shows a temperature dependence of $I_{\rm d}$ - $V_{\rm g}$ characteristics of the conventional InGaZnO MOSFET measured from 300 K to 10 K. As the temperature was reduced, on-current ($I_{\rm on}$) was decreased, whereas $V_{\rm th}$ was increased and subthreshold swing (*S.S.*) became less steep. Figure 2 (b) shows the temperature dependence of mobility at fixed $N_{\rm s}$ values. As the temperature is reduced, the mobility was decreased from 13.9 cm²/Vs at 300 K to 2.8 cm²/Vs at 10 K for $N_{\rm s} = 10^{13}$ cm⁻². As $N_{\rm s}$ increases, the mobility was increased from 5.7 cm²/Vs for $N_{\rm s} = 10^{12}$ cm⁻² to 13.9 cm²/Vs for $N_{\rm s} = 10^{13}$ cm⁻² at 300 K. The distinct temperature and $N_{\rm s}$ dependences of mobility caused by a phonon scattering and a roughness scattering in Si MOSFETs [10] were not observed. These characteristic temperature and $N_{\rm s}$ dependence was reported to be also observed in Hall mobility extracted by Hall measurements of InGaZnO film [7]. Assuming that the thickness of accumulation layer induced

by the gate voltage is around 1 nm, the range of carrier concentration (N_e) modulated by the gate voltage in this work corresponds to around 10¹⁹ cm⁻³ to 10²⁰ cm⁻³. In [7], Hall mobility of InGaZnO film was reported to decrease from ~10 cm²/Vs at $N_e = 3 \times 10^{20}$ cm⁻³ to ~4 cm²/Vs at $N_e = 2 \times 10^{19}$ cm⁻³ at 300 K. These extracted mobility values in InGaZnO MOSFET agree with Hall mobility values by Hall measurements of InGaZnO film.



FIGURE 3. (a) Arrhenius plot of temperature dependence of mobility at different N_s and (b) an illustration of trap-limited conduction model. At high temperature region (300 K~25 K), mobility follows a thermally activated behavior.

Figure 3 (a) shows Arrhenius plot of the temperature dependence of mobility at different N_s . At high temperature region (300 K~25 K), mobility follows a thermally activated behavior. The activation energy (E_a) extracted from 300 K to 25 K is 7 meV at low N_s (~ 10¹² cm⁻²) and decreases to be 2 meV at high N_s (~ 10¹³ cm⁻²). This N_s dependence of activation energy indicates that trap-limited conduction occurs dominantly at relatively high temperature region [7], [8]. As shown in Fig. 3 (b), potential fluctuations are formed around E_c and band transport occurs with help of thermal energy and Fermi energy modulation by gate voltage.

Figure 4 (a) shows temperature dependence of mobility displayed in terms of log μ - $T^{-1/4}$ plot. Mobility follows $T^{-1/4}$ law at low temperature region (< 25 K). This suggests that localized electrons at cations transport via overlapping of electron orbitals of In atoms by Mott's variable range hopping (VRH) conduction [11], [12] at low temperature, in which electrons cannot gain enough thermal energy to band transport ($k_BT < 2$ meV), as illustrated in Fig. 4 (b).

Therefore the temperature dependence of mobility with InGaZnO MOSFET was confirmed to follow a thermally activated behavior at high temperature region (300 K~25 K) and $T^{-1/4}$ law at low temperature region (< 25 K). This indicates that in InGaZnO MOSFET, trap-limited conduction is dominant at relatively high temperature region and variable range hopping conduction becomes dominant at low temperature region.

IV. ORIGIN OF HIGH MOBILITY IN INSNZNO MOSFETS

Figure 5 (a) shows a comparison of I_d - V_g characteristics between fabricated InSnZnO MOSFET and InGaZnO MOSFET. InSnZnO MOSFET showed higher on-current



FIGURE 4. Temperature dependence of mobility displayed in terms of log μ - $T^{-1/4}$ plot and (b) an illustration of Mott's variable range hopping conduction model. Mobility follows $T^{-1/4}$ rules at low temperature region (< 25 K), which suggests Mott's variable range hopping conduction.



FIGURE 5. (a) Comparison of I_d - V_g characteristics between InSnZnO and InGaZnO MOSFETs and (b) oxygen-bond dissociation energy [14]. InSnZnO MOSFET showed normally-off characteristics even without Ga atoms.

than InGaZnO. Also, InSnZnO MOSFET showed normallyoff characteristics even without Ga atoms. In general, it is considered that Ga atom plays an important role of suppressing V_0 formation to reduce intrinsic carrier concentration in InGaZnO film, which realizes an normally-off characteristics of InGaZnO MOSFET [13]. These results indicates that Sn atoms in InSnZnO could suppress V_0 formation, which may originate from large oxygen-bond dissociation energy as well as Ga atoms as shown in Fig. 5 (b) [14].

Figure 6 shows a comparison of mobility characteristics for different oxide semiconductor channel MOSFET at 300 K. Compared to mobility of InGaZnO MOSFET, In-rich InGaZnO and InSnZnO MOFSETs showed higher mobility. It was confirmed that mobility of InSnZnO MOSFET was about 26 cm²/Vs, almost 2 times higher than that of conventional InGaZnO.

In order to understand roles of each atom to mobility, temperature dependence with different oxide semiconductor MOSFETs were investigated. Figure 7 shows temperature dependence of I_d - V_g characteristics of (a) InSnZnO, (b) InSnGaO and (c) In-rich InGaZnO from 300 K to 10 K. All MOSFETs show normally-off characteristics and as well as conventional InGaZnO MOSFET shown in Fig. 2 (a), I_{on} decreases and *S.S.* became less steep with decreasing



FIGURE 6. Comparison of mobility characteristics for different oxide semiconductor channel MOSFET at 300 K. Mobility of InSnZnO MOSFET was about 26 cm²/Vs, almost 2 times higher than that of conventional InGaZnO.



FIGURE 7. Temperature dependence of I_d - V_g characteristics of (a) InSnZnO, (b) InSnGaO and (c) In-rich InGaZnO MOSFETs from 300 K to 10 K. All MOSFETs show normally-off characteristics.



FIGURE 8. (a) Comparison of N_s dependence of E_a of mobility with different oxide semiconductor channels and (b) illustrations of potential fluctuation at mobility edge of InSnZnO and InGaZnO. Although E_a with InSnZnO MOSFET becomes larger than that of InGaZnO MOSFET at low N_s ($\sim 10^{12}$ cm⁻²), it decreased to be 2 meV at high N_s ($\sim 10^{13}$ cm⁻²) as well as InGaZnO MOSFET.

temperature. Temperature dependences of mobility characteristics were extracted from Fig. 7. All mobility characteristics of InSnZnO, InSnGaO and In-rich InGaZnO were confirmed to change from a thermally activated behavior to $T^{-1/4}$ law as well as conventional InGaZnO MOSFET.

Figure 8 (a) shows a comparison of N_s dependence of E_a of mobility with different oxide semiconductor channels. The potential fluctuation around E_c of InSnZnO increases to be 12 meV at low N_s (~ 10¹² cm⁻²) while that of InGaZnO



FIGURE 9. Relationship between mobility at 300 K and E_a extracted from different oxide semiconductor channel MOSFETs. There was no clear correlation between mobility and E_a .



FIGURE 10. (a) N_s dependence of the coefficient *B* extracted at low temperature region (< 25 K) and (b) an illustration of relationship between coefficient B value and the degree of overlapping of localized states. The coefficient *B* value of InSnZnO MOSFET is smaller than that of InGaZnO MOSFET.



FIGURE 11. (a) Relationship between the coefficient *B* in Fig. 11 and mobility with different oxide semiconductor channels at 300 K, $N_{\rm s} = 10^{13}$ cm⁻² and (b) illustrations of overlapping of cation electrons. The strong correlation suggests that overlapping of cation electrons mainly dominates band transport in oxide semiconductor channel.

is 7 meV as shown in Fig. 8(b). However, regardless of oxide semiconductor channel composition, E_a are reduced to be 2 meV at high N_s (~ 10¹³ cm⁻²). Moreover, E_a of In-rich InGaZnO MOSFET behaves almost same as conventional InGaZnO MOSFET even at N_s low region, which indicates that potential fluctuations were almost independent on channel composition ratios.

In a hydrogenated amorphous Si (a-Si:H) film, potential fluctuation around E_c extracted from E_a of mobility was

around 60 meV and it was reported that there is a strong correlation between the degree of the potential fluctuation and the values of mobility of a-Si:H [11], [15]. Figure 9 show the relationship between mobility at 300 K and E_a extracted from different oxide semiconductor channel MOSFETs. In amorphous oxide semiconductors in this work, there was no clear correlation between mobility at 300 K and E_a at both low N_s and high N_s . Therefore it was confirmed that E_a analysis could not explain the cause for high mobility characteristics in InSnZnO MOSFET.

Figure 10 shows the N_s dependence of the coefficient *B* extracted at low temperature region (< 25 K). As shown in the inset of Fig. 4 where $k_{\rm B}$, $1/\alpha$ and $N(E_{\rm F})$ are Boltzmann's constant, the localization length and the density of states around $E_{\rm F}$, respectively. We extracted each coefficient B by fitting the slope of temperature dependence of mobility at low temperature region (< 25K) with $T^{-1/4}$ law. Since coefficient *B* indicates the degree of spatial/energy overlapping of localized state, the smaller coefficient *B* means the increase of overlapping of localized state. Among the investigated oxide semiconductors, coefficient *B* of InSnZnO MOSFET showed the smallest value for T < 25K. This suggests that the largest overlapping of electron orbitals at localized state was obtained by InSnZnO, as shown in Fig. 10 (b).

Figure 11 (a) shows the relationship between mobility at 300 K, $N_{\rm s} = 10^{13}$ cm⁻² and coefficient *B*. Compared with conventional InGaZnO, InSnZnO and In-rich InGaZnO with higher mobility showed smaller coefficient B. And coefficient B of InSnGaO was larger than that of InSnZnO. As shown here, it was confirmed that there was a strong correlation between mobility and coefficient *B*. Therefore, In oxide semiconductors, it is presumed that there is a mechanism in which increase of overlapping of electron orbitals formed by cations contributes to increase band transport in oxide semiconductor MOSFETs as shown in Fig. 11 (b).

We summarize roles of Sn atoms in InSnZnO. InSnZnO MOSFET realizes high mobility by enhancing the spatial overlapping of unoccupied electron orbitals, thanks to 5s orbital like In atoms, of Sn atoms different from Ga atoms. In addition, since Sn has large oxygen-bond dissociation energy [14], it could play a role of suppressing oxygen vacancy formation like Ga atoms as mentioned in Fig. 5. Therefore, Sn atoms contribute to the formation of electron orbitals with In atoms, while maintaining the effect of suppressing the formation of oxygen vacancy like Ga atoms.

V. CONCLUSION

Comprehensive analyses of temperature and $N_{\rm s}$ dependence of mobility revealed that the potential fluctuation around $E_{\rm c}$ of InSnZnO increases to be 12 meV at low $N_{\rm s}$ (~ 10¹² cm⁻²) while that of InGaZnO is 7 meV, but they decreased to be 2 meV at high $N_{\rm s}$ (~ 10¹³ cm⁻²). Incorporated Sn atoms were found to enhance the overlapping of electron orbitals of cations with In atoms, which results in mobility improvement.

REFERENCES

- K. Nomura *et al.*, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, pp. 488–492, Nov. 2004.
- [2] T. Aoki et al., "30.9 Normally-off computing with crystalline InGaZnO-based FPGA," in ISSCC Tech Dig., 2014, pp. 502–504.
- [3] Y. Kobayashi *et al.*, "Scaling to 50-nm C-axis aligned crystalline In-Ga-Zn oxide FET with surrounded channel structure and its application for less-than-5-nsec writing speed memory," in VLSI Symp. Tech. Dig., 2014, pp. 170–171.
- [4] K. Kaneko, N. Inoue, S. Saito, N. Furutake, and Y. Hayashi, "A novel BEOL transistor (BETr) with InGaZnO embedded in Cu-interconnects for on-chip high voltage I/Os in standard CMOS LSIs," in VLSI Symp. Tech. Dig., 2011, pp. 120–121.
- [5] K. Ota *et al.*, "Silicon-compatible low resistance S/D technologies for high-performance top-gate self-aligned InGaZnO TFTs with UTBB (ultra-thin body and BOX) structures," in *VLSI Symp. Tech. Dig.*, 2015, pp. 214–215.
- [6] S. Tomai *et al.*, "High-performance thin film transistor with amorphous In₂O₃-SnO₂-ZnO channel layer," *Jpn. J. Appl. Phys.*, vol. 51, Mar. 2012, Art. no. 03CB01.
- [7] K. Nomura *et al.*, "Carrier transport in transparent oxide semiconductor with intrinsic structural randomness probed using single-crystalline InGaO₃(ZnO)₅ films," *Appl. Phys. Lett.*, vol. 85, no. 11, p. 1993, 2004.
- [8] T. Kamiya, K. Nomura, and H. Hosono, "Electronic structures above mobility edges in crystalline and amorphous In-Ga-Zn-O: Percolation conduction examined by analytical model," *J. Display Technol.*, vol. 5, no. 12, pp. 462–467, 2009.
- [9] A. Takagi et al., "Carrier transport and electronic structure in amorphous oxide semiconductor, a-InGaZnO₄," *Thin Solid Films*, vol. 486, nos. 1–2, pp. 38–41, 2005.
- [10] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of inversion layer mobility in Si MOSFET's: Part I—Effects of substrate impurity concentration," *IEEE Trans. Electron Devices*, vol. 41, no. 12, pp. 2357–2362, Dec. 1994.
- [11] A. Nagy, M. Hundhausen, L. Ley, G. Brunst, and E. Holzenkämpfer, "Steady-state hopping conduction in the conduction-band tail of a-Si:H studied in thin-film transistors," *Phys. Rev. B, Condens. Matter*, vol. 52, no. 15, pp. 11289–11295, 1995.
- [12] W. C. Germs et al., "Charge transport in amorphous InGaZnO thinfilm transistors," Phys. Rev. B, Condens. Matter, vol. 86, Oct. 2012, Art. no. 155319.
- [13] T. Iwasaki *et al.*, "Combinatorial approach to thin-film transistors using multicomponent semiconductor channels: An application to amorphous oxide semiconductors in In-Ga-Zn-O system," *Appl. Phys. Lett.*, vol. 90, no. 24, 2007, Art. no. 232114.
- [14] Y. R. Luo, "Bond dissociation energies," in CRC Handbook of Chemistry and Physics, 90th ed. Boca Raton, FL, USA: CRC Press, 2009, pp. 9–65.
- [15] S. Sherman and S. Wagner, "Relationship between a-Si:H band tails and TFT performance," in *Proc. AMLCDs*, 1995, pp. 42–45.



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