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Ultra-High-Efficiency Writing in Voltage-Control Spintronics Memory (VoCSM): The Most Promising Embedded Memory for Deep Learning

Y. OHSAWA [1], H. YODA [1], N. SHIMOMURA [1], S. SHIROTORI [1], S. FUJITA [1], K. KOI [1], A. BUYANDALAI [1], S. OIKAWA [1], M. SHIMIZU [1], Y. KATO [1], T. INOKUCHI [1], H. SUGIYAMA [1], M. ISHIKAWA [2], K. IKEGAMI [1], S. TAKAYA [1], AND A. KUROBE [1]

1 Corporate Research and Development Center, Toshiba Corporation, Kawasaki 212-8582, Japan
2 Department of Systems Innovation, Graduate School of Engineering Science, Osaka University, Toyonaka 560-8531, Japan

CORRESPONDING AUTHOR: Y. OHSAWA (e-mail: yuichi.osawa@toshiba.co.jp)

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ABSTRACT Our new proposal of voltage-control spintronics memory (VoCSM) in which spin-orbit torque in conjunction with the voltage-control-magnetic-anisotropy effect works as the writing principle showed small switching current of 37 μA for about 350 K_BT switching energy. This indicates VoCSM's writing efficiency is so high that VoCSM would be applicable for deep learning memories requiring ultra-low power consumption.

INDEX TERMS Magnetic memory, nonvolatile memory, magnetic tunneling, magnetic devices, learning (artificial intelligence), Nanopatterning.

I. INTRODUCTION

Since logic chips for deep learning (DL) such as Graphics Processing Unit (GPU), Field-Programmable Gate Array (FPGA) or DL-specific-System-on-a-Chip (SoC) certainly require high-memory bandwidth, current DL-chips use TSV-based solutions (TS) with interposers and 3D-stacked DRAM. However, in the case of TS, the cost performance of TS is a severe issue, since integration cost is high and bandwidth is limited because of the number of TSVs. The ideal memory solution is "ultra-high density embedded memory." Although embedded Spin Transfer Torque MRAM (eSTT-MRAM), which would replace eSRAM with 4x higher density, had been considered the ideal candidate, switching current (Ic) and endurance of STT-MRAM is severely degraded as the write time is shorter for DL memory (<20ns) [1]. VoCSMs have been proposed as a new MRAM concept to break the STT-MRAM impasse and demonstrated their unique writing concepts and their features such as the possibility of ultra-low power consumption [2], high-speed writing [3], read-disturb robustness and unlimited endurance [3], [4]. One of the features of VoCSM is ultra-high efficiency in writing. However, the envisaged capabilities of VoCSM remain unproven owing to the immaturity of the technologies.

In this study, the ultra-high efficiency in writing was demonstrated for the first time by developing self-aligned cell structure and the ultra-precise fabrication process to show the potential for a memory solution for DL logic chips. The planar and cross-sectional structure of the self-aligned cell were explained using electron microscopic images. Patterning damage at the MTJ edge introduced by the newly developed process was compared with that by the conventional process. Furthermore, the prospect of further reduction of power consumption and the comparison with embedded (e)DRAM / eSRAM about application possibility as a memory for DL of VoCSM were performed.

II. THE VOCSM CELL, MATERIAL, STRUCTURE, AND PROPERTIES

A. MATERIALS

The MTJ film mainly used had the structure of (from bottom) Ta (2)/TaB (3) / FeB (2.1-2.2) / MgO (1.8)/CoFeB (1.8)/Ru (0.9)/CoFe (1.8)/IrMn (8.0)/Ta (5.0)

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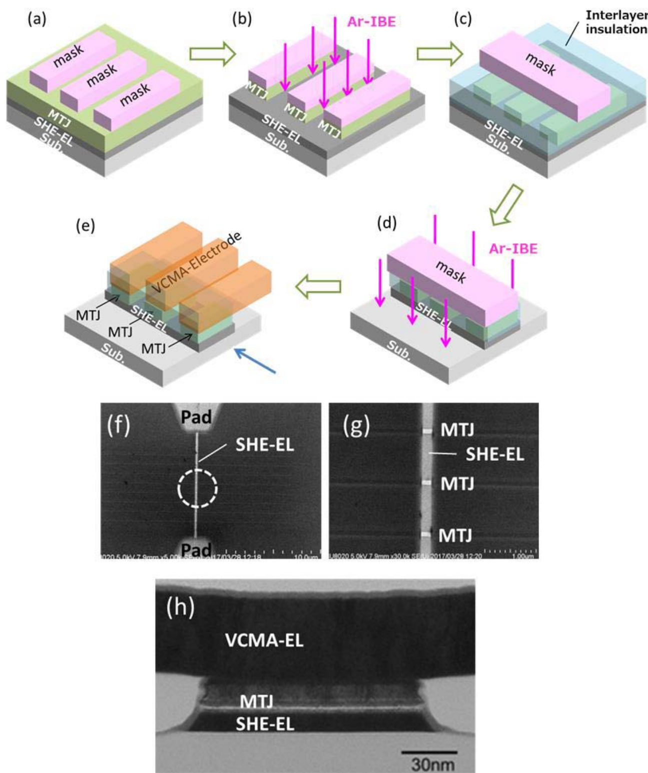

FIGURE 1. Schematic drawings of the TSSA process. (a) First mask patterning, (b) 1st ion-beam etching (IBE) of MTJ. Etching stops on the SHE electrode surface, (c) 2nd mask patterning, (d) 2nd IBE of MTJ. The SHE electrode is patterned into stripe configuration. (e) Top (VCMA) electrodes are connected on MTJ cells on the same SHE electrode stripe. (f) Plane-view SEM image of the device before top (VCMA) electrode patterning. SHE electrode connects the two pads. (g) Expanded image of dashed-circle area in (f). Three rectangular MTJs are patterned on the SHE electrode. (h) Cross-sectional TEM image of MTJ / SHE-electrode region observed from the arrow in (e).

[nm] fabricated using an ultra-high-vacuum magnetron sputtering machine at room temperature. The films were then annealed at 300°C for 1 h for pinning. Saturation magnetization (M_s) and dead-layer thickness are 1076 emu/cc and 0.003 nm, respectively. The 3 nm-TaB layer is inserted between the FeB storage layer (SL) and the Ta layer to reduce dead-layer thickness in the SL [5].

B. STRUCTURE AND PROCESS

B.1. CELL STRUCTURE

The cell configuration is designed to reduce I_c compared with that of the conventional structure used in our previous demonstrations [2], [3]. We developed two key fabrication processes as described below.

A two-step self-alignment (TSSA) fabrication and device image are shown in Fig. 1. Schematic drawings of the TSSA process are shown in (a)-(e). MTJs are patterned by orthogonally crossed stripes. This process can make MTJs and the spin Hall effect (SHE) electrode have the same width, which contributes to decrease in I_c [6]. I_c is defined as the switching current whose writing probability is 50%. Plane-view SEM images of the device before top (VCMA) electrode patterning (f)(g), and cross-sectional transmission electron microscopy (XTEM) image of MTJ / SHE-electrode region (h) show MTJ and SHE electrode have the same size.

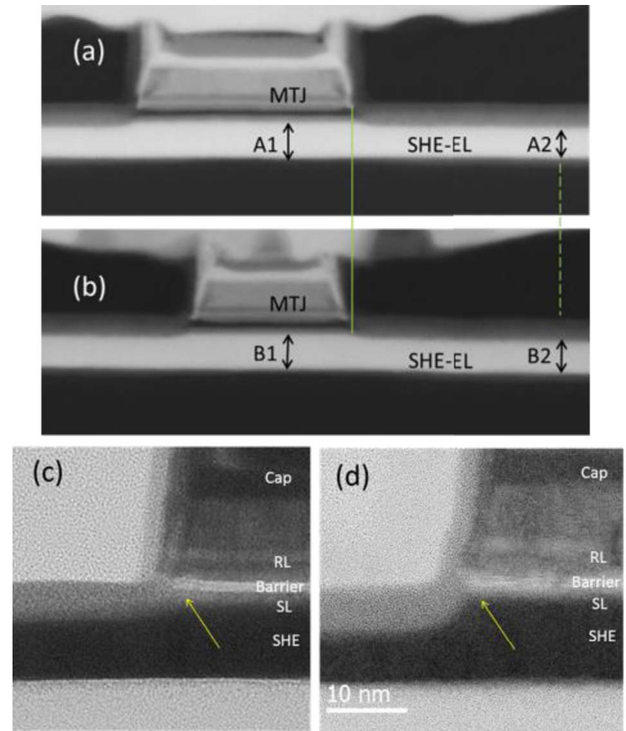

FIGURE 2. Cross-sectional images of the MTJ on SHE electrode. High-angle annular dark field scanning TEM images of the conventional process (a).

B.2. ETCHING PROCESS

We developed a new MTJ-patterning process for ultra-thin SHE electrode that is based on highly selective etching (HSE) of a storage layer (SL) on a Ta-SHE electrode. A comparison of the conventional etching process and the newly developed HSE process is shown in Fig. 2. Cross-sectional transmission electron microscopy (XTEM) images of high-angle annular dark field (HAADF) fabricated by the two processes are shown. In the case of the conventional process (a), thickness of the Ta-SHE electrode under MTJ (position A1) is 10 nm and thickness at the MTJ etched area indicated as A2 is 6.8 nm. On the other hand, in the case of the HSE process (b), thickness of the Ta-SHE electrode under MTJ (position B1) is 10 nm and thicknesses at the MTJ etched area (position A2) is 8.9 nm. It means only about 1 nm-over-etching is performed in the case of the HSE process.

Bright field XTEM images of patterning edges etched by the conventional process and the HSE process are shown in Fig. 2 (c) and (d), respectively. The conventional process introduces several nm-depth damaged regions at the SO layer and the SL layer, whereas there is little damaged depth in the case of the HSE process. The damaged regions are indicated by arrows. However ion-beam etching on MTJs or magnetic films introduces many kinds of damage [7]–[9]. Therefore some patterning damage could be included at the MTJ edge even in the case of the HSE process.

C. PROPERTIES

I_c as a function of MTJ size under a 20 ns-width write pulse is shown in Fig. 3. I_c decreases linearly as MTJ size decreases. A device with I_c of about 50 μA is obtained whose MTJ size is about 5000 nm^2 (= 50 × 100 nm). The I_cs are much smaller than those in our previous report [6] for which the conventional process was used.

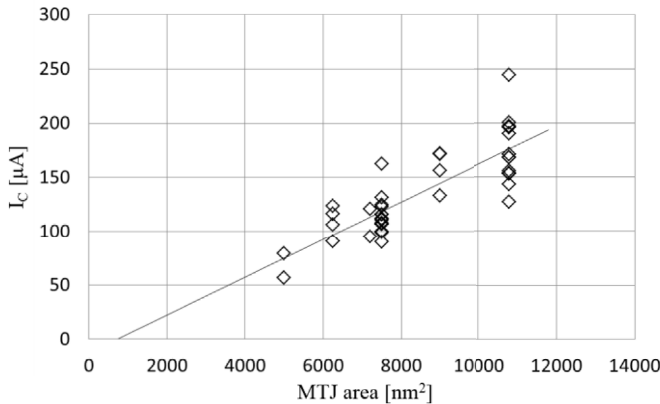

FIGURE 3. I_c **as a function of MTJ area. MTJ area is estimated from CAD design. The line is a linear approximation fit.**

The effect of reduction in SHE electrode thickness is shown in Fig. 4. I_c comparison between SHE electrode thickness of 8 nm (circles) and 5 nm (triangles) with resistance of about 110 kΩ is shown. SHE electrodes are composed of (from bottom) Ta 5nm/ TaB 3nm (◯) and Ta 2nm / TaB 3nm (△), respectively. SL is FeB 2.2 nm in both cases. Designed MTJ size is 50 × 150 nm in both cases. Because of size and RA distribution, thinner SHE samples show about 10% smaller resistance. Samples of thinner SHE electrode (△) show about half the I_c of those of thicker SHE electrode (◯). Therefore, the HSE process capable of fabricating MTJ cells with ultra-thin SHE electrode would have great potential for reducing write current.

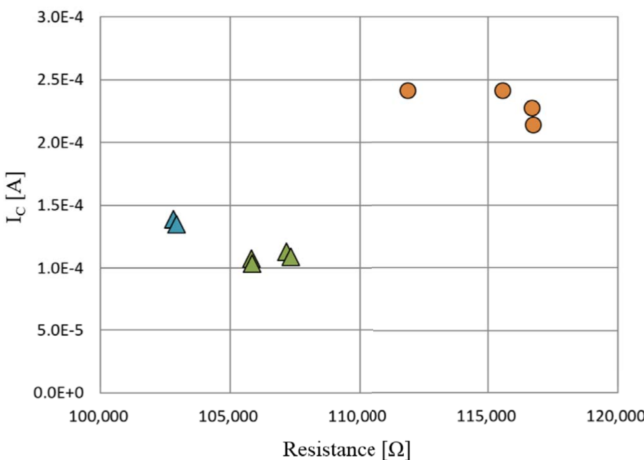

FIGURE 4. I_c **comparison between 8 nm(◦)- and 5 nm(△)-SHE electrode (total thickness).**

III. WRITE TESTS AND THE RESULTS

A. DEPENDENCE OF CRITICAL CURRENT ON FEATURE SIZE

Dependence of I_c on feature size (W_F) for various combinations of SL and SHE electrode is shown in Fig. 5. Combinations of the SHE electrode / SL (thickness in nm) are A: Ta10/FeB 1.9, B: Ta 10/CoFeB 1.2, and C: Ta 10/TaB 3/ FeB 1.9, respectively. The lines A, B, and C are second-order polynomial (SOP) approximate lines crossing the origin for each data group since I_c dependence on MTJ size in perpendicular (p) - STT MTJs is well plotted on the SOP approximate line empirically. The SOP approximate lines are a good fit with the data groups of VoCSMs as functions of W_F.

I_c dependence on W_F of VoCSM without MTJ bias and p-STT MTJs (in house) is shown in Fig. 6. An aspect ratio defined as SL length (L_F)/ feature size (W_F) of the SL is used as a parameter (see Fig. 5 inset). W_F for the p-STT MTJs is diameter of the SL. The lines are SOP approximation. I_c decreases as the aspect ratio decreases since I_cs are directly dependent on SL length (L_F). I_c as a function of bias voltage (V_b) of the VoCSM cell, indicated by the arrow in Fig. 6, is shown in Fig. 7. Negative bias at the top electrode decreases the I_c whose slope of the linear fit is about 18 μA / V. The I_c value showed as small as 37 μA under V_b of −0.8 V. The size of the SL in the cell is estimated as W_F 53 × L_F 118 nm, respectively.

I_c comparison between p-STT MTJs and VoCSM is shown in Fig. 8. The data points of VoCSM are V_b of −0.8 V. The dashed line indicates CMOS current availability with an assumption of 1 mA/μm, which means the write current limitation. The lines for the p-STT MTJs and the VoCSM are SOP approximation. It can be seen that the p-STT MTJs encounter the CMOS current limitation wall, whereas VoCSM has smaller I_c at the same W_F and would have potential for CMOS current-drive limitation owing to high write efficiency of SOT writing under the VCMA effect.

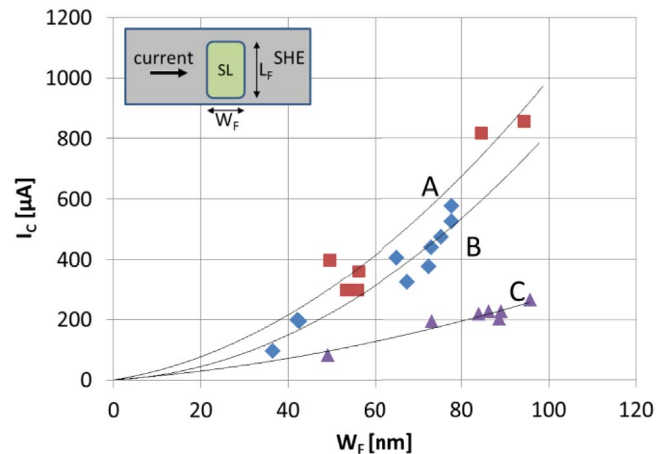

FIGURE 5. Empirical fits for I_c**s dependence on feature size. The inset shows feature size (**W_F**) and SL length (**L_F**).**

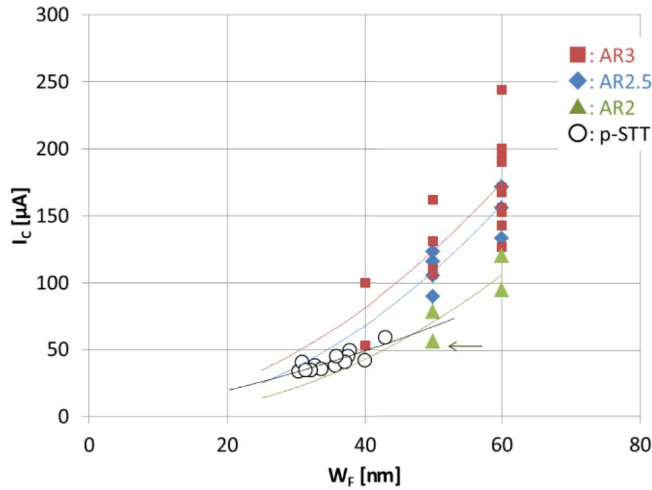

FIGURE 6. Effect of VCMA on I_c. The inset shows resistance-current (*R-I*) curves at each bias voltage. The line is a linear approximation fit. Negative bias at the top electrode decreases the I_c.

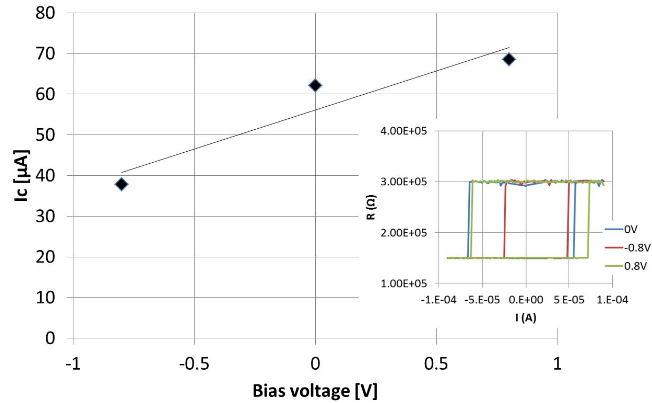

FIGURE 7. Effect of VCMA on I_c. The inset shows resistance-current (*R-I*) curves at each bias voltage. The line is a linear approximation fit. Negative bias at the top electrode decreases the I_c.

B. WRITE EFFICIENCY

We define the write efficiency η as $\eta = \Delta E_{sw}/I_c$, where ΔE_{sw} is a switching energy of SL described as $\Delta E_{sw} = M_S t H_{Keff}/4\ k_B$T, where M_S: saturation magnetization of the SL, t: thickness of the SL, H_{Keff}: anisotropic field in the SL perpendicular to the film plane (perpendicular magnetic anisotropy), k_B : Boltzmann constant, and T: temperature. H_{Keff} and ΔE_{sw} of the cell indicated by the arrow in Fig. 8 are estimated as 3.3 kOe and 350 k_BT, respectively. Therefore, η is about 9.5 k_BT / μA under V_b of -0.8 V; $\eta = 350\ k_B$T/37 μA, which is the writing efficiency of SOT with the VCMA effect. Even in the case of Vb = 0V, η is about 6.6 k_BT/μA; $\eta = 350\ k_B$T/53 μA, which is high efficiency of only SOT without the VCMA effect. Whereas, in the case of p-STT writing whose ΔE_{sw} is equal to a retention energy $\sim 40\ k_B$T, η is about 1. Therefore, η of SOT writing is much larger than that of STT writing; besides the VCMA effect increases η further. However, ΔE_{SW} would vary from 225 (60%) to 700 (200%) k_BT compared with the stated value of 350 k$_B$T owing to variation of H_{Keff} estimation in the MTJ cell.

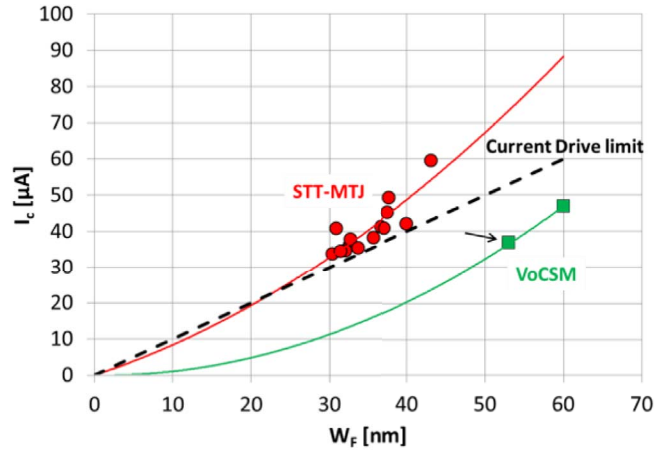

FIGURE 8. I_c comparison between VoCSM (■) and p-STT MTJs (●). Lines for p-STT MTJ and VoCSM are SOP fits. I_c of the data point indicated by the arrow is 37μA. That corresponds to the critical current density of about 3.2 MA/cm^2, assuming SHE electrode and SL have the same conductivity.

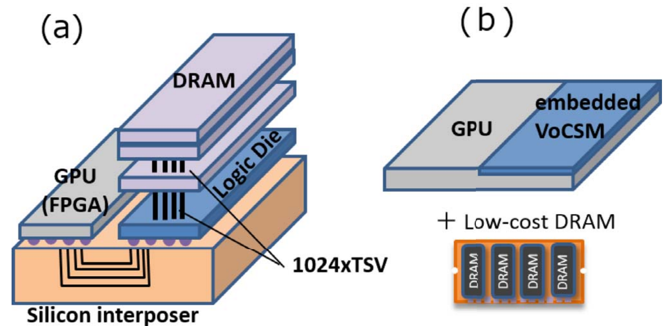

FIGURE 9. Illustrations of deep learning SoC chips with high-density and high-bandwidth memories.

C. FURTHER DECREASE IN POWER CONSUMPTION

The values of θ_{SH} and VCMA coefficient of the samples used in the write tests are about 0.18 and 70 fJ/Vm, respectively. Write current can be decreased by increasing θ_{SH} and/or VCMA coefficient [2]. As for the θ_{SH}, about 0.3 for W [10] and in the case of topological insulator 2.0-3.5 for Bi-Se [12] have been reported. As for the VCMA coefficient, the state-of-the-art coefficient of about 300 fJ/Vm has been reported [11]. Furthermore, giant VCMA coefficient of about 1800 has been calculated [13] and about 1000 has been observed in highly strained Fe-Co systems recently [14]. Therefore, VoCSM has tremendous potential for reducing power consumption, and the introduction of tailored strain into the VoCSM device is expected to be one of the important engineering techniques.

IV. VOCSM FOR DL LOGIC CHIP APPLICATION

Although GPU or FPGA for DL applications needs embedded giga (G) bit memory with extremely high memory bandwidth (HMB), SRAM is unavailable owing to huge overhead of area and standby power. Therefore, high-cost HBM

TABLE 1. Comparison of memory solutions for DL logic chips. Data on VoCSM are based on circuit simulations and layout design.

	Memory Bandwidth	Power (a.u.)	e Memory Capacity of SoC CMOS (the same area for eSRAM)	Latency between SoC/memory (including bus)
eSRAM (reference)	☺Several TB/s	1	☹<512 Mb (~300f²)	☺20~30ns
(a) High-cost (TSV/3D)	512G (on HBM2)	>1.3	-	☹~50ns
(b) Low-cost (VoCSM)	☺Several TB/s	☺0.4	☺2.5 Gb (60f²)	☺20~30ns
(b') with eDRAM	☺Several TB/s	☹>5	☺2.5~3 Gb (50~60f²)	☺20~30ns

(3D-stacked DRAM with TSV) and TSV-based silicon interposer are currently used instead of eSRAM. e-STT-MRAM cannot be a candidate since endurance is greatly reduced to less than 1×10^7 as write pulse time decreases to less than 20 ns [1].

VoCSM with practically unlimited endurance even with a 5 ns-write time has been reported [3]. Also, VoCSM read time operation using VCMA-MTJ is reported to be 10 to 20 ns for high-density embedded memory. Considering these reports and the results presented in this paper, it has been confirmed that VoCSM is applicable to low-cost embedded Gbit memory for DL logic chips. Table 1 shows a comparison of memory solutions for DL logic chips. Smaller area (higher density), higher access speed and lower power of VoCSM are indicated compared with other memory solutions. VoCSM is applicable to low-cost embedded Gbit memory for DL logic chips, as illustrated in Fig. 9.

V. CONCLUSION

We proved the ultra-high-efficiency writing in VoCSM in which SOT in conjunction with the VCMA effect works as the writing principle. We found I_C decreases with second-order polynomials in accordance with the reduction in feature size, and write current is about 40 μA, which would be much smaller than that of p-STT MTJs with the same switching energy and the same size. Due to the proved high efficiency in writing, VoCSM is thought to be the most suitable solution for DL memories.

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Y. OHSAWA received the B.S., M.S., and Ph.D. degrees from the Department of Electrical Engineering and Electronics, Aoyama Gakuin University, Tokyo, Japan, in 1983, 1985, and 2009, respectively. He joined Toshiba Corporation, Kawasaki, Japan, in 1985, where he has been engaged of magnetic devices, such as VCR magnetic heads, giant-MR sensor, nanocontact-MR sensor, HDD write heads, and MRAMs. From 2002 to 2011, he also joined as a Research Fellow with the Research Institute of Electrical Communication, Tohoku University, Sendai, Japan. He was a recipient of the Imperial Invention Prize in National Commendation for Invention from the Japan Institute of Invention and Innovation in 2001.

H. YODA received the Master of Science degree in electrical engineering from Washington University, St. Louis. He had worked on HDD heads from 1991 to 1999. Since 2000, he had led MRAM project in Toshiba. He is currently a Principal Investigator of Japanese Government Project, ImPACT Program, and a Senior Fellow of the Research and Development Center, Toshiba Corporation. He was a recipient of the Nikkei BP Grand Award on GMR Heads in 1996, the Kanto Invention Award on HDD Read and Write Heads in 2005, the Ichimura Industrial Award on HDD Read and Write Heads in 2005, and the Japan National Invention Award on HDD Read and Write Heads in 2007.

N. SHIMOMURA received the bachelor’s, master’s, and Ph.D. degrees in physics from Tokyo University, Japan, in 1990, 1993, and 1996, respectively. He was a Research Scientist with Toshiba Corporation. His research includes an MTJ cell and memory design of MRAM. He is currently working for voltage control spintronics memory.

S. SHIROTORI received the B.S., M.S., and Ph.D. degrees in applied physics from Tohoku University, Sendai, Japan, in 2001, 2003, and 2015, respectively. He joined the Research and Development Center, Toshiba Corporation, Kawasaki, Japan, in 2003. He has been engaged in the research of storage and memory of magnetic devices.

S. FUJITA received the Ph.D. degree from the University of Tokyo and joined Toshiba Corporation in 1989. He has been working for new nonvolatile memory (NVM) circuit and system designs for over 15 years. His major designs are ReRAM-based NV-logics, ReRAM-based-FPGA, NVM-based random number generators, NV-SRAM-based cache memories, and normally-off processors with e-STT-MRAM used from cloud computing to IoT/wearables. He is currently a Senior Fellow of the Research and Development Center, Toshiba Corporation, and leading a Project for NVM circuit and systems for energy efficient computing with advanced voltage-control-MRAM.

K. KOI received the Ph.D. degree from the University of Tokyo and joined Toshiba Corporation in 1997. He worked for HDD technologies, such as GMR Head, and Microwave-Assisted Magnetic Recording for 19 years. In 2016, he joined MRAM Project and has been engaged in magnetic design of MTJ element. He is currently a Chief Research Scientist of the Research and Development Center, Toshiba Corporation.

A. BUYANDALAI was born in Ulaanbaatar, Mongolia. She received the Bachelor of Science degree in materials science and engineering from the Toyohashi University of Technology in 2013 and the Master of Science degree from the University of Toyohashi in 2015. She is a Research Engineer with the Research and Development Center, Toshiba Corporation. She was assigned to the ImPACT project, and currently working as a nano process expert of MRAM.

S. OIKAWA received the Dr.Eng. degree in electronics from Nagoya University, Nagoya, Japan, in 1998. He joined the Hard Disk Drive Development Department and the Research and Development Center, Toshiba Corporation, Kawasaki, Japan, in 1998 and 2016, respectively. He has been engaged in the research of materials and magnetic properties of thin films.

M. SHIMIZU received the B.S. and M.S. degrees in applied physics from the University of Tokyo, Tokyo, Japan, in 2004 and 2006, respectively. She joined the Research and Development Center, Toshiba Corporation, Kawasaki, Japan, in 2006. She has been engaged in the development of material and micro-fabrication process for magnetic devices in HDD and spintronics memory.

Y. KATO received the Ph.D. degree from the Tokyo Institute of Technology and joined Toshiba Corporation in 2011. He has been working for new spintronics materials used for MRAM.

T. INOKUCHI received the B.S., M.S., and Ph.D. degrees in applied physics from the University of Tokyo, Tokyo, Japan, in 1999, 2001, and 2004, respectively. He joined the Research and Development Center, Toshiba Corporation, Kawasaki, Japan, in 2004. He has been engaged in the research of spintronics-based emerging devices.

H. SUGIYAMA received the B.Eng. degree in applied physics and the M.Eng. and D.Eng. degrees in quantum engineering from Nagoya University, Nagoya, Japan, in 1993, 1995, and 1998, respectively. He joined the Research and Development Center, Toshiba Corporation, Kawasaki, Japan, in 1998. He has been engaged in the research of superconducting devices and magnetic devices.

M. ISHIKAWA received the B.S. degree in physics from Nihon University in 2004 and the M.S. degree in engineering science from Osaka University, Japan, in 2006, where she is currently pursuing the Ph.D. degree, focusing on spin-transport in Si. She was with the Research and Development Center, Toshiba Corporation, Japan, from 2006 to 2018.

K. IKEGAMI received the B.S. degree in physics and the M.S. degree in advanced materials science from the University of Tokyo, Tokyo, Japan, in 2004 and 2006, respectively. He joined the Research and Development Center, Toshiba Corporation, Kawasaki, Japan, in 2006. He has been engaged in the research of circuit and system technology of emerging devices.

S. TAKAYA received the B.E., M.E., and Ph.D. degrees in engineering from Kobe University, Kobe, Japan, in 2009, 2011, and 2014, respectively. He joined Toshiba Corporation in 2014.

A. KUROBE received the B.S. and Ph.D. degrees in physics from the University of Tokyo, Tokyo, Japan in 1979 and 1984, respectively. From 1991 to 1995, he was a Visiting Scholar with the Cavendish Laboratory, University of Cambridge, U.K., researching on the quantum transport in low dimensional semiconductor devices. From 2010 to 2013, he was the Director of the Center for Semiconductor Research and Development, Toshiba Corporation, where he is currently a Chief Fellow. His scientific interests include wide range of novel semiconductor devices and materials.