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P-Channel and N-Channel Super-Steep Subthreshold Slope PN-Body Tied SOI-FET for Ultralow Power CMOS

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ABSTRACT In this paper, *n*-channel and *p*-channel super-steep subthreshold slope (SS) PN-body tied (PNBT) silicon on insulator field-effect transistors (SOI-FETs) are demonstrated. The PNBT structure has a symmetrical source and drain structure. The devices show super-steep SS ($<$ 1 mV/dec) characteristics while maintaining low off current ($<$ 1 pA/μm) and high on/off ratio (up to 6 decades) with low drain voltage ($V_d = \pm$ 0.1 V), good output characteristics, and threshold voltage controllability. The devices have a body current and a hysteresis characteristic; however, these can be suppressed under proper device conditions. The operation mechanism of the PNBT SOI-FET is clarified by simulation, and an inherent thyristor on the PNBT structure plays a significant role. Both the *p*-channel and *n*-channel PNBT SOI-FET characteristics are discussed, and it is indicated that an ultralow power complementary metal-oxide-semiconductor can be realized by the PNBT SOI-FET.

INDEX TERMS Body tied, feedback, floating body, SOI MOSFET, steep subthreshold slope, thyristor.

I. INTRODUCTION

Ultralow power devices for micro and nanowatt electronics, such as the Internet of Things and medical applications, are one of the frontier research themes for large scale integration (LSI) [1]. To achieve ultralow power LSI, low power-supply voltages (V_{DD}) and off currents I_{off} are required. To that end, it is necessary to reduce the subthreshold slope (SS) of the metal-oxide semiconductor field-effect transistors (MOSFETs). Recently, steep SS devices to overcome the fundamental lower limit of the conventional MOSFET's SS ($\approx$ 60 mV/dec) at room temperature have been studied. In particular, tunnel field-effect transistors (FETs) [2], [3] and negative capacitance FETs [4], [5] have been reported as mainstream research. These devices have achieved a steep SS ($<$ 60 mV/dec), maintaining low I_{off} in the simulation results; however, actual fabricated devices have not yet achieved these ideal characteristics. Other devices, such as impact ionization metal-oxide semiconductors (I-MOSs) [6], ultra-thin buried-oxide (Box) fully depleted (FD)-silicon on insulator (SOI) [7], microelectromechanical (MEM) logic switches [8], feedback FETs (FBFETs) [9], and resistive-gate FETs (ReFETs) [10] have been proposed. Those devices have realized a steeper SS ($<$ 10 mV/dec). However, they also exhibit some issues, for example, I-MOSs require a high drain voltage (V_d) because they require avalanche breakdown. The ultra-thin Box FD-SOI uses floating body effects and can operate at lower V_d than the I-MOSs. However, the device operates over $V_d = 1.0$ V because it uses impact ionization. MEM logic switches implement ideal switching by using mechanical contact, but also have significant hysteresis characteristics. Additionally, they have a problem with repeatability because of mechanical strength problems. FBFETs use potential modulation by charging carriers to the sidewall; thus, they also have hysteresis characteristics. ReFETs use a gate with resistive switching. The key issue of ReFETs is to develop feasible materials. Moreover, some of the steep SS devices have an asymmetric source and drain (S/D) structure.

As an alternative, we have proposed the n-channel super-steep SS PN-body tied (PNBT) SOI-FET [11]–[14]. The

PNBT SOI-FET realizes a super-steep SS (< 1 mV/dec) while maintaining a low I_{off} (< 1 pA/μm) with a low V_d (= 0.1 V). It also has a symmetrical S/D structure.

In this study, first, the operation mechanism of the PNBT SOI-FET is clarified by using technology computer-aided design (TCAD). Second, we demonstrate the actual measurement results of the super-steep SS PNBT SOI-FET. Specifically, for the first time, the p-channel super-steep SS PNBT SOI-FET is reported. We found that substrate bias (V_{sub}) is necessary to reduce I_{off}. We also discuss the possibility of an ultralow power complementary metal-oxide-semiconductor (CMOS) with the PNBT SOI-FET, based on the results.

II. DEVICE STRUCTURE OF PNBT SOI-FET

Fig. 1 shows the device structure of the PNBT SOI-FET. It is a conventional body-tied SOI-FET with an n (or p)-region inserted between a p^+ (or n^+) contact region and a channel region. The polarity is changed between the p-channel and n-channel PNBT SOI-FET as shown in Figs. 1(a) and 1(b). The front view and top view are shown in Figs. 1(c) and 1(d). The impurity concentration of the n (or p) region was set to be lightly doped to reduce the operating body voltage (V_b) below 1.0 V, as we reported in our previous study [12]. The actual devices were fabricated using a 0.2-μm SOI CMOS process with a 50-nm-thick SOI (T_{Si}), a 200-nm Box (T_{Box}), a 4.4-nm-thick gate oxide (T_{ox}), 0.2/1 μm gate length (L_g), and 1 μm gate width (W_g). In this study, the gate has a T-shape and the n (or p)-region width (W_b) was set to be 1.2 μm, to maintain the overlay accuracy, according to the layout rules of the process that we used [13]. The PNBT structure consists of a pnpn junction between the S/D and the body terminal; therefore, it has an inherent thyristor as shown in Fig. 1(e). This inherent thyristor plays a significant role in the appearance of the super-steep SS.

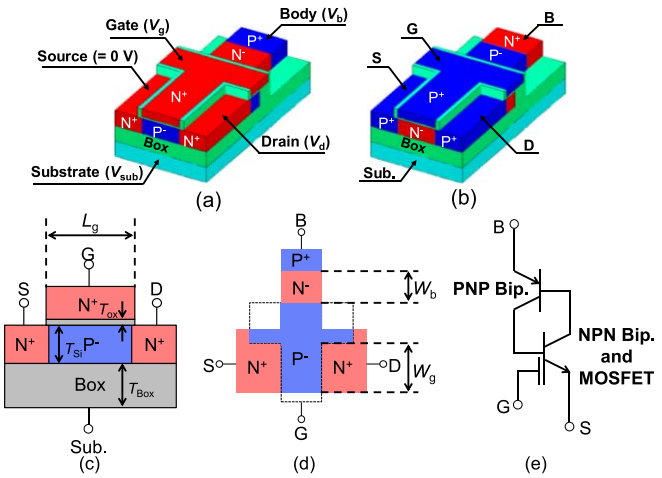

FIGURE 1. Device structure of PNBT SOI-FET. (a) n-channel PNBT SOI-FET, (b) p-channel PNBT SOI-FET, (c) front view, (d) top view, (e) inherent thyristor.

III. SIMULATION RESULTS AND OPERATION MECHANISM

We clarified the operation mechanism of the PNBT SOI-FET with 3D device simulation using TCAD "HyENEXSS" [15]. We used the Shockley–Read–Hall recombination, trap-assisted tunneling, auger recombination, and band-to-band tunneling model. However, the impact ionization model was not enabled. Fig. 2 shows the simulated drain current I_d and the body current I_b vs the gate voltage V_g, and the characteristics of the p-channel and n-channel PNBT SOI-FETs at $V_d = \pm 0.1$ V and $V_b = \pm 0.8$ V. Super-steep SS characteristics appear in both devices when $-0.1\ V < V_g < 0.1$ V. This indicates that the PNBT SOI-FET will allow the CMOS to operate at $V_{DD} = 0.1$ V. Additionally, power consumption by I_b will not be an issue when considering $P = I \times V$, as I_b is one-tenth lower than I_d, although V_b is higher than V_d. However, when the CMOS configuration is considered, I_b flows from the body terminal to the ground (or power supply) terminal in the CMOS inverter with the PNBT SOI-FET and cannot be blocked at the steady state, as mentioned in [16]. This increases the power consumption in the CMOS inverter operation. We thus need to further reduce I_b or design a circuit to solve this critical issue.

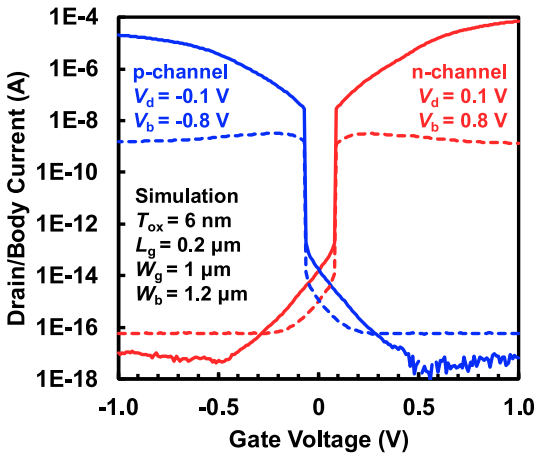

FIGURE 2. Simulated I_d and I_b–V_g characteristics of the p-channel and n-channel PNBT SOI-FETs. Solid line: I_d, dotted line: I_b.

Fig. 3 shows the hole concentration in the n-channel PNBT SOI-FET at the off state and on state as the super-steep SS appears. Only the n-channel case was considered here because both the p-channel and n-channel have the same mechanism. In the off state, holes accumulate in the neutral region under the gate. However, for the on state, the holes fill the entire SOI region. This phenomenon seems to be the floating body effect in the SOI MOSFET [7]. Conventional floating body effects are induced by the carrier charging due to impact ionization; however, it should be noted that this simulation does not use the impact ionization model. Therefore, the holes are provided by a method other than impact ionization. It is considered that the holes are provided by the positive feedback from the inherent thyristor on our

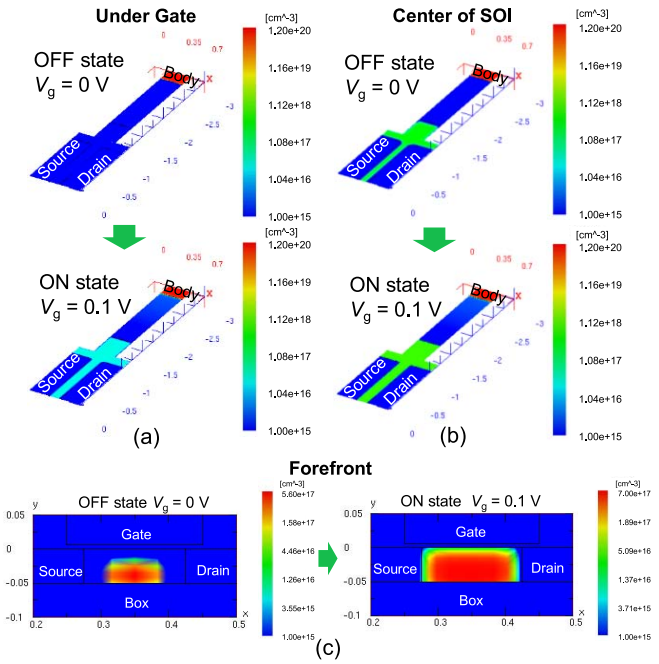

FIGURE 3. Hole concentration in the n-channel PNBT SOI-FET at (a) under the gate, (b) center of SOI, and (c) forefront.

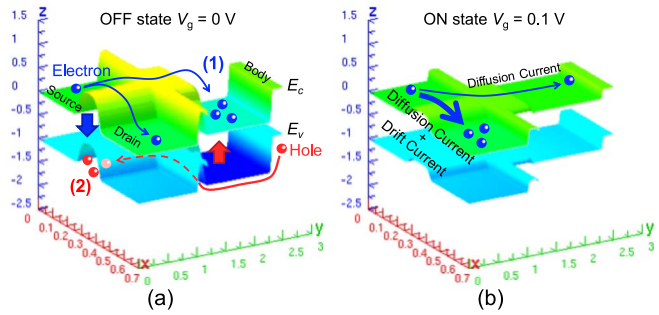

FIGURE 4. Band diagrams in the n-channel PNBT SOI-FET under the gate at the (a) off state and (b) on state as the super-steep SS appears.

PNBT SOI-FET. Fig. 4 shows the band diagrams in the n-channel PNBT SOI-FET at the off and on states as the super-steep SS appears. At the off state, the barrier heights between the channel region and the n-region are maintained. However, those barrier heights are lowered at the on state. When V_g is increased, electrons diffuse from the source to the n-region and decrease the n-region potential, as indicated by (1) in Fig. 4(a). As a result, the holes are injected into the channel region and increase the channel region potential [13], as indicated by (2) in Fig. 4(a). Therefore, the appearance of the super-steep SS is expected to be caused by the positive feedback of the inherent thyristor and by the SOI floating body effects. Moreover, I_b is a diffusion current, while I_d includes both drift and diffusion currents in the on state. Therefore, I_b is lower than I_d.

Devices that have a similar mechanism have been proposed, such as FBFETs [9], field-effect diodes [17], and

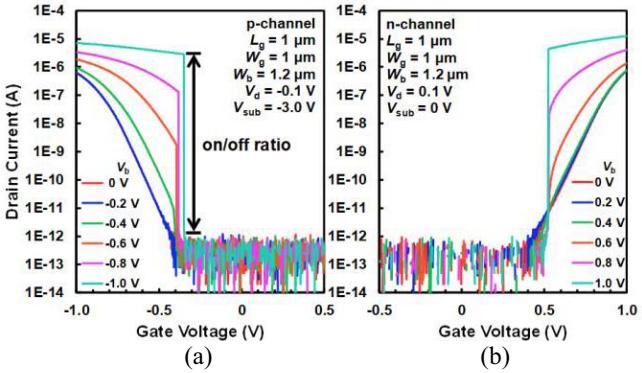

FIGURE 5. Measured I_d-V_g characteristics and dependence on V_b at L_g = 1 μm. (a) p-channel PNBT SOI-FET. (b) n-channel PNBT SOI-FET.

Z^2-FETs [18]. However, our PNBT structure makes it possible to realize a symmetrical S/D and operation with low V_d.

IV. ACTUAL MEASUREMENT CHARACTERISTICS

Fig. 5 shows the measured I_d–V_g characteristics and dependence on V_b at L_g = 1 μm. V_{sub} in the n-channel PNBT SOI-FET was grounded. On the other hand, V_{sub} in the p-channel PNBT SOI-FET was set to be −3.0 V because we found that negative V_{sub} is required to confirm super-steep SS on the p-channel PNBT SOI-FET. When V_b is equal to zero, PNBT SOI-FET acts as a conventional MOSFET. However, as V_b is raised to ± 0.6 V, the super-steep SS (< 1 mV/dec) appears in both p-channel and n-channel devices, keeping low I_{off} (< 1 pA/μm) and high on/off ratio (up to 6 decades). Fig. 6 shows the measured I_d and I_b−V_g characteristics dependence on V_{sub} at V_b = ± 0.8 V. In the n-channel PNBT SOI-FET, when V_{sub} is negatively biased, the trigger voltage of the super-steep SS slightly shifts to the positive direction. In contrast, in the p-channel PNBT SOI-FET, a large I_b flows and I_d and I_b are not controlled by V_g when V_{sub} = 0 V. The p-channel PNBT SOI-FET requires V_{sub} < −2.0 V to decrease I_{off} and induce the super-steep SS. This phenomenon seems to occur because of a barrier lowering for electron injection from the body terminal to the channel region. The expected cause along with the band diagram between the S/D and the body terminals in the p-channel PNBT SOI-FET are shown in Fig. 7. We consider that positive charge exists in the Box of SOI as discussed in [19]. When this charge is considered, the barrier height of the p-region is expected to become low. This results in electron injection and large I_{off} of the p-channel PNBT SOI-FET when V_{sub} is set to be unbiased (grounded). However, when a negative V_{sub} is applied, the barrier height of the p-region increases, reducing electron injection, which results in low I_{off} and the appearance of super-steep SS. A positive charge does not reduce the barrier height on the n-channel PNBT SOI-FET. Therefore, it is a specific phenomenon to the p-channel device. Moreover, fortunately, the n-channel PNBT SOI-FET maintains a super-steep SS even

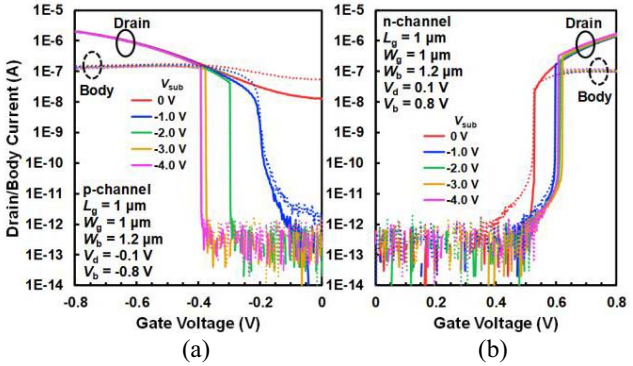

FIGURE 6. Measured I_d and I_b–V_g characteristics and dependence on V_{sub}. (a) p-channel PNBT SOI-FET. (b) n-channel PNBT SOI-FET. Solid line: I_d, dotted line: I_b.

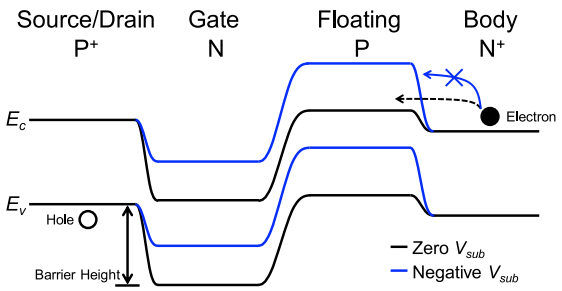

FIGURE 7. Illustration of a band diagram between S/D and body terminals in the p-channel PNBT SOI-FET.

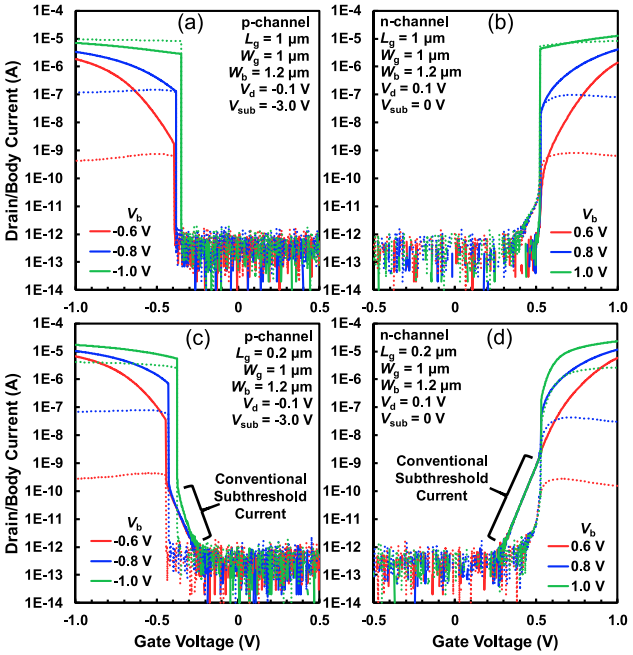

FIGURE 8. Measured I_d and I_b–V_g characteristics with various L_g's as the super-steep SS appears. (a) p-channel PNBT SOI-FET at L_g = 1 μm, (b) n-channel PNBT SOI-FET at L_g = 1 μm, (c) p-channel PNBT SOI-FET at L_g = 0.2 μm, (d) n-channel PNBT SOI-FET at L_g = 0.2 μm. Solid line: I_d, dotted line: I_b.

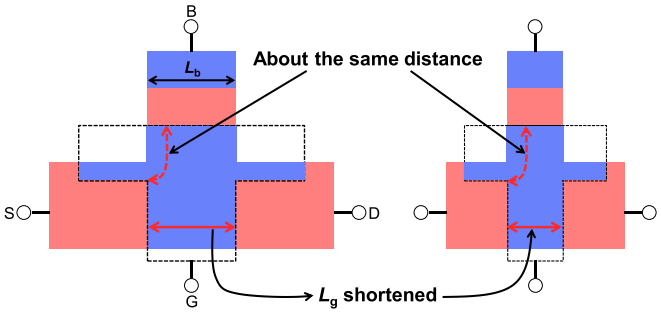

FIGURE 9. Illustration of difference between L_g = 1 μm and L_g = 0.2 μm. In this study, the body length L_b changes with L_g.

with negative V_{sub}. This indicates that both p-channel and n-channel PNBT SOI-FETs can operate as CMOS devices with the same $V_{sub} < -2.0$ V.

Fig. 8 shows the measured I_d and I_b–V_g characteristics for $L_g = 1$ μm and $L_g = 0.2$ μm with three V_b and V_{sub} conditions as the super-steep SS appears. At $L_g = 1$ μm, the super-steep SS occurs from the $I_d = 1$ pA level. The on/off ratio improves when V_b increases; however, I_b is larger than I_d at $V_b = 1.0$ V. In contrast, I_b is lower than I_d at $L_g = 0.2$ μm. However, the super-steep SS occurs from $I_d = 0.1 - 1$ nA level; therefore, the on/off ratio at $L_g = 0.2$ μm is less than that of $L_g = 1$ μm. This is expected owing to the difference in the threshold voltage V_{th} between the "source to drain" and "source to body terminal." Fig. 9 illustrates the difference between $L_g = 1$ μm and $L_g = 0.2$ μm. The "source to drain" and "source to body terminal" have different distances; therefore, V_{th} between these two directions is also different. V_{th} of "source to drain" with $L_g = 0.2$ μm is lower than V_{th} of "source to body terminal" because of the short-channel effect of the MOSFET. Therefore, a conventional subthreshold current starts to flow before the super-steep SS appears at the start of the "source to body terminal" current. However, both values of V_{th} are nearly the same for $L_g = 1$ μm. Therefore, the super-steep SS starts from a very low current level before the start of the conventional subthreshold current.

Fig. 10 shows a summary of the I_d/I_b ratios. The ratio was calculated from I_d and I_b at V_g as the super-steep SS appears in Fig. 8. At $L_g = 1$ μm, the I_d/I_b ratios are lower than 3. The I_d/I_b ratios at $L_g = 0.2$ μm are higher than for $L_g = 1$ μm. However, the ratios decrease with increasing V_b. It is desirable that the I_d/I_b ratio be higher than the V_b/V_d ratio to ensure that the power consumption by I_b is lower than by I_d. For example, in the p-channel PNBT SOI-FET, I_b at $L_g = 0.2$ μm with $V_b = 0.8$ V was less than one-tenth of I_d and the current ratio is higher than the V_b/V_d ratio (= 8). This means that the power consumption by I_b is lower than that of I_d when considering $P = I \times V$. Additionally, the body length L_b changes with L_g as shown in Fig. 9; thus, I_b at $L_g = 1$ μm is larger than I_d because

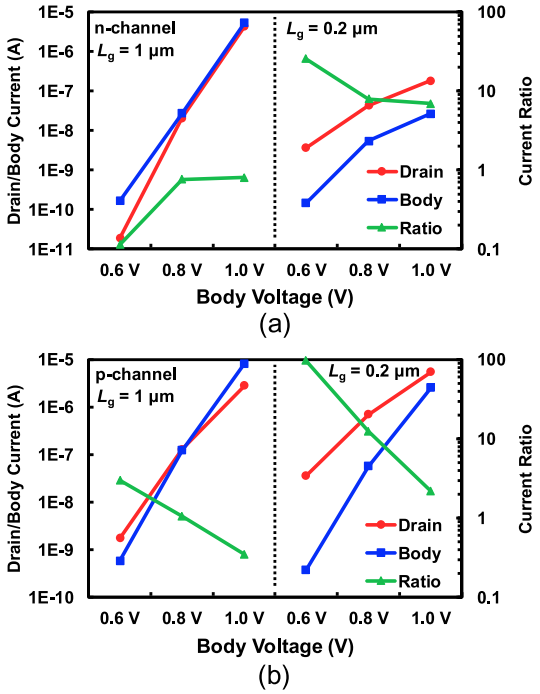

FIGURE 10. Measured I_d and I_b at V_g = minimum SS point and I_d/I_b ratio. (a) n-channel PNBT SOI-FET. (b) p-channel PNBT SOI-FET.

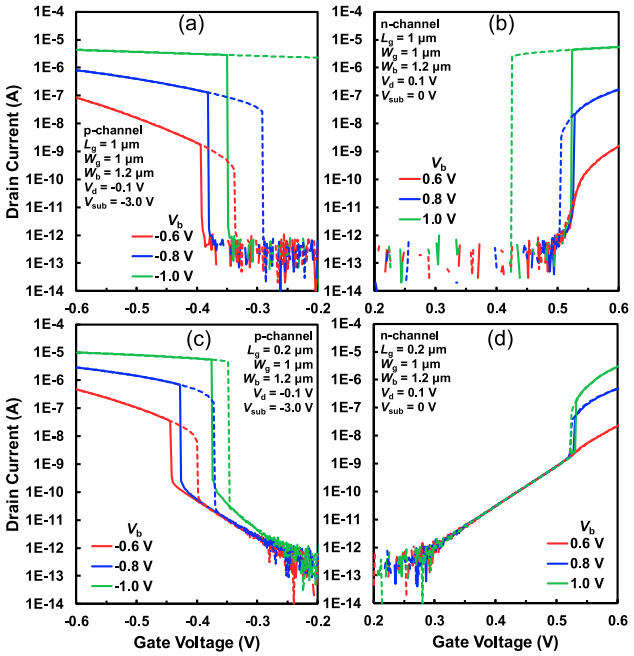

FIGURE 11. Double sweep measurement of I_d-V_g characteristics. (a) p-channel PNBT SOI-FET at $L_g = 1$ μm, (b) n-channel PNBT SOI-FET at $L_g = 1$ μm, (c) p-channel PNBT SOI-FET at $L_g = 0.2$ μm, (d) n-channel PNBT SOI-FET at $L_g = 0.2$ μm. Solid line: forward scan, dotted line: backward scan.

L_b is equivalent to the gate width of the inherent thyristor between the S/D and the body terminal.

Fig. 11 shows the results of the double-sweep measurement of I_d-V_g characteristics. All the devices exhibit hysteresis loops. We consider that the channel potential is maintained by the accumulated carriers, as shown in Fig. 3. Therefore, the PNBT SOI-FET has hysteresis characteristics. This phenomenon has also been confirmed on devices operating with a similar mechanism (i.e., using accumulation carriers) [7], [9], [16]–[18]. As V_b increases, the hysteresis widths at $L_g = 1$ μm increase. Particularly, the p-channel PNBT SOI-FET with $L_g = 1$ μm at $V_b = 1$ V cannot turn off. It is thought that the condition which cannot be turned off is induced by the accumulated carriers causing a strong positive feedback. The accumulated carriers in the entire SOI completely block the effect of the electric field from the gate [17]. In contrast, the hysteresis loop widths at $L_g = 0.2$ μm are lower than those at $L_g = 1$ μm. The difference between $L_g = 1$ μm and $L_g = 0.2$ μm seems to be the difference in the carrier accumulation area in the n (or p)-region and the channel region [14]. Fig. 12 shows the summary of hysteresis widths. The hysteresis widths are less than 0.1 V other than those of the p-channel PNBT SOI-FET with $L_g = 1$ μm at $V_b = 1$ V. It indicates that the CMOS with the PNBT SOI-FET can swing within $V_{DD} = 0.1$ V, even though a hysteresis width exists.

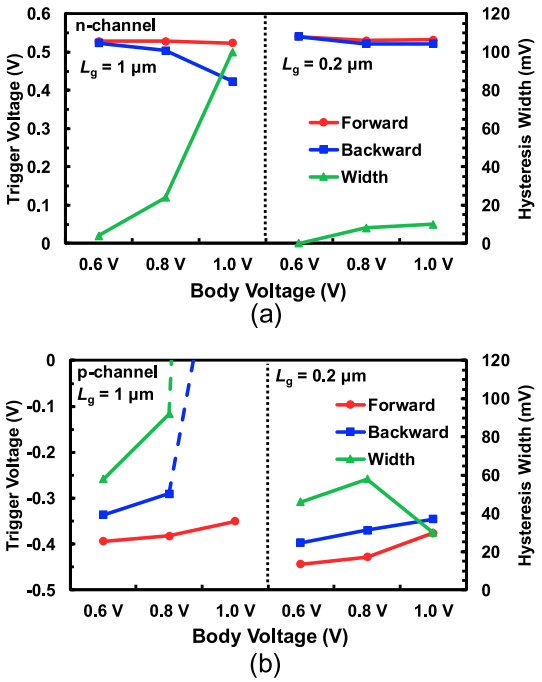

FIGURE 12. Measured trigger voltage and hysteresis width. (a) n-channel PNBT SOI-FET. (b) p-channel PNBT SOI-FET.

Summarizing the above, the on/off ratio, I_d/I_b ratio, and hysteresis widths are in a trade-off relationship. The L_g scaling improves the I_d/I_b ratio and hysteresis characteristics; however, the on/off ratio deteriorates. It is noted that when V_{th} of "source to body terminal" is set to be the same as V_{th} of "source to drain," the on/off ratio well improves as shown in Figs. 8–10. This is good news for the L_g scaling

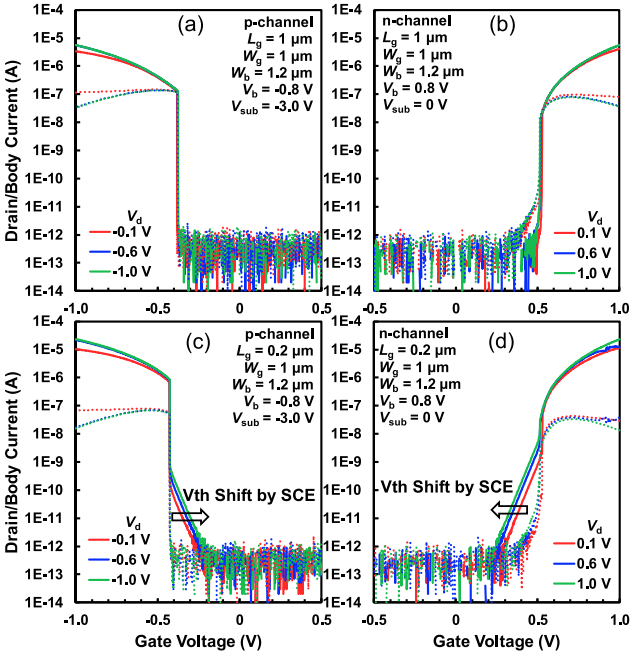

FIGURE 13. Measured I_d and I_b–V_g characteristics dependence on V_d. (a) p-channel PNBT SOI-FET at $L_g = 1$ μm, (b) n-channel PNBT SOI-FET at $L_g = 1$ μm, (c) p-channel PNBT SOI-FET at $L_g = 0.2$ μm, (d) n-channel PNBT SOI-FET at $L_g = 0.2$ μm. Solid line: I_d, dotted line: I_b.

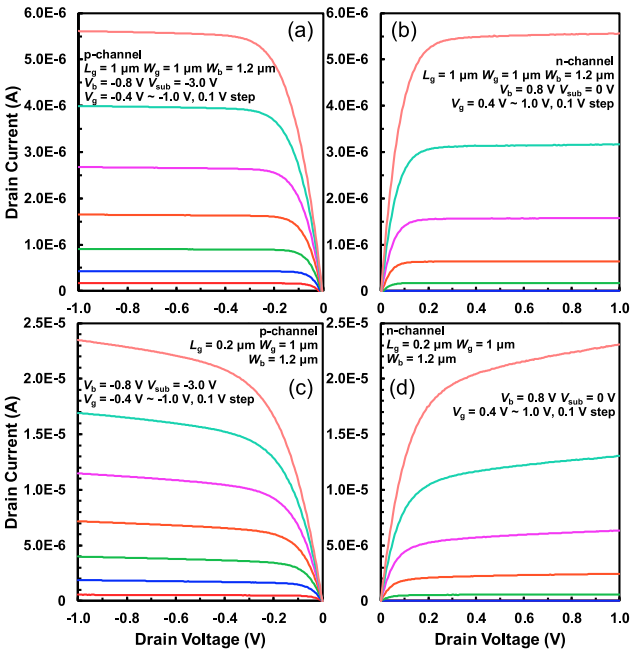

FIGURE 14. Measured I_d-V_d characteristics. (a) p-channel PNBT SOI-FET at $L_g = 1$ μm, (b) n-channel PNBT SOI-FET at $L_g = 1$ μm, (c) p-channel PNBT SOI-FET at $L_g = 0.2$ μm, (d) n-channel PNBT SOI-FET at $L_g = 0.2$ μm.

of the PNBT SOI-FET. The PNBT SOI-FET should be optimized by considering these conditions. Further research is necessary to overcome the trade-off.

We measured the dependence of V_d for high-performance operation with the PNBT SOI-FET. Fig. 13 shows the measured I_d and I_b–V_g characteristics at different values of V_d. At $L_g = 1$ μm, the super-steep SS appears at the same trigger voltage, regardless of the value of V_d. When $L_g = 0.2$ μm, the point at which the conventional subthreshold current begins to flow is shifted by V_d with the short-channel effect. Fig. 14 shows the measured I_d-V_d characteristics. There are no super-linear characteristics in the linear region and no hump characteristics in the saturation region, indicating that the PNBT SOI-FET has a good output characteristic. Additionally, we found a slight issue on the output characteristics, i.e., the PNBT SOI-FET has a slight reverse current at $V_d = 0$ V, as shown in Fig. 15. This is because the leakage current flows from the drain to the body terminal. This should be considered when designing practical circuits.

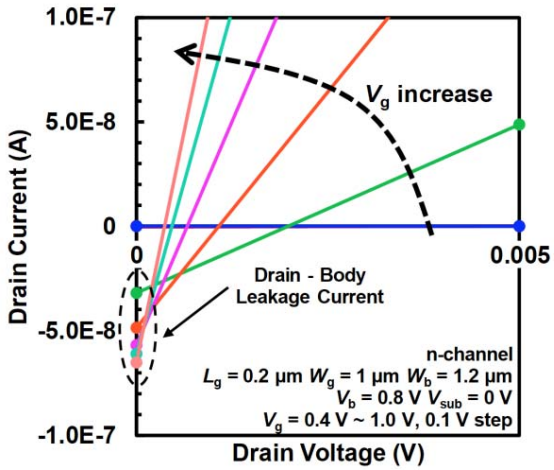

FIGURE 15. Expanded I_d-V_d characteristics of Fig. 14(d) around 0 V.

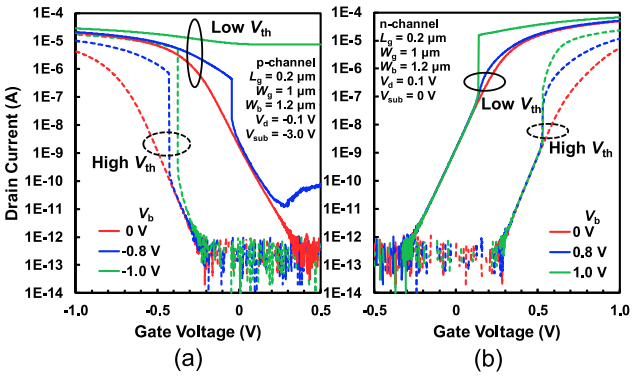

FIGURE 16. Measured I_d-V_g characteristics for two V_{th} devices. (a) p-channel PNBT SOI-FET at $L_g = 0.2$ μm, (b) n-channel PNBT SOI-FET at $L_g = 0.2$ μm.

Fig. 16 shows the measured I_d-V_g characteristics for two V_{th} devices. V_{th} is controlled by the channel impurity concentration. The super-steep SS also appears on the device when V_{th} approaches 0 V. This indicates that the PNBT has V_{th} controllability, and it means that the device design for the ultralow V_{DD} (e.g., 0.1 V) will be possible. However, the

PNBT SOI-FET uses the accumulation carriers to achieve super-steep SS. Therefore, channel impurity concentration is an important parameter because carriers do not accumulate in a fully depleted SOI MOSFET. More research is required on the degree of V_{th} controllability by the channel impurity concentration maintaining the super-steep SS.

V. CONCLUSION

We demonstrated p-channel and n-channel super-steep SS PNBT SOI-FETs. The operation mechanism of the PNBT SOI-FET is clarified by TCAD simulations. The super-steep SS is induced by the positive feedback with the inherent thyristor and the SOI floating body effect. The devices show a super-steep SS, maintaining a low I_{off} with a low V_d. We found that a negative V_{sub} is necessary to reduce I_b on the p-channel PNBT SOI-FET. The hysteresis widths are small depending on the condition. I_b is lower than I_d under appropriate conditions; however, I_b is not ignorable in the CMOS configuration. We must further reduce power consumption by I_b in CMOS invertor operation.

Moreover, the device has a good output characteristic and V_{th} controllability. This suggests that the n-channel and p-channel PNBTs have achieved the super-steep SS CMOS operation with ultralow $V_{DD} = 0.1$ V.

It is noted that for future studies, investigating the high-speed operation characteristics of the PNBT SOI-FET is necessary.

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