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Performance of Stacked Nanosheets Gate-All-Around and Multi-Gate Thin-Film-Transistors

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ABSTRACT This comprehensive study of the horizontally p-type stacked nanosheets inversion mode thin-film transistor with gate-all-around (SNS-GAATFT) and multi-gate (SNS-TFT) structures. The stacked nanosheets device structure, fabrication, and electrical characteristics are analyzed. The SNS-GAATFT reveals better performance to multi-gate SNS-TFT. The proposed inversion mode SNS-TFT has properties of the easy process with low cost and compatible with all 3-D Si CMOS and AMOLED applications. Moreover, the SNS-GAATFT is suitable for future monolithic 3-D IC for 2015's ITRS technology roadmap for the year 2024-2030.

INDEX TERMS Thin-film transistor (TFT), gate-all-around (GAA), Nanosheet (NS), stacked structure.

I. INTRODUCTION

To reduce the cost and enrich the smartphone, more functions are required to embed on a glass substrate of LCD and OLED display, which are called system on panel (SOP). Therefore, high-performance TFT is favorable, and multi-gate TFT is a strong candidate to enhance transistor characteristics. The multi-gate structure, such as tri-gate [1], and gate-all-around [2], [3] with ultra-thin body channel [4], [5], effectively enhance the gate control of the channel and thus reduce short channel effect (SCE) and leakage current. Recent studies [6], [7] have used 3D stacking technologies to integrate with multi-gate structures. However, the multi-gate TFT of the nanosheet channel with ultra narrow thickness yields a low conducting area and also has a high parasitic S/D resistance, resulting in the low driving current. Therefore, we provide a horizontally p-type multi-layer stacked nanosheets thin-film transistor with the gate-all-around structure to overcome this low driving current issue. In addition, we used 3D TCAD simulator to verify the SNS-GAATFT nanosheet dimension design. In short, the SNS-TFT suits for high driving current monolithic 3D (M3D) IC and AMOLED applications [8], [9].

II. EXPERIMENTAL DETAILS

Figure 1 shows the schematic diagram of channel structure and key process flow of the p-type stacked nanosheets thin film transistor (SNS-TFT) and the p-type stacked nanosheets gate-all-around thin film transistor (SNS-GAATFT). The double-channel SNS-GAATFT is fabricated by firstly growing a 400-nm-thick thermal SiO_2 layer on the 6-inch silicon wafer. A 50-nm-thick undoped amorphous silicon (a-Si) layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550°C as the bottom channel. Then, the a-Si layer was crystallized by solid-phase recrystallization (SPC) method at 600°C for 24 hrs in a nitrogen ambient atmosphere, forming large grains. A 30-nm-thick dry oxide was grown to separate two vertically stacked channels. Then, another 50-nm-thick a-Si was deposited by LPCVD and used

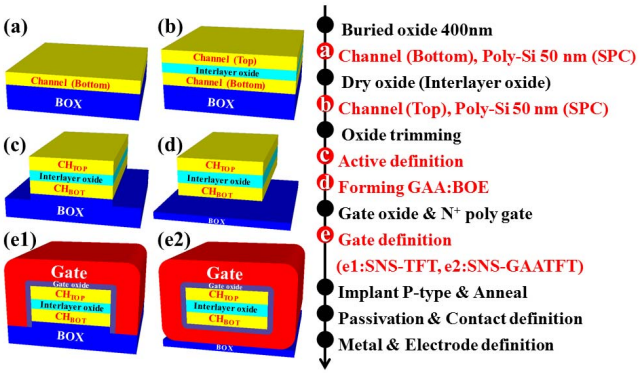


FIGURE 1. **The structure and key process flow of the p-type stacked nanosheets thin film transistor (SNS-TFT) and the p-type stacked nanosheets gate-all-around thin film transistor (SNS-GAATFT).**

SPC method as the top channel. The top channel applied oxidation trimming method to form a nanosheet (NS). The active region of the device was patterned by electron beam lithography (EBL) and transferred by reactive-ion etching (RIE). For forming GAA structure, the devices were dipped in BOE solution for suspending nanosheets. Next, a 10-nm-thick thermal SiO_2 layer was grown as the gate oxide layer. Then, 200-nm-thick in-situ doped n^+ poly-Si was formed as a gate electrode, and then patterned by EBL and RIE. The bottom and top channels were both implanted with same BF_2 ions dosage of 5E15 with 90 keV and 30 keV, respectively. Then, the dopant was activated by the rapid thermal annealing (RTA). After RTA, the top and the bottom channel region are doped with same concentration. The concentration of the top and the bottom channel region is confirmed by secondary ion mass spectrometer (SIMS). A 200-nm-thick TEOS was deposited as a passivation layer. Finally, a 300-nm-thick Al-Si-Cu metallization was performed and sintered at 400 °C for 30 minutes.

III. RESULTS AND DISCUSSION

Figure 2 (a) displays the TEM images of the SNS-TFT channel. The width and the height of the bottom channel of the SNS-TFT are 93.4 nm and 10.7 nm, respectively. And the width and height of the top channel of the SNS-TFT are 72.4 nm and 21.3 nm, respectively. The gate oxide thickness of the SNS-TFT is around 10.7 nm. It is noteworthy that the bottom channel of the SNS-TFT is a double gate device and the top channel of the SNS-TFT is a tri-gate device. Figure 2 (b) displays the TEM images of the SNS-GAATFT channel. The width and the height of the bottom channel of the SNS-GAATFT are 133 nm and 17.6 nm, respectively. And the width and height of the top channel of the SNS-GAATFT are 111 nm and 13.7 nm, respectively. The gate oxide thickness of the SNS-GAATFT is around 9 nm.

Figure 3 plots the normalized I_D-V_G curves for the (a) SNS-GAATFT and (b) SNS-TFT, respectively. The subthreshold slope (SS) of the SNS-GAATFT and SNS-TFT are 98.7 mV/dec and 151 mV/dec, respectively. Notably, the

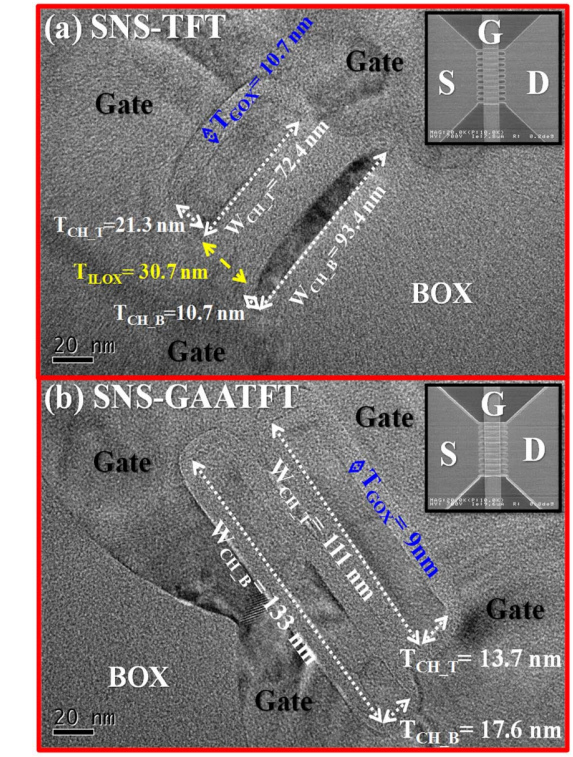


FIGURE 2. **TEM images for the two stacked nanosheet channels of (a) SNS-TFT and (b) SNS-GAATFT. Important dimensions are indicated. The inset SEM images are ten nanosheets after gate pattern dry etching.**

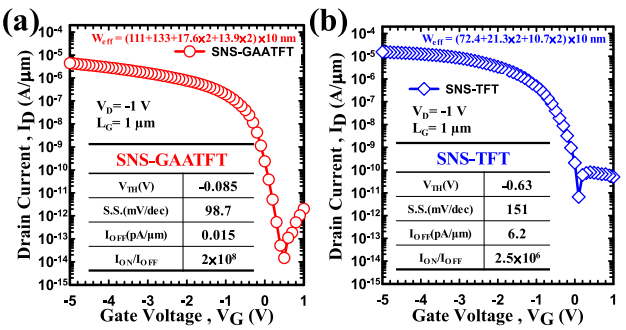


FIGURE 3. **(Experimental results) The I_D–V_G curves of (a) SNS-GAATFT (W_{eff} = (111+133+17.6×2+13.9×2)×10 nm) and (b) SNS-TFT (W_{eff} = (72.4+21.3×2+10.7×2)×10 nm).**

SNS-GAATFT has superior electrical characteristics such as lower off current and higher on/off current ratio, which owing to the gate-all-around structure has better gate control ability. Figure 4 (a)-(b) demonstrates temperature dependence on I_D–V_G curves for SNS-GAATFT and SNS-TFT devices. The SNS-GAATFT device exhibits the smallest temperature coefficients of V_{TH} (−2 mV/°C) and SS owing to the better gate control ability. Figure 5 (a)-(c) show the DIBLs, SS and off current at various L_G from 0.5μm to 1.0μm for SNS-GAATFT and SNS-TFT devices. The mean value is obtained from results for twenty devices with the same conditions with each L_G. The results reveal that the SNS-GAATFT structure can reduce short channel effect.

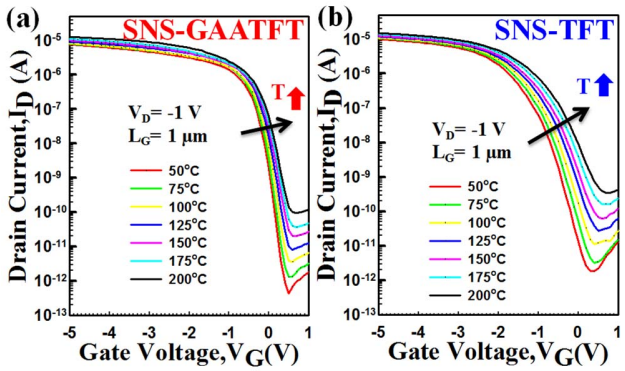


FIGURE 4. (Experimental results) The temperature variation effect of I_D–V_G curves of the (a) SNS-TFT and (b) SNS-GAATFT.

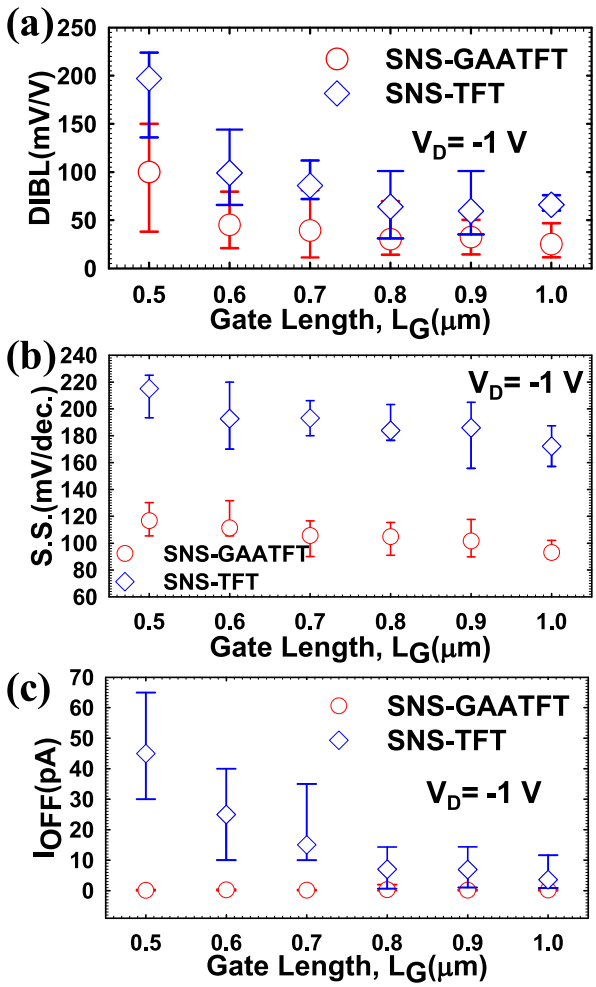
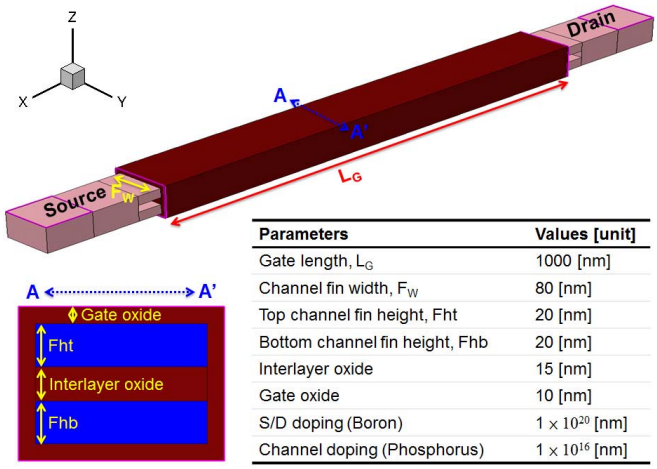


FIGURE 5. (Experimental results) The comparison with the (a) DIBL, (b) SS and (c) I_{OFF} at various L_G from 0.5 μm to 1.0 μm for the SNS-TFT and SNS-GAATFT. The mean and variation value is obtained from results of twenty devices. SNS-GAATFT shows smaller DIBL, SS, and I_{OFF} than SNS-TFT, owing to GAA structure has best gate electrical control.

Further detail study, technology computer-aided design (TCAD) simulation results are also utilized to demonstrate the physical inside of the SNS-GAATFT



Parameters	Values [unit]
Gate length, L_G	1000 [nm]
Channel fin width, F_W	80 [nm]
Top channel fin height, Fht	20 [nm]
Bottom channel fin height, Fhb	20 [nm]
Interlayer oxide	15 [nm]
Gate oxide	10 [nm]
S/D doping (Boron)	1×10^{20} [nm]
Channel doping (Phosphorus)	1×10^{16} [nm]

FIGURE 6. Device structure and important parameters of TCAD simulated of the p-type SNS-GAATFT.

and SNS-TFT. The simulated device structure and the important parameters are shown in Figure 6. The dimension of the simulated device is similar with the experimental SNS-GAATFT. The gate length (L_G) is set to 10 nm. This simulation used 10 nm of SiO_2 as the gate oxide. The channel fin width (F_W) is 80 nm and the top (Fht) and bottom (Fhb) channel height are 20 nm. The interlayer oxide is 15 nm which is between the top (Fht) and bottom (Fhb) channel. The doping concentrations of the source/drain and channel region are 1×10^{20} cm^{-3} and 1×10^{16} cm^{-3}, respectively. Phosphorus and Boron are used as the n-type and p-type dopant in the device simulation, respectively.

The physical models of Sentaurus TCAD were used to perform 3D simulations, which included density-gradient (DG) model, bandgap narrowing (BGN). The DG model for quantum correction was calibrated to the solution of the Poisson–Schrödinger equations. In order to take the high doping concentration of the source and drain region, the BGN model was comprised. The generation-recombination mechanisms are based on the doping concentration-dependent Shockley-Read-Hall (SRH) recombination model were also considered.

In this study, the nanosheets channel dimension design was analyzed by simulation and experiment, shown in Figure 7 (a)-(b). Figure 7 (a) plots the simulation results on I_{on}/I_{off} ratio versus the channel thickness and the nanosheet width for the SNS-GAATFT. Reducing the channel thickness and enlarging the nanosheet width improves I_{on}/I_{off} ratio of the SNS-GAATFT. Thinner channel thickness has excellent gate control to reduce I_{off}. Figure 7 (b) experimental results indicate that higher on current at the same off current can be enabled by larger width result from longer channel perimeter for a given track.

Figure 8 shows the TCAD simulated results for cross-sectional structure of the SNS-GAATFT and SNS-TFT with (a) Off state at $V_D = -1V$, $V_G = 0V$ and (b) On

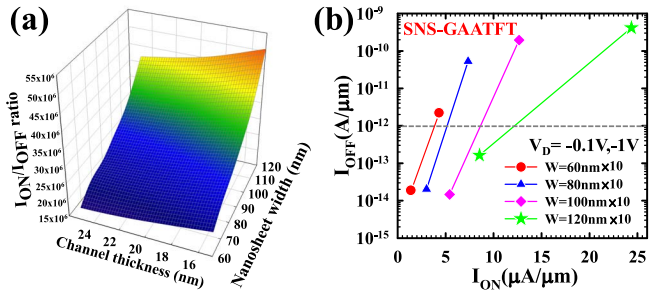


FIGURE 7. **(a) TCAD simulated 3D plot of SNS-GAATFT with different NS width and channel thickness for I_{ON}/ I_{OFF} ratio. It reveals that ultra-thin body and wide channel width has best I_{ON}/ I_{OFF} ratio. (b) Experimental results of I_{ON}–I_{OFF} performances of SNS-GAATFT with different channel width. Currents are all normalized by top width under the same channel thickness. Wide and thin SNS-GAATFT shows optimal I_{ON} and I_{OFF}.**

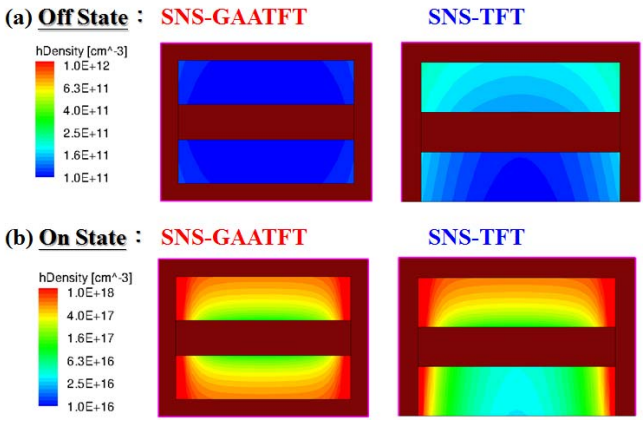


FIGURE 8. **TCAD simulated results for cross-section of the p-type SNS-TFT and SNS-GAATFT at (a) Off state ($V_D = -1V$, $V_G = 0V$) and (b) On state ($V_D = -1V$, $V_G = -1V$). SNS-GAATFT both show superior On and Off performance.**

state at $V_D = -1V$, $V_G = -1V$. In the off state, the SNS-GAATFT can effective fully deplete hole as a result of the device has better gate control ability. In the on state, the hole density results show that both the top channel and bottom channel of SNS-GAATFT are tri-gate devices. For the SNS-TFT, the top channel is a tri-gate device and the bottom channel is a double gate device.

IV. CONCLUSION

The horizontally p-type stacked nanosheets inversion thin-film transistor with gate-all-around (SNS-GAATFT) and multi-gate (SNS-TFT) structures are successfully demonstrated. The SNS-GAATFT reveals the better I_{on}/I_{off} ratio, SS, and DIBL. The TCAD simulation results also support the devices experimental performance. The SNS-TFT and SNS-GAATFT are highly promising for 2015's ITRS technology roadmap to the year 2024-2030[11]. Also, this high-performance SNS-GAATFT and SNS-JLTFT are favorable for AMLCD and AMOLED.

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