Received 30 June 2018: revised 5 August 2018 and 20 September 2018: accepted 23 September 2018. Date of publication 28 September 2018: date of current version 12 October 2018. The review of this paper was arranged by Editor P. R. Berger.

Digital Object Identifier 10.1109/JEDS.2018.2872689

# Suppressing Oxidation-Enhanced Diffusion of **Boron in Silicon With Oxygen-Inserted Layers**

DANIEL CONNELLY<sup>® 1</sup>, RICHARD BURTON<sup>1</sup>, NYLES W. CODY<sup>1</sup>, PAVEL FASTENKO<sup>2</sup>, MAREK HYTHA<sup>1</sup>, ROBERT STEPHENSON<sup>1</sup>, HIDEKI TAKEUCHI<sup>1</sup>, KEITH DORAN WEEKS<sup>1</sup>, AND ROBERT MEARS<sup>1</sup>

> 1 Atomera Inc., Los Gatos, CA 95032, USA 2 Synopsys Inc., Mountain View, CA 94043, USA

CORRESPONDING AUTHOR: D. CONNELLY (e-mail: daniel.connelly@atomera.com)

This work was supported by Atomera.

ABSTRACT Oxygen-Inserted (OI) layers are shown to shield a buried boron profile from oxidation enhanced diffusion. A TCAD model for the OI layer, including point defect and dopant trapping, as implemented in Sentaurus Process is shown to match experimental results, demonstrating the retention of steeper boron profiles after oxidation. Incorporation of the oxygen insertion layers into a CMOS process increases on-current and reduces threshold variability and mismatch.

**INDEX TERMS** Semiconductor device modeling, CMOS, diffusion, oxidation, interstitials.

#### I. INTRODUCTION

Boron diffusion in silicon is strongly enhanced by interstitials [1]. This is most evident for low temperature anneals with relatively little intrinsic diffusion. Interstitials can be generated by implants, resulting in transientenhanced-diffusion (TED), or via thermal oxidation, yielding oxidation-enhanced-diffusion (OED). In a typical CMOS process a well is created by ion implantation, then a gate insulator is thermally formed, causing OED of the well dopants. Source/drain and halo implants generate interstitials contributing to diffusion of profiles later in the process (TED). Steep doping gradients are important to device scaling, so reducing interstitials near the channel region during anneals is critical.

Doping control is important in a broad range of technologies. In planar CMOS, doping gradients in the channel and source/drain extensions are critical to scaling [2], and limiting the influence of doping variability [3]. In bulk FinFET CMOS, doping control of the punch-through stopper improves gate control of the channel, especially in lowoff-current devices [4]-[6]. But legacy planar nodes, for example 130 nm, remain active in present designs (e.g., [7]), and planar silicon CMOS remains popular in cost-sensitive higher-power technologies such as 5 volt [8].

Blocking layers can reduce interstitial populations. For example, inserting Si-Ge-C into the silicon [9] reduces boron

diffusion. Carbon immobilizes silicon interstitials, allowing for the formation of steeper profiles. A carbon dose of  $6 \times 10^{14}$  /cm<sup>2</sup> was able to reduce, but clearly not eliminate, diffusion of a buried boron marker during an 850 C, 30 min anneal. We propose another approach: utilizing buried epitaxial oxygen inserted (OI) layers to trap interstitials. OI layers were demonstrated to effectively preserve super-steep retrograde profiles in MOSFET channels from TED [6]. OI layers have been shown to reduce TED and thereby reduce junction depths [10]. Here we examine their effect on OED.

This experiment was described in our prior publication [11]. Here we present results for additional anneal conditions and a more sophisticated process model, with improved matching between simulation and experiment.

#### **II. EXPERIMENTS**

A silicon structure was epitaxially deposited as shown in Fig. 1. The following were deposited, in sequence:

- 1) an undoped epitaxial silicon buffer,
- 2) a 3 nm buried marker layer with a boron dose of approximately  $2 \times 10^{12}$ /cm<sup>2</sup>,
- 3) a nominally 50 nm undoped buffer,
- 4) a 14 nm OI region with oxygen dose comparable to the carbon dose used in [9] (omitted for control case),
- 5) another nominally 50 nm undoped buffer,



FIGURE 1. Schematic of deposited structure with OI layer.

- 6) an upper 3 nm marker layer with a boron dose of approximately  $2 \times 10^{12}/\text{cm}^2$ ,
- 7) a 50 nm undoped epitaxial silicon cap.

The following anneals in dry oxygen were performed, with the associated simulated oxide thicknesses (measured oxide thicknesses within 1 nm of simulated values):

- 800 C for 30 minutes (3 nm oxide),
- 850 C for 30 minutes (6 nm oxide),
- 850 C for 60 minutes (10 nm oxide),
- 875 C for 30 minutes (8 nm oxide),
- 900 C for 30 minutes (11 nm oxide).

In addition to oxidation, inert anneals could also have been tested. However, these require substantial care to avoid oxidation as the wafers are loaded into and removed from the furnace. For example, inert anneals can be performed in the epitaxial reactor without breaking vacuum.

## **III. CONTROL CASE**

To model the structure, the boron marker layers were treated as piecewise analytic profiles. The primary boron peaks were generated with smoothed boxes, formed with the superposition of two error functions. Additional exponential tails were fit to the unannealed profiles. The local maximum of a tail and the rounded box were used for the final profile. This "marker kernel" was applied to the positions of the individual markers, the same for each, and the same for each wafer. This is a simplification relative to fitting each marker individually.

To compare simulated results with SIMS measurements, the Gautier convolution kernel [12] was applied to the simulated "true" profiles. To this an additional surface component, proportional to  $e^{-xv}$ , with  $x \equiv$  depth and v = 0.6, was added to model surface contamination in the experimental SIMS. This process is important when simulating steep dopant profiles: to directly compare a simulation with SIMS would result in artificial smoothing of the actual profile.

SIMS profiles for the first two anneals without the OI region are shown in Fig. 2, along with S-Process simulations.



FIGURE 2. Results without OI layers: (a) 800 C for 30 minutes in oxygen, (b) 850 C for 30 minutes in oxygen.

The boron is substantially diffused such that the marker layers overlap, most notably in the 850 C anneal. The S-Process AdvancedCalibration models reproduce these results well, providing confidence in the process simulation's model for interstitial injection from dry oxidation and for the effect of interstitials on boron diffusion.

## **IV. MODELING OF OI LAYERS**

Modeling of OI layers included both the evolution of the layers themselves, and how they interact with point defects and dopants:

- 1) Oxygen can be liberated from an OI layer, creating free oxygen, at a rate proportional to the oxygen dose in the OI layer.
- 2) Free oxygen can be absorbed by an OI layer, proportional to the product of the concentration of free oxygen and the dose of trapped oxygen in the OI layer.
- 3) Free oxygen can diffuse, per Ficks Law.
- 4) Free oxygen diffusion is retarded by an OI layer, resulting in a finite difference of free oxygen across an OI layer proportional to the dose of trapped oxygen there and proportional to the free oxygen normal diffusive flux.

- 5) Interstitials are captured at the OI layer proportional to the adjacent concentrations of interstitials and proportional to available point defect trapping sites. Total point defect trapping sites are considered proportional to the trapped oxygen dose.
- Vacancies are captured at the OI layer proportional to the adjacent concentrations of vacancies and proportional to available point defect trapping sites.
- Interstitials and vacancies trapped at the OI layer can recombine, proportional to the product of the two area densities.
- Boron is trapped by the OI layer, proportional to available sites for boron trapping and to each adjacent boron concentration. Dopant trapping sites are proportional to the trapped oxygen.

Oxidation injects primarily interstitials [13], not vacancies, so vacancy modeling is non-critical. Additionally, since the profiles were formed separate from the OI region, dopant trapping and other direct dopant-OI interactions are deemphasized. However, as will be seen, dopant trapping still played a role in the results.

Equations were inserted into Sentaurus Process [14] using the Alagator scripting interface, using an Arrhenius dependence for kinetic terms. Point defect trapping was modeled with a relatively small 0.5 eV activation energy, but this parameter may be refined with future work. Boron trapping was assumed to be transport-limited, 3.53 eV based on diffusivity data [15].

Coefficients were taken from a variety of sources. The oxygen trapping and emission coefficients and activation energies were fit to inert anneals, using oxygen SIMS. Boron trapping was calibrated to a separate experiment where the diffused boron overlapped the OI layers. Dopant and point defect emission were considered insignificant at these temperatures. Vacancy trapping, not important to this experiment, was calibrated to experiments with arsenic implants. Vacancy calibration is ongoing and will be published in the future. Point defect recombination was set to a plausible value but was insignificant due to a dearth of vacancies. The interstitial trapping coefficient was treated as the single process fitting parameter for anneals up to 850 C, with the trapping capacity fitted to the 900 C anneal. The 875 C anneal was used only for model validation.

## **V. RESULTS WITH OI LAYERS**

The initial oxygen structure and model were calibrated using inverse modeling of oxygen SIMS, treating the oxygen profile as a series of  $\delta$ -functions, subsequently convolved with the Gautier kernel for comparison to SIMS. Trapped boron was also treated as  $\delta$ -functions.

A comparison between simulation and experiment for the 800 C and 850 C anneals is shown in Fig. 3. Profiles are shown both without and with the oxidation anneals. The spike in boron at the OI region was associated with inadvertant boron incorporation into the top of the OI region, modeled as a trapped boron dose of  $3 \times 10^{11}$ /cm<sup>2</sup>.



FIGURE 3. Results with OI layers, located where indicated in the figures: (a) 800 C for 30 minutes in oxygen, (b) 850 C for 30 minutes in oxygen, (c) 850 C for 60 minutes in oxygen.

Setting the peak interstitial trapping coefficient to  $3 \times 10^{-15}$  cm<sup>3</sup>/sec per OI layer oxygen atom at 850 C, with an activation energy of 0.5 eV, produces credible fits to all profiles. In each case a shift, attenuation, and widening of the upper marker profile is well reproduced, with the exception of the silicon immediately above the OI region, where boron



FIGURE 4. Higher temperature (875 C, 900 C) oxidations with OI layers.

concentration is overestimated. The increased diffusion of the upper peak is due to this peak being exposed to the interstitial flux from the surface oxidation. The upper boron marker shifts deeper because the interstitial concentration decreases closer to the OI region. Boron is more mobile toward the surface, less mobile toward the OI region. Thus boron tends to accumulate closer to the OI region. In contrast, there is substantially reduced diffusion of the buried peaks.

A comparison between experiment and simulation for the 875 C and 900 C anneals is shown in Fig. 4. Substantial reduction in the diffusion of the buried boron layer is evident in both cases. The 900 C result was sensitive to the modeling of the interstitial trapping capacity, and was used to calibrate the capacity of the OI layer for point defect trapping to one point defect per three oxygen atoms. The 900 C data also show the importance of modeling boron trapping, which increases through the OI region.

### **VI. INTERSTITIAL EVOLUTION**

Key to the modeling of these results is the evolution of the interstitial profiles. Interstitial concentrations integrated over the top micrometer of the structure are plotted in Fig. 5. Plots are shown for an oxidizing anneal (corresponding to the experiment) and in an inert anneal (simulation only). Oxidation increases the interstitial population, but the OI layers reduce the interstitial populations, according to the calibrated model. Interstitials, and therefore boron diffusion, is reduced even under inert anneal conditions.

The baseline inert curve is particularly interesting due to the peak. For times 0 to 2 seconds, the interstitials are increasing due to increased generation at the anneal temperature relative to room temperature. However, during the interval from 2 to 300 seconds, the vacancy concentration (not shown) reaches a level sufficient to substantially increase interstitial-vacancy recombination, and interstitial populations decrease. Finally after 300 seconds a steadystate equilibrium is reached. Oxidation without OI layers reduces the time lag to maximal interstitial concentration to



FIGURE 5. Net interstitials during 850 C anneals integrated to a 1  $\mu$ m depth. After an initial transient, OI layers reduce interstitial concentrations by an order of magnitude.



FIGURE 6. Trapped interstitials versus anneal time at 850 C: approximately linear for oxygen ambient, sub-linear for inert ambient.

100 msec, and maintains a high concentration throughout the anneal. With OI layers rapid trapping of interstitials reduces transient effects.

According to the model, the OI region reduces the bulk interstitial population by trapping. Trapped interstitials increase with time unless they are emitted (with a zero rate here), recombine with trapped vacancies (which have a low concentration here), or until available trapping sites are saturated. The total trapped interstitial concentration is plotted in Fig. 6. The trapped oxygen concentration is more than three times the trapped interstitial concentration, so the interstitial trapping continues through the anneal.

A key to this analysis is that the OI region reduces interstitial concentrations during oxidation, in some cases below the level of inert anneals without OI layers, implying reduced boron diffusion. In contrast, the insertion of Si-Ge-C into silicon [9] was shown to reduce diffusion during oxidation

 TABLE 1. Parametric improvements in 130 nm CMOS process with OI layers

 below the MOSFET channels.

parameter		NFET	PFET
isolated FET improvement	$\sigma_{ m VTLin}$	17%	8%
	$\sigma_{ m VTSat}$	19%	9%
paired FET improvement	$\sigma_{ m VTLin}$	17%	8%
	$\sigma_{ m VTSat}$	19%	15%
	$\Delta I_D$	20%	14%

only to a comparable level to what was observed during an "inert" anneal, although the claimed inert profile exhibited enhanced diffusion relative to what we predicted with Sentaurus Process simulations of the same anneal condition [11], implying only partial suppression of OED in their work, since the "inert" anneal was not truly inert.

## **VII. CMOS INTEGRATION**

Table 1 shows parametric improvements from adding OI layers to a commercial 130 nm process, including reduced transistor variability (transistors at different parts of the die) and improved transistor matching (transistors in adjacent matched pairs). A retrograde channel profile with a buried dopant peak provided by the OI region separates dopants from the channel, reducing the sensitivity of threshold voltage to local stochastic dopant variation [3]. Both n-FETs and p-FETs improved, demonstrating an advantage to both acceptor and donor channel profiles.

The simulated performance enhancement of using OI layers at the punch-through stopper layer of a 22 nm node FinFET were published in [6]. The advantage of steeper punch-through stopper doping gradients to a 7/8 nm node FinFET was documented in [4] and [5]. Accurately modeling a CMOS process requires calibrated treatment of both vacancies and interstitials, as well as the trapping of arsenic and phosphorus in addition to boron. Results of such experiments will be presented in a future publication.

#### **VIII. CONCLUSION**

Buried oxygen layers were effective at trapping interstitials generated by surface oxidation, reducing the diffusion of epitaxially-formed boron profiles. Modeling the boron diffusion required modeling the evolution of the oxygen and the interaction of the oxygen with interstitials and boron. Integration of these oxygen layers into a CMOS process improved device matching and drive current by reducing dopant diffusion.

#### REFERENCES

- B. Sadigh *et al.*, "Mechanism of boron diffusion in silicon: An ab initio and kinetic Monte Carlo study," *Phys. Rev. Lett.*, vol. 83, pp. 4341–4344, Nov. 1999. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevLett.83.4341
- [2] Y. Taur, "CMOS design near the limit of scaling," IBM J. Res. Develop., vol. 46, nos. 2–3, pp. 213–222, Mar. 2002.

- [4] X. Zhang *et al.*, "Analysis of 7/8-nm bulk-Si FinFET technologies for 6t-SRAM scaling," *IEEE Trans. Electron Devices*, vol. 63, no. 4, pp. 1502–1507, Apr. 2016.
- [5] X. Zhang *et al.*, "Comparison of SOI versus bulk FinFET technologies for 6T-SRAM voltage scaling at the 7-/8-nm node," *IEEE Trans. Electron Devices*, vol. 64, no. 1, pp. 329–332, Jan. 2017.
- [6] H. Takeuch *et al.*, "Punch-through stop doping profile control via interstitial trapping by oxygen-insertion silicon channel," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 481–486, Nov. 2017.
- [7] J. Dang et al., "A low noise figure K-band receiver in 130 nm CMOS," in Proc. 11th German Microw. Conf. (GeMiC), Mar. 2018, pp. 243–246.
- [8] J. Plummer, "Power devices: Silicon vs. new materials," in *Proc. Compel Conf.*, 2017, p. 9. [Online]. Available: http://sites.ieee.org/compel2017
- [9] M. S. Carroll, C.-L. Chang, J. C. Sturm, and T. Büyüklimanli, "Complete suppression of boron transient-enhanced diffusion and oxidation-enhanced diffusion in silicon using localized substitutional carbon incorporation," *Appl. Phys. Lett.*, vol. 73, no. 25, pp. 3695–3697, 1998. [Online]. Available: https://doi.org/10.1063/1.122866
- [10] X. Zhang *et al.*, "Effects of oxygen-inserted layers on diffusion of boron, phosphorus, and arsenic in silicon for ultra-shallow junction formation," *J. Appl. Phys.*, vol. 123, no. 12, 2018, Art. no. 125704. [Online]. Available: https://doi.org/10.1063/1.5022078
- [11] D. Connelly et al., "Suppressing oxidation-enhanced diffusion of boron via buried epitaxial oxygen-inserted layers in silicon," in Proc. 2nd Electron Devices Technol. Manuf. Conf., Mar. 2018, pp. 163–165.
- [12] B. Gautier, R. Prost, G. Prudon, and J. Dupuy, "Deconvolution of SIMS depth profiles of boron in silicon," *Surface Interface Anal.*, vol. 24, no. 11, pp. 733–745, 1996. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/%28SICI%291096-9918%28199610%2924%3A11%3C733%3A%3AAID-SIA173%3E3.0.CO%3B2-W
- [13] S. M. Hu, "Formation of stacking faults and enhanced diffusion in the oxidation of silicon," *J. Appl. Phys.*, vol. 45, no. 4, pp. 1567–1573, 1974. [Online]. Available: https://doi.org/10.1063/1.1663459
- [14] Sentaurus Process Version O-2018.06 User's Manual, Synopsys, Inc., Mountain View, CA, USA, 2018. [Online]. Available: http://www.synopsys.com
- [15] Complete Guide to Semiconductor Devices. Accessed: Oct. 2, 2018.
   [Online]. Available: http://elektroarsenal.net/impurity-diffusion-coefficients.html



**DANIEL CONNELLY** received the S.M. degree from MIT and the Ph.D. degree from Stanford University. He was with Motorola, Acorn Technologies, Synopsys Inc, the University of California at Berkeley, as a Visiting Scholar, and Atomera. His focus has been in semiconductor device and process simulation.

**RICHARD BURTON**, photograph and biography not available at the time of publication.

**NYLES W. CODY**, photograph and biography not available at the time of publication.

**PAVEL FASTENKO**, photograph and biography not available at the time of publication.

**MAREK HYTHA**, photograph and biography not available at the time of publication.



**ROBERT STEPHENSON** (M'01–SM'11) received the B.Sc. (Hons.) degree in electrical engineering from the University of Alberta, Canada, in 1991 and the Ph.D. degree from Cambridge University, U.K., in 1995, where he was a Post-Doctoral Fellow for one-year. He went to Japan as a Visiting Research Fellow with NRIM, Tsukuba. He spent two years with IMEC, Leuven, Belgium, on a Marie Curie Fellowship investigating 2-D dopant profiling techniques. In 1999, he joined Bookham Technologies, Oxfordshire, U.K., to research on

optoelectronic sensors and communication components. In 2001, he joined Nanovis, Newton, MA, USA to develop advanced optical components, which became Mears Technologies, and subsequently Atomera. He is currently researching on device implementation and characterization of novel electronic materials for leading edge CMOS devices. He was the 2011–12 Chairman for the Boston Section of the IEEE Photonics Society.

**HIDEKI TAKEUCHI**, photograph and biography not available at the time of publication.

**KEITH DORAN WEEKS** received the master's degree from Arizona State University. His work experience includes Lawrence Semiconductor Research Laboratories, Conexant, ASM Inc., and Atomera Inc. His expertise is in chemical vapor deposition of epitaxial silicon and its alloys.

**ROBERT MEARS**, photograph and biography not available at the time of publication.