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# An Optimized 4H-SiC Trench MOS Barrier Schottky (TMBS) Rectifier

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**ABSTRACT** This paper proposes an optimal 4H-silicon carbide trench MOS barrier Schottky (TMBS) Rectifier. The optimal structure of this rectifier is achieved by adding an N- wrapping region at the P+ shielding of the conventional TMBS structure, which significantly reduces the depletion region formed by the P+ shielding region. As a result, the proposed structure provides a lower ON-resistance comparing with the conventional P+ shielding structure. Moreover, we study the electric characteristics of the proposed structure via numerical simulation. Such a structure improves the specific ON-resistance and figure of merit of the conventional P+ shielding TMBS by 32.2% and 48.4%, respectively, and offers a high breakdown voltage, i.e., up to 1908 V.

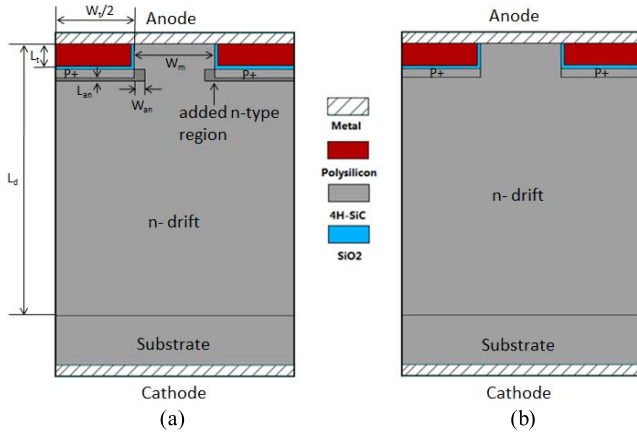
**INDEX TERMS** TMBS, breakdown voltage (BV), specific ON-resistance, figure of merit (FoM).

## I. INTRODUCTION

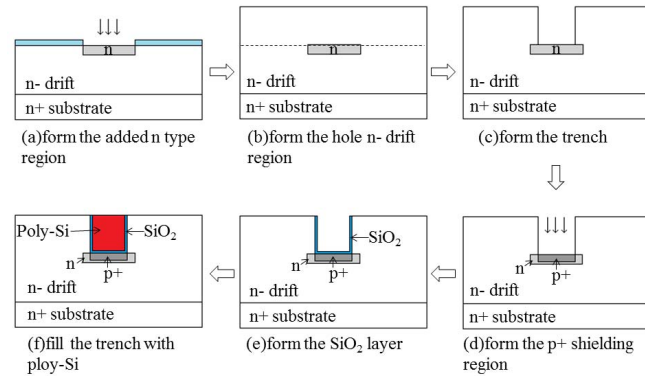
Silicon carbide (SiC) is a wide band-gap material which is endowed with high thermal conductivity, strong critical electric field and fast electron saturation drift, making it quite attractive for high-power and high-temperature applications [1]–[4]. The SiC Schottky diode introduces low onset voltage and no reverse recovery [3]. However, it is incapable of providing low ON-resistance and low leakage current density, as the Schottky barrier affects both the forward and reverse characteristics of the diode. To overcome this restriction, hybrid structure may be used, including the junction barrier Schottky (JBS), dual metal trench Schottky (DMT), and the trench MOS barrier Schottky (TMBS) diodes [5]–[8]. However, the JBS requires high temperature ion implantation and annealing at high temperatures, which causes big damage to the material, yielding working instability of the devices [9]. The DMT diode has less flexibility in adjusting the Schottky barrier which is used to optimize the forward and reverse performances [10]. The TMBS diode uses a thin MOS structure to modulate the electric field distribution, which may be tuned by adjusting the mesa width, the oxide thickness and the trench depth. Hence, one may achieve a low Schottky surface electric field while preserving the low ON-resistance easily [11], which

has been successfully used in the silicon field [12], [13]. However, a strong reverse bias electric field is distributed in the oxide layer which exceeds the withstand field of the oxide layer, yielding the TMBS structure unsuitable for the SiC field [11], [14]–[17]. To overcome this issue, the electric field in the oxide layer may be significantly reduced by adding a P+ shielding region at the trench bottom of the TMBS device, similar to the SiC MOSFET architecture. Nevertheless, the P+ shielding region brings the JFET region, which significantly increases the ON-resistance [18].

To address the above problem, here we propose an optimized 4H-SiC P+ shielding TMBS with low ON-resistance. Figures 1 (a) and (b) show cross-sectional views for the architectures of the proposed structure and the conventional TMBS structure. In contrast to the conventional P+ shielding structure, the optimized structure contains an N-type region with higher doping concentration than the drift region, wrapping the P+ shielding region incorporated at the trench bottom. This N-type region may widen the electron path during the on state, and hence, decreases the ON-resistance. In this paper, we provide a comprehensive study on the proposed structure, especially on the dopant concentration and the depth of the added N-type region.



**FIGURE 1.** Schematic cross-sectional view of (a) optimized p+ shielding TMBS and (b) conventional p+ shielding TMBS.



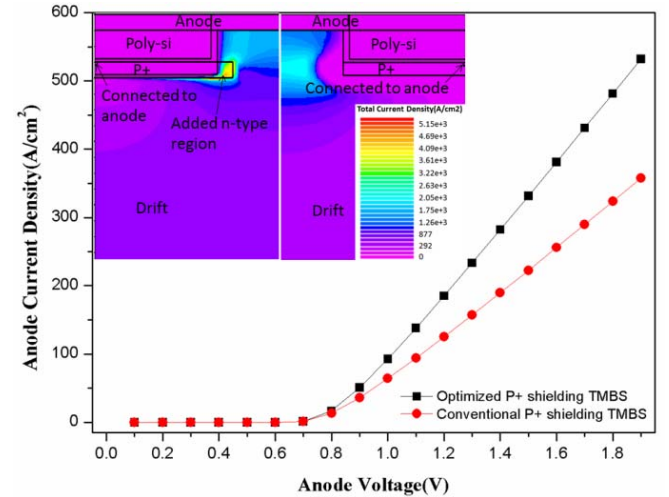
**FIGURE 2.** Main fabrication process steps for the optimized p+ shielding TMBS.

**II. FABRICATION PROCEDURE AND PARAMETERS**

In Fig. 2, we provide a feasible fabrication procedure of the proposed device. The main fabrication process steps are summarized as follows. A SiC epitaxial layer growing on an n+ type 4H-SiC substrate serves as the first drift layer. After a mask layer [cyan area in figure 2(a)] formed on the first drift layer, ion implantation is proceeded to form the added n-type region. Then the second drift layer [the region above the dashed line in figure 2(b)] grows on the first layer after the removal of the mask layer. The two drift layers have the same dopant concentration, and make up the whole drift region of the device. The dopant concentration and the thickness of the whole drift region are  $5 \times 10^{15} \text{cm}^{-3}$  and  $11 \mu\text{m}$ , respectively. Thereafter, the trench is formed by ICP etching with a depth of  $1 \mu\text{m}$  [16], and then ion implantation is applied to form the p+ shielding region at the bottom of the trench [deep shadowed area in Figure 2(d)]. Then, the oxide film is formed at the side wall and bottom of the trench by thermal oxidation and PECVD process [blue area in Figure 2(e)] [16]. The total thickness of the oxide is  $0.1 \mu\text{m}$ . Then, the trench is filled with polysilicon with p+ type dopant. Detailed parameters of the devices used in the simulation are listed in Tab. 1.

**TABLE 1.** Devices parameters for the simulations.

Parameter	Value
Width of trench( $W_t$ )	$4.0 \mu\text{m}$
Width of Mesa( $W_m$ )	$2.0 \mu\text{m}$
Width of added n-type region( $W_{an}$ )	$0.25 \mu\text{m}$
Thickness of drift( $L_d$ )	$11 \mu\text{m}$
Depth of trench( $L_t$ )	$1.0 \mu\text{m}$
Thickness of oxide	$0.1 \mu\text{m}$
Added n-type region depth( $L_{an}$ )	$0.1 \mu\text{m}$
p+ junction depth( $L_{p+}$ )	$0.4 \mu\text{m}$
n-drift Doping( $N_D$ )	$5 \times 10^{15} \text{cm}^{-3}$
Added n-type region Doping( $N_{an}$ )	$1.5 \times 10^{17} \text{cm}^{-3}$



**FIGURE 3.** Forward characteristic and total current density contours of the optimized and the conventional p+ shielding TMBS.

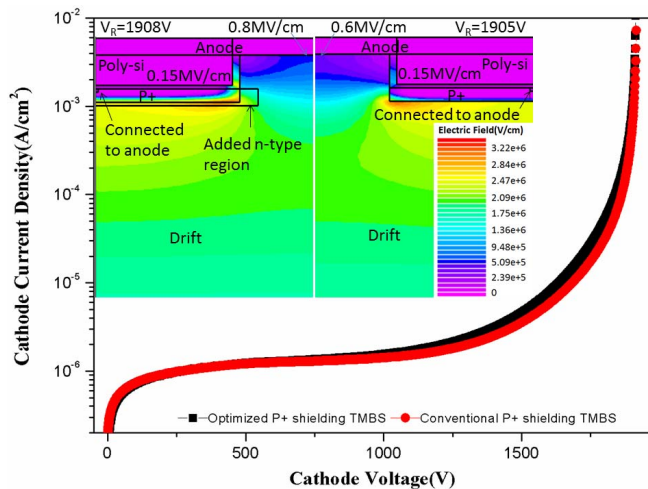
**III. SIMULATION RESULTS AND DISCUSSION**

To best investigate the performance of the structures in Figs. 1(a) and (b), we use the 2-D simulation tool ATLAS, considering the parameters described above. The simulation software uses a variety of physical models, including the comob, analytic, fldmob, srh, auger, fermi, incomplete, bgn and impact selb [19]. For the sake of comparison, we simulate both the proposed structure and a conventional P+ shielding TMBS with the same parameters.

*Forward Characteristics:* Figure 3 plots the simulation results for the forward I-V curves of the optimized P+ shielding TMBS and the conventional P+ shielding TMBS. These results show that the I-V curve slope of the optimized structure is apparently greater than that of the conventional structure. Moreover, these two structure presents specific ON-resistance of  $1.98 \text{m}\Omega \cdot \text{cm}^2$  and  $2.92 \text{m}\Omega \cdot \text{cm}^2$ , respectively (at  $J_F = 400 \text{A/cm}^2$ ,  $W_{an} = 0.25 \mu\text{m}$  and  $N_{an} = 1.5 \times 10^{17} \text{cm}^{-3}$ ), which is 32.2% lower than that of the conventional structure. The current density contours of the optimized and the conventional P+ shielding TMBS for the case of  $V_F = 2 \text{V}$  are shown in the inset of Fig. 2. From this picture, it may be seen that the current path of the optimized P+ shielding TMBS is wider than that of the conventional structure. Such a wide current path is due to

the added N<sup>-</sup> type region with higher doping concentration than the drift region. According to the semiconductor PN junction theory, the width of the depletion region may be made narrower by increasing the doping concentration. Hence, the added N<sup>-</sup> type region may reduce the depletion region width caused by the P<sup>+</sup> shielding region, and widen the current path. As a result, the ON-resistance of the device significantly decreased.

**Reverse Characteristics:** Figure 4 plots the simulation results for the reverse I-V curves of the optimized P<sup>+</sup> shielding TMBS and the conventional structure. The breakdown voltage of these two structures at room temperature is respectively 1908V and 1905V. Figure 4 also shows the electric field contours of the optimized P<sup>+</sup> shielding TMBS and the conventional structure at the breakdown. It may be seen from this figure that the electric field in the bottom oxide layer is very weak, i.e., about 0.15MV/cm, which is much lower than the critical strength value [11]. In addition, the peak electric field of both structures appears at the corner of the P<sup>+</sup> shielding region. Because the added N-type region has higher doping concentration than the drift region, the field shielding effect is reduced. So the electric field of the optimized structure at the Schottky surface (0.8MV/cm) is higher than that of the conventional P<sup>+</sup> shield structure (0.6MV/cm). The higher electric field at the schottky interface brings to larger schottky barrier lowering [22]. Therefore the reverse leakage current density is slightly higher than that of the conventional TMBS, as is shown in the figure 4.



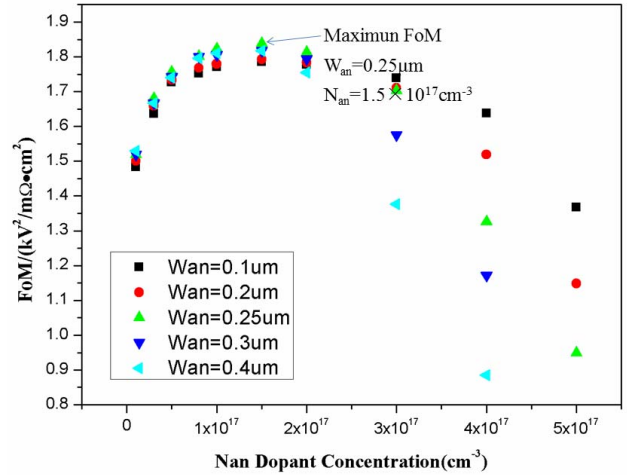
**FIGURE 4.** Reverse characteristic curves and electric field contours of the optimized p<sup>+</sup> shielding TMBS and the conventional p<sup>+</sup> shielding TMBS.

**Parameter Optimization:** We use the Figure of merit (FoM)  $V_{BR}^2/R_{on-sp}$  to comprehensively evaluate the positive and negative characteristics of the device [18]. According to the simulation results, the FoM of the proposed and conventional devices are about 1.84 kV<sup>2</sup>/mΩ·cm<sup>2</sup> and 1.24 kV<sup>2</sup>/mΩ·cm<sup>2</sup>, respectively. As shown in Tab. 2, the FoM of the proposed device has improved by 48.4%

**TABLE 2.** Performance comparison.

Parameter	Optimized TMBS	Conventional TMBS	Percentage
BV(V)	1908	1905	+0.3
$R_{on-sp}(m\Omega \cdot cm^2)$	1.98	2.92	-32.2
$FoM(kV^2/m\Omega \cdot cm^2)$	1.84	1.24	+48.4

+: increased; -: reduced.



**FIGURE 5.** The Simulation results for FoM of the optimized P<sup>+</sup> shielding TMBS.

compared to the conventional TMBS device. The doping concentration  $N_{an}$  and the width of the added N-type region  $W_{an}$  are of great influence on the proposed device. Thus, we optimize these two parameters, where the  $N_{an}$  ranges from  $1 \times 10^{16} cm^{-3}$  to  $5 \times 10^{17} cm^{-3}$  and the  $W_{an}$  ranges from 0.1 um to 0.25 um.

Firstly, with the increase in the  $N_{an}$ , the FoM rapidly reaches to its peak value and then decreases gradually. This may be explained with the help of the ON-resistance and the breakdown voltage extracted from the simulation process. When the  $N_{an}$  is lower than  $1.5 \times 10^{17} cm^{-3}$ , the depletion region form by the P<sup>+</sup> region is wider, so the current path is narrow, as the case of conventional P<sup>+</sup> structure shown in the Fig. 3. As we see in the Fig. 6, by increasing the  $N_{an}$ , the depletion becomes smaller immediately, yielding rapid decrease in the ON-resistance. Additionally, as Fig. 7 shows, the breakdown voltage almost remains unchanged when the  $N_{an}$  is smaller than  $1 \times 10^{17} cm^{-3}$ . These two factors lead to increase in the FoM with the increase in the  $N_{an}$ , and reaches to its peak value when the  $N_{an}$  is around  $1 \times 10^{17} cm^{-3}$ . Further increasing the  $N_{an}$ , the specific ON-resistance will decrease slowly to saturation. Moreover, when the  $N_{an}$  is bigger than  $2 \times 10^{17} cm^{-3}$ , the P<sup>+</sup> region cannot shield the oxide layer, so that the breakdown voltage decreases with further increase in the  $N_{an}$ , which is depicted in Fig. 7. Finally, the FoM decreases with the increase in the  $N_{an}$ .

Secondly, for a small  $N_{an}$ , the N- region width,  $W_{an}$ , slightly affects the FoM, for  $N_{an}$  is the key factor to the FoM during this section as discussed above. However, as we see

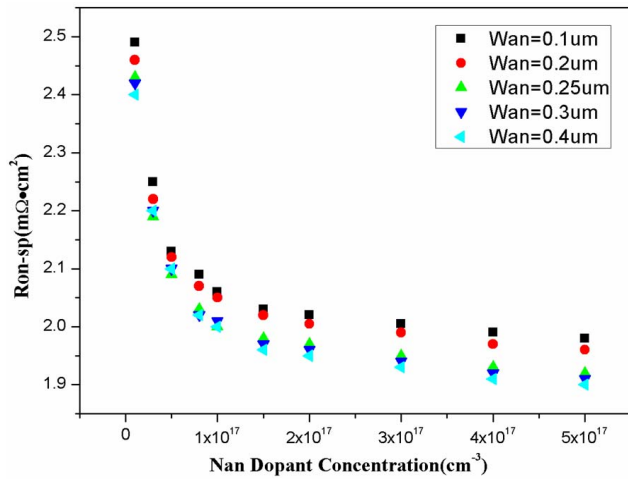


FIGURE 6. The Simulation results for specific ON-resistance of the optimized P+ shielding TMBS.

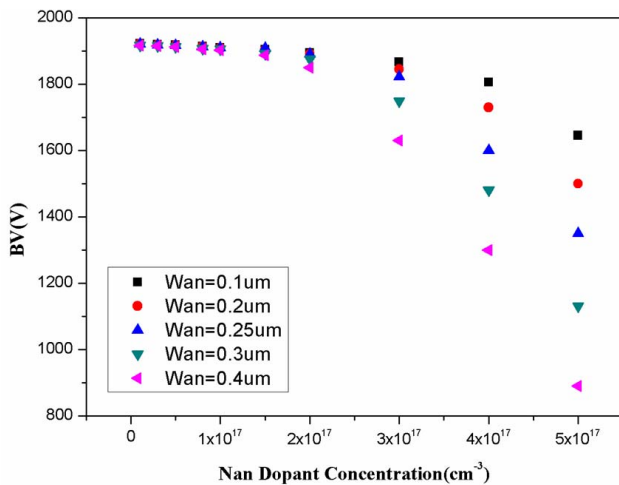


FIGURE 7. The Simulation results for breakdown voltage of the optimized P+ shielding TMBS.

in Fig. 7, when the  $N_{an}$  is greater than  $2 \times 10^{17} cm^{-3}$ , the  $W_{an}$  significantly affects the breakdown voltage, because the electric field in the oxide soars with the increase in  $W_{an}$ . Simultaneously, the specific ON-resistance is more stable when the  $N_{an}$  is bigger than  $2 \times 10^{17} cm^{-3}$ . As a result, as shown in the Fig. 5, the FoM becomes worse when the  $W_{an}$  is large. Additionally, we may find that the breakdown voltage exhibits a big window for the  $N_{an}$  and  $W_{an}$ , reducing the manufacturing requirements.

**Temperature Effects:** Figure 8 (a) and (b) plot the forward I-V characteristics and reverse leakage current density at 1300V of the optimized and conventional P+ shielding TMBS in a temperature range from 300 to 600 K. These results are achieved through the simulation using ATLAS software, where the lat.temp model is used and the therm-contact is defined. The optimized parameters listed in Tab. 1 are used and the localized self-heating effect is taken into account [19]. As the figure 8 (a) shows, when the forward

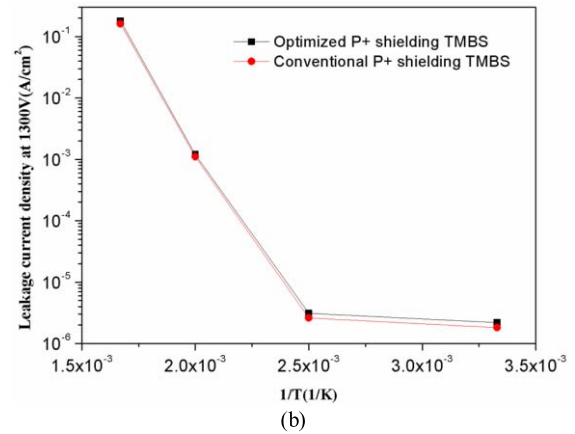
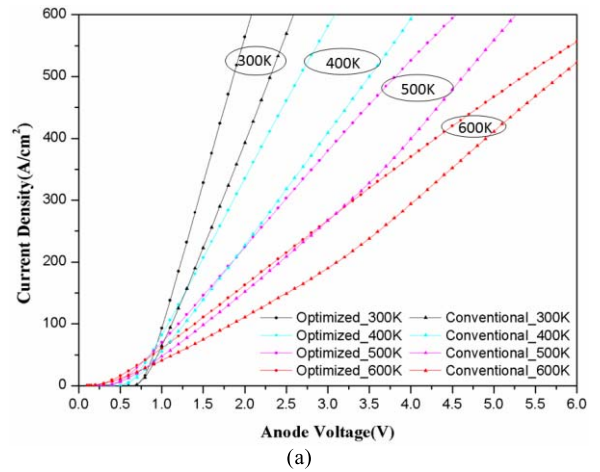


FIGURE 8. Forward I-V characteristics (a) and reverse current density at 1300V (b) of the Optimized and Conventional P+ shielding TMBS in a temperature range from 300 to 600 K.

voltage is less than 0.7 V, the forward voltage and the onset voltage decrease with the temperature rise. The reason is that current being dominated by thermionic emission at low current density [20]. While the forward voltage is more than 0.7 V, the temperature dependence of the current turns to negative. The lattice scattering is the main scattering mechanism due to the low doping concentration in the drift region. Hence, as the temperature rises, the scattering will enhance, causing rapid decrease in the electron mobility. For the 4H-SiC, it may be expressed as [21]

$$\mu_n(4H - SiC) = 1140 \left( \frac{T}{300} \right)^{-2.70} \quad (1)$$

The decrease in mobility will cause the ON-resistance increase in the drift region. So the I-V curve slope declines with the temperature rise as shown in the figure 8 (a). In comparison, the proposed structure has lower ON-resistance than the conventional one.

In figure 8 (b), the reverse leakage current density at 1300V depending on the temperature of both optimized and conventional devices is demonstrated in the form of Arrhenius plots. As the temperature rise, the leakage current



density of the two devices increases, which is mainly attributed to the thermionic emission through the schottky barrier and schottky barrier lowering [22], [23]. The leakage current of the optimized TMBS is slightly larger than that of the conventional one due to the added N-type region reducing the field shielding as explained in the reverse characteristics part.

#### IV. CONCLUSION

This paper proposes an improved P+ shielding 4H-SiC TMBS device structure with an N- type wrapped region. Compared to the conventional device, the ON-resistance has significantly reduced and the FoM has greatly improved. The doping concentration and the width of the added N-type region have been optimized using the ATLAS software. As a result, the specific ON-resistance and the FoM has improved by 32.2% and 48.4%, respectively, compared to the conventional P+ shielding TMBS. Additionally, the ON-resistance of the optimized device is lower than that of the conventional one up to 600K.

#### REFERENCES

- [1] M. Shur, S. Rumyantsev, and M. Levinshstein, *SiC Materials and Devices*, vols. 1–2. Beijing, China: Publ. House Electron. Ind., 2012.
- [2] R. Singh, J. A. Cooper, M. R. Melloch, T. P. Chow, and J. W. Palmour, "SiC power Schottky and PiN diodes," *IEEE Trans. Electron Devices*, vol. 49, no. 4, pp. 665–672, Apr. 2002, doi: [10.1109/16.992877](https://doi.org/10.1109/16.992877).
- [3] A. Itoh, T. Kimoto, and H. Matsunami, "Excellent reverse blocking characteristics of high-voltage 4H-SiC Schottky rectifiers with boron-implanted edge termination," *IEEE Electron Device Lett.*, vol. 17, no. 4, pp. 139–141, Mar. 1996, doi: [10.1109/55.485193](https://doi.org/10.1109/55.485193).
- [4] J. D. Scofield *et al.*, "High temperature DC–DC converter performance comparison using SiC JFETs, BJTs and Si MOSFETs," *Mater. Sci. Forum*, vols. 556–557, pp. 991–994, Sep. 2007, doi: [10.4028/www.scientific.net/MSF.556-557.991](https://doi.org/10.4028/www.scientific.net/MSF.556-557.991).
- [5] F. Dahlquist, C. M. Zetterling, M. Östling, and K. Rottner, "Junction barrier Schottky diodes in 4H-SiC and 6H-SiC," *Mater. Sci. Forum*, vols. 264–268, pp. 1061–1064, Feb. 1998, doi: [10.4028/www.scientific.net/MSF.264-268.1061](https://doi.org/10.4028/www.scientific.net/MSF.264-268.1061).
- [6] K. J. Schoen, J. P. Henning, J. M. Woodall, J. A. Cooper, and M. R. Melloch, "A dual-metal-trench Schottky pinch-rectifier in 4H-SiC," *IEEE Electron Device Lett.*, vol. 19, no. 4, pp. 97–99, Apr. 1998, doi: [10.1109/55.663526](https://doi.org/10.1109/55.663526).
- [7] N. Ren, J. Wang, and K. Sheng, "Design and experimental study of 4H-SiC trenched junction barrier Schottky diodes," *IEEE Trans. Electron Devices*, vol. 61, no. 7, pp. 2459–2465, Jul. 2014, doi: [10.1109/TED.2014.2320979](https://doi.org/10.1109/TED.2014.2320979).
- [8] W. C.-W. Hsu, F. Udrea, P.-L. Lin, Y.-Y. Lin, and M. Chen, "Innovative designs enable 300-V TMBS® with ultra-low on-state voltage and fast switching speed," in *Proc. IEEE 23rd Int. Symp. Power Semicond. Devices ICs*, Sep. 2011, pp. 80–83, doi: [10.1109/ISPSD.2011.5890795](https://doi.org/10.1109/ISPSD.2011.5890795).
- [9] Y. Wang, H.-Y. Wang, F. Cao, and H.-Y. Wang, "High performance of polysilicon/4H-SiC dual-heterojunction trench diode," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1653–1659, Apr. 2017, doi: [10.1109/TED.2017.2662198](https://doi.org/10.1109/TED.2017.2662198).
- [10] F. Roccaforte, F. La Via, A. La Magna, S. Di Franco and V. Raineri, "Silicon carbide pinch rectifiers using a dual-metal Ti-Ni<sub>2</sub>Si Schottky barrier," *IEEE Trans. Electron Devices*, vol. 50, no. 8, pp. 1741–1747, Aug. 2003, doi: [10.1109/TED.2003.815127](https://doi.org/10.1109/TED.2003.815127).
- [11] B. J. Baliga, *Advanced Power Rectifier Concepts*. Boston, MA, USA: Springer, 2009, doi: [10.1007/978-0-387-75589-2](https://doi.org/10.1007/978-0-387-75589-2).
- [12] M. Mehrotra and B. J. Baliga, "The trench MOS barrier Schottky (TMBS) rectifier," in *Proc. IEEE Int. Electron Devices Meeting*, Washington, DC, USA, 1993, pp. 675–678, doi: [10.1109/IEDM.1993.347222](https://doi.org/10.1109/IEDM.1993.347222).
- [13] M. Mudholkar, M. T. Qaddus, D. Bushong, A. Sarwari, and A. Salih, "A novel trench Schottky rectifier structure with controlled conductivity modulation," in *Proc. IEEE 26th Int. Symp. Power Semicond. Devices (IC's)*, Waikoloa, HI, USA, 2014, pp. 139–142, doi: [10.1109/ISPSD.2014.6855995](https://doi.org/10.1109/ISPSD.2014.6855995).
- [14] V. Khemka, V. Ananthan, and T. P. Chow, "A 4H-SiC trench MOS barrier Schottky (TMBS) rectifier," in *Proc. 11th Int. Symp. Power Semicond. Devices (ICs)*, Toronto, ON, Canada, 1999, pp. 165–168, doi: [10.1109/ISPSD.1999.764088](https://doi.org/10.1109/ISPSD.1999.764088).
- [15] K. W. Chu *et al.*, "An improvement of trench profile of 4H-SiC trench MOS barrier Schottky (TMBS) rectifier," *Mater. Sci. Forum*, vols. 740–742, pp. 687–690, Jan. 2013, doi: [10.4028/www.scientific.net/MSF.740-742.687](https://doi.org/10.4028/www.scientific.net/MSF.740-742.687).
- [16] C.-Y. Lee *et al.*, "A novel 4H-SiC trench MOS barrier Schottky rectifier fabricated by a two-mask process," in *Proc. 25th Int. Symp. Power Semicond. Devices (IC's)*, Kanazawa, Japan, 2013, pp. 139–142, doi: [10.1109/ISPSD.2013.6694473](https://doi.org/10.1109/ISPSD.2013.6694473).
- [17] D. Cho *et al.*, "High-voltage 4H-SiC trench MOS barrier Schottky rectifier with low forward voltage drop using enhanced sidewall layer," *Jpn. J. Appl. Phys.*, vol. 54, no. 12, Oct. 2015, Art. no. 121301, doi: [10.7567/JJAP.54.121301](https://doi.org/10.7567/JJAP.54.121301).
- [18] J. Tan, J. A. Cooper, and M. R. Melloch, "High-voltage accumulation-layer UMOSFET's in 4H-SiC," *IEEE Electron Device Lett.*, vol. 19, no. 12, pp. 487–489, Dec. 1998, doi: [10.1109/55.735755](https://doi.org/10.1109/55.735755).
- [19] *ATLAS User's Manual: Device Simulation Software, Version 5.16.3.R*, Silvaco Inc., Santa Clara, CA, USA, 2010.
- [20] R. Raghunathan, D. Alok, and B. J. Baliga, "High voltage 4H-SiC Schottky barrier diodes," *IEEE Electron Device Lett.*, vol. 16, no. 6, pp. 226–227, Jun. 1995, doi: [10.1109/55.790716](https://doi.org/10.1109/55.790716).
- [21] N. G. Wright, D. J. Morrison, C. M. Johnson, and A. G. O'Neill, "Electrothermal simulation of 4H-SiC power devices," *Mater. Sci. Forum*, vols. 264–268, pp. 917–920, Feb. 1998, doi: [10.4028/www.scientific.net/MSF.264-268.917](https://doi.org/10.4028/www.scientific.net/MSF.264-268.917).
- [22] M. Bakowski, J.-K. Lim, and W. Kaplan, "Merits of buried grid technology for SiC JBS diodes," *ECS Trans.*, vol. 50, no. 3, pp. 415–424, 2013, doi: [10.1149/05003.0415sect](https://doi.org/10.1149/05003.0415sect).
- [23] H. Elahipanah *et al.*, "Design optimization of a high temperature 1.2 kV 4H-SiC buried grid JBS rectifier," *Mater. Sci. Forum*, vol. 897, pp. 455–458, May 2017, doi: [10.4028/www.scientific.net/MSF.897.455](https://doi.org/10.4028/www.scientific.net/MSF.897.455).

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