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# Consideration of UFET Architecture for the 5 nm Node and Beyond Logic Transistor

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**ABSTRACT** In this paper, we propose a trench MOS architecture for the upcoming 5 nm node and beyond logic transistor. The intended device has a gate formed vertically downward, with added spacers along the gate to S/D sidewall. In doing so, the recessed device having longer channel length (than the defined gate footprint) would be a constructive approach to limit the short channel effects (SCE). The novel transistor has the potential to enable the scaling of gate length (footprint) less than 10 nm and contacted gate pitch below 32 nm, resulting in the smallest active area (on-wafer footprint) for a single device. Novel process steps are simulated depicting easier fabrication while the electrical analysis shows a better electrostatic control over any unwanted leakage flows. Along with the area scaling and SCE control, the planar upper surface allows a vertical integration. Growing another flipped device on top surface permits the designer to implement a logic circuit on a footprint of a single device, achieving ∼50% area gain further. TCAD based simulations were performed to design and characterize the performances of an individual device and the vertical inverter.

**INDEX TERMS** CMOS Logic, 5 nm Node, GAA-NWFET, UFET, 3D Integration, TCAD.

## I. INTRODUCTION

Size of the silicon transistor is continuously scaled in every generation to deliver the smaller and faster electronics technology [1]. Since last few decades, the trend of CMOS scaling was accelerated by many prime movers such as strained silicon and high-k/metal-gate technology [2]–[4]. However, while scaling down below 32 nm node, short channel effects (SCE), such as sub-threshold leakage become a major concern in planar MOS devices. Therefore, the planar MOSFET was replaced by a tri-gate architecture (FinFET) to improve the electrostatic control at the 22nm node [5]. Subsequently, the major industries followed the same FinFET based architecture for their 16/14nm, 10nm and 7nm node (N7) technology [6]–[11]. Aiming at the forthcoming sub-7nm node CMOS device, the critical key dimensions are predicted in Table-1. The expected contacted gate pitch (CGP) would be below 32nm for beyond 5nm node technology. This tighter CGP budgeting would lead the gate length scaling of less than 10nm. Even though the FinFET has gate wrapping around the channel providing better electrostatics, yet controlling the short channel effects at this shortest gate length would be a real big challenge.

Researchers are looking into Gate-All-Around (GAA) architectures, such as Nanowire (NW) /NanoSheet (NS) as the leading device structure for the 5nm node due to its superior electrostatics integrity than the FinFET [12], [13]. Although the NW with reduced diameter delivers best electrostatic control, the reduction of channel area reduces the current driving capability significantly. However, compromising electrostatics to some extent in GAA-NS device, drive currents are improved, yet the tighter constraint on width scaling doesn't allow a designer to scale down device

**TABLE 1.** Node to Node Scaling Target.

| Technology Node | N7 | N5 | N3 |
|---|---|---|---|
| Contacted Gate Pitch (CGP) (nm) | 42 | 32 | 24 |
| Metal Pitch(MP) (nm) | 32 | 24 | 18 |
| Gate Length ($L_g$) (nm) | 14 | 10 | 6 |

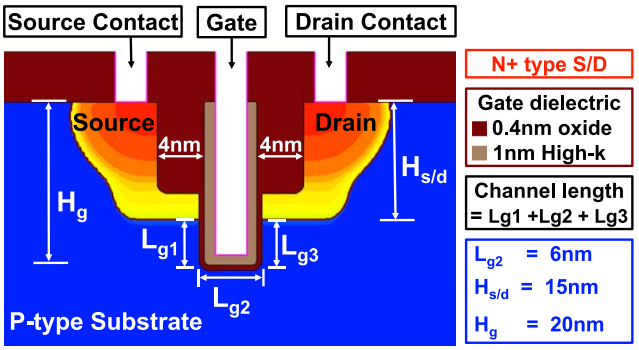


**FIGURE 1.** Cross-sectional view of the proposed UFET transistor having foot-print gate length of 6nm and trench depth of 20 nm.

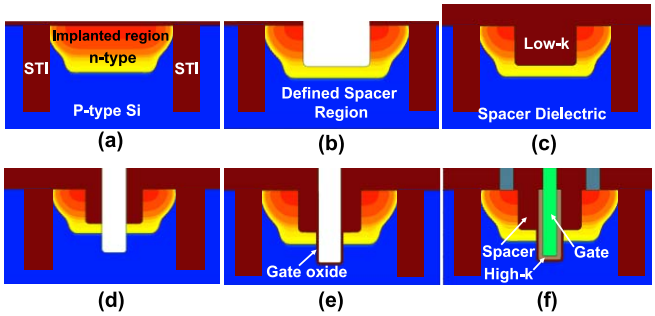


**FIGURE 2.** Novel process steps followed to make the UFET device.

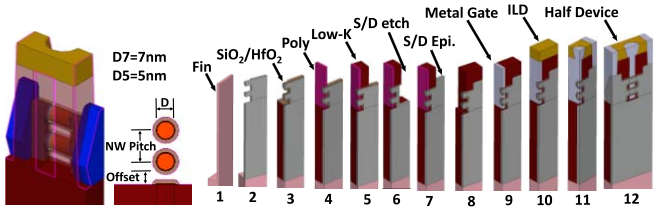


**FIGURE 3.** Process flow used to create two stacked GAA-NW transistor with epitaxial S/D contacts.

size further. Though drive current in GAA devices can be increased by stacking multiple wires/sheets per fin, but a taller fin device increases the process complexity and parasitic capacitances [14], [15].

In this study, an alternative device structure, a vertically integrated recessed channel transistor [16], with parasitic modifications is proposed as an alternative approach to continue the CMOS scaling. The cross-sectional view of the proposed nano-scale transistor is shown in Fig. 1. As the channel forms a U-shape inside the bulk, we referred this transistor as UFET.

Though recessed channel devices are already being used in DRAM cell [17], [18], and the U-shaped FET (V-shaped FET) are also being used in power semiconductor applications since last few decades [19]. We have studied the recessed channel planar device targeting the upcoming 5nm node and beyond logic technologies.

TCAD Sprocess [20] was used to implement the individual device structures and Sdevice [21] simulation with SRH, auger, BTBT recombination, bandgap narrowing, anisotropic density gradient, fixed interface charge, mobility model with multivalley correction, thin inversion layer correction with high-k dielectric, and quantum correction for the inversion layer were used to obtain electrical performances for both UFET and GAA-NW. Mixed-mode simulation was performed to obtain the characteristics of a vertically integrated inverter device.

## II. DEVICE SPECIFICATION AND PROCESS FLOW

The n-channel UFET transistor was built on a p-type bulk Si substrate considering the surface on {100} plane and sidewall surfaces along with the {110} plane. The source and drain regions were doped with n+ type active dopant atoms. The gate trench was considered of length 6nm and depth 20nm. The gate dielectric of 0.4nm oxide ($SiO_2$) and 1nm high-k ($HfO_2$) were used. The recessed gate was filled with the metal line considering proper work-function (WF). Gate to S/D spacers (low-k) were considered having a height of 6nm and length of 4nm. Silicide contacts similar to a planar MOSFET [4] were made at top of the source and drain regions which may provide a benefit of reducing the increased contact resistivity over epitaxial or wrap around contacts in GAA architecture. In this device, actual channel length would be the sum of $L_{g1} + L_{g2} + L_{g3}$. Other parameters of the n-channel UFET device are specified in Table 2.

**TABLE 2.** Specifications for n-Channel UFET Device.

| Parameters | Value | Unit |
|---|---|---|
| S/D doping ($N_d$) | $3 \times 10^{20}$ | $/cm^3$ |
| Channel doping ($N_a$) | $2 \times 10^{17}$ | $/cm^3$ |
| Effective oxide thickness (EOT) | 0.577 | nm |
| Drive Voltage ($V_{dd}$) | 0.6 | V |
| Targeted off state current ($I_{off}$_target) | $10 \times 10^{-9}$ | A/μm |

The recent development of advanced patterning techniques (EUV) has enabled the most critical process steps [22]. The novel process steps to fabricate the n-channel UFET device is described in Fig. 2. The p-type silicon substrate was patterned and implanted to define the active region (source, gate and drain region together) leading to the high-temperature activation at beginning of the process. Then, the center region of doped silicon was patterned and etched away for the S/D to gate spacers as shown in Fig. 2(b). Subsequently, the spacer material (low-k) was filled into the trench to minimize the S/D to gate overlap parasitic

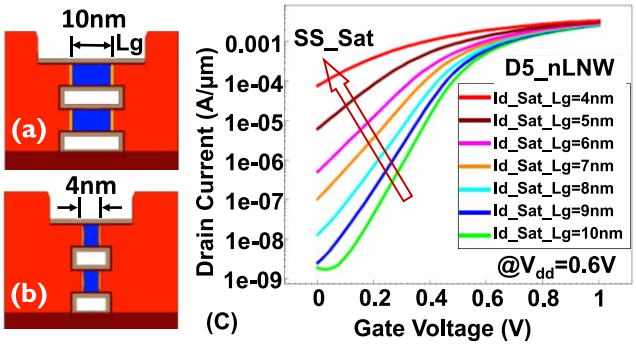


**FIGURE 4.** Deviation of sub-threshold currents while scaling the gate length from 10nm to 4nm for 5nm diameter (D5) based GAA-NW.

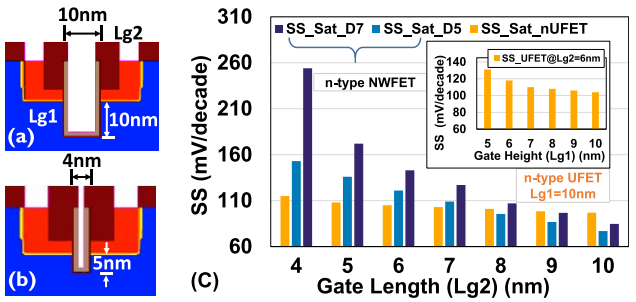


**FIGURE 5.** Comparisons of the Sub-threshold Slope (SS) of UFET and D7/D5 GAA-NW.

capacitance, as shown in Fig. 2(c). A narrow trench was then created by selectively removing the spacer dielectric and silicon underneath to open the gate region as shown in Fig. 2(d). After that, a thin conformal oxide covering was grown up for interface oxide layer. Finally, a high-k layer deposition followed by trench fill up with the gate material was performed. Narrow windows were created to make the contacts for source and drain terminal. The complete device is shown in Fig. 2(f). Similarly, the p-channel UFET transistor can be designed and processed on an n-type silicon substrate. In Fig. 3, we show the steps used of making GAA-NW device [23] with specifications similar to [15].

## III. ELECTRICAL PERFORMANCES OF UFET AND GAA-NW

While scaling down below 10nm gate length (Lg), a stronger gate control is merely achieved by a thinner diameter for GAA-NW's. Above all, at this dimension ballistic [24] flow is enabled significantly. In the UFET channel, the straight lines are also within 5nm to10nm, so the Lg1, Lg2 and Lg3 region might experience more ballistic conduction compared to the two corner regions, however, at corners the carrier will face more scattering as well as change the path direction leading to a more drift-diffusion conduction. Hence, more extensive studies are required to benchmark the ON state drive current in both the devices. At this point, a drift-diffusion based simulation model was used to analyze the sub-threshold characteristics. The obtained total current was normalized (by the width of UFET (W = 18nm) and the fin

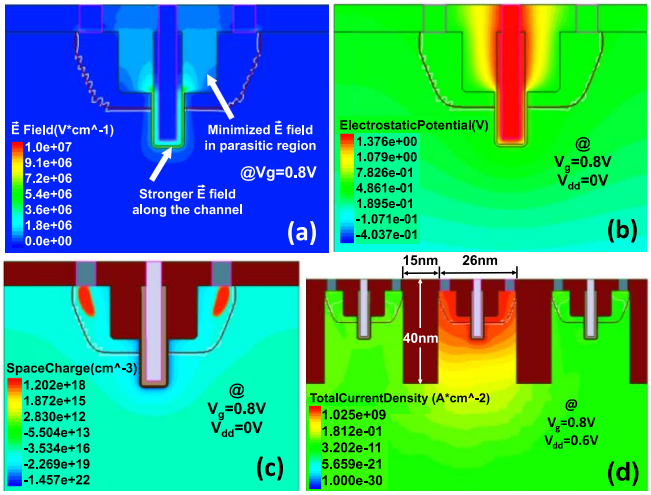


**FIGURE 6.** The electrical behavior in UFET: (a) Electric field distribution, (b) Spreading of Electrostatics potential, (c) Space Charges, and (d) STI isolation.

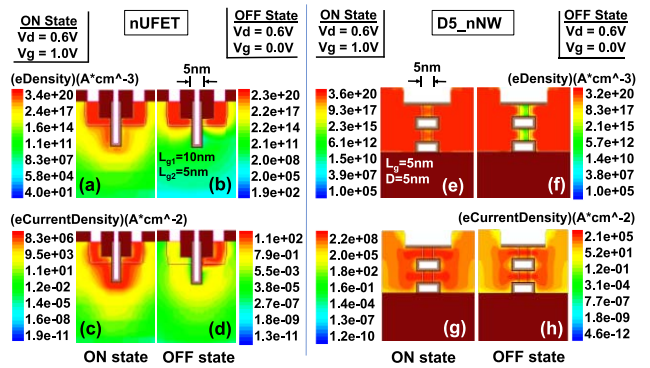


**FIGURE 7.** Carrier (electron) distributions in both the UFET and GAA-NW devices at a gate length of 5nm (footprint).

pitch of NW (FP = 18nm) and targeted at the same off-state current (10nA/μm).

Fig. 4(a) and 4(b) predicts gate length scaling of two stacked GAA-NW considering 5nm wire diameter (D5). Fig. 4(c) shows the degradation of sub-threshold slopes (SS) while reducing the gate lengths from 10nm to 4nm. The gate length scaling with the 7nm diameter (D7) based NW delivers even worst electrostatics. The Fig. 5(c), compares SS variations for both the D7/D5 NW and the UFET transistor. In D5 NW, SS degradation from ∼78mV/decade to ∼160mV/decade is observed whereas, in UFET transistor, an SS degradation of ∼87 mV/decade to ∼112mV/decade is witnessed. At the applied potential, the distribution of electric fields inside the bulk UFET is shown in Fig. 6(a). The densely distributed fields along the channel dielectric would form a strong inversion channel inside the bulk while minimized field distribution in the low-k spacer would help to shrink the S/D to gate overlap parasitics. The impact of electrostatic potential spread by the buried gate is shown in Fig. 6(b). Also, the distribution of space charge is illustrated in Fig. 6(c). As the device operates

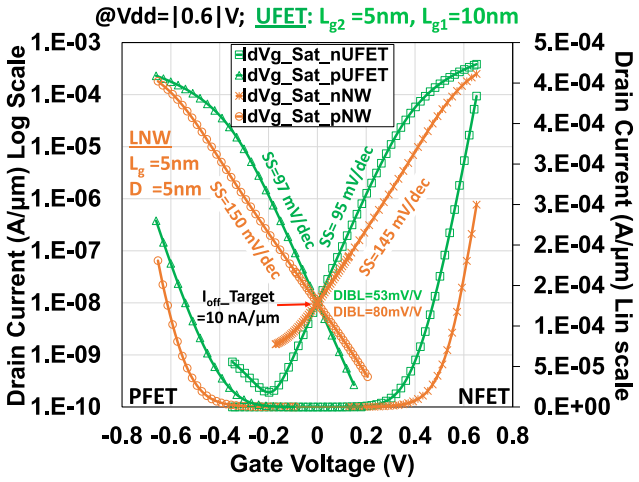


**FIGURE 8.** Saturation transfer characteristics compared for both the n-channel and the p-channel devices (UFET and GAA-NW FET).

**TABLE 3.** Electrostatics Comparison at the 5nm Foot-Print.

| Parameters | D7 NW | D5 NW | UFET |
|---|---|---|---|
| SS_Sat ( mV/decade) | 185 | 150 | 95 |
| DIBL (mV/V) | 110 | 80 | 53 |

inside bulk silicon, one of the big challenges would be isolation between two devices. Fig. 6(d) shows the carrier distributions in multiple devices while isolated by the STI.

At the shortest gate length ($L_g$ = 5nm in NW, $L_{g2}$ = 5nm in UFET), distribution of (carrier) electron and electron current densities are shown in Fig. 7 during the ON ($V_g$ = 1V, $V_{dd}$ = 0.6V) and OFF ($V_g$ = 0V, $V_{dd}$ = 0.6V) state condition. At high and low applied gate voltages, the peak electron current densities of $8.343\times10^6$A/cm$^2$ and $1.137\times10^2$A/cm$^2$ are observed in the UFET device, whereas electron current densities of $2.229\times10^8$A/cm$^2$ and $2.132\times10^5$A/cm$^2$ are observed in D5 NW. This provides an on-off current ratio of $10^4$ and $10^3$ for UFET and NW respectively. The transfer ($I_dV_g$) characteristics (at $V_{dd}$ = |0.6|V) for both UFET and GAA-NW are plotted in Fig. 8. Compared to GAA-NW, the UFET shows ~50mV/decade SS and ~25mV/V DIBL improvements in both the n-channel and p-channel devices. The Table 3 summarizes SS and DIBL values for the GAA-NW and UFET.

In UFET, the buried gate-dielectric layer physically isolates the source and drain region, resulting in an effective shading between the drain electric field and the source electric field. This isolation at an ultra-scaled device would play a major role in conserving the short channel effects (such as SS, DIBL etc.). Also, the impact of direct S/D tunneling between source and drain is expected to be minimal, thus less leakage flow from source to drain is expected. The gate length scaling reduces $L_{g2}$ part (foot-print gate length) of UFET's channel, continuing the area scaling, and maintaining larger physical channel length keeping the device capable of better off-state control.

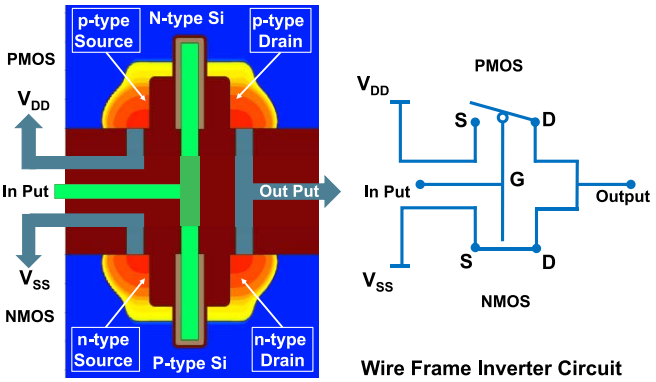


**FIGURE 9.** Proposal of Vertical Inverter shows the possibility of 50% area gain in scaling beyond the 3nm node.

## IV. VERTICAL LOGIC CELL DESIGN

The novel UFET device has some key advantages over other device configuration such as: possibly easier process steps and scalability. The advantage of having a planar upper surface can be used to process another flipped UFET transistor to continue the scaling beyond 3nm node. Fig. 9 shows the schematic design of the proposed novel inverter. Vertically integrated top and the bottom device will be acting as a pull-up and pull-down devices which can be fabricated on a single transistor area (same on-wafer footprint). Source terminal of bottom n-channel UFET is connected to the lower potential ($V_{ss}$) and source terminal of top p-channel UFET is connected to the higher potential ($V_{dd}$). Both the gate and the drain terminals are continuously connected. The input is applied to the commonly connected gate and the output is taken from the commonly connected drain. This

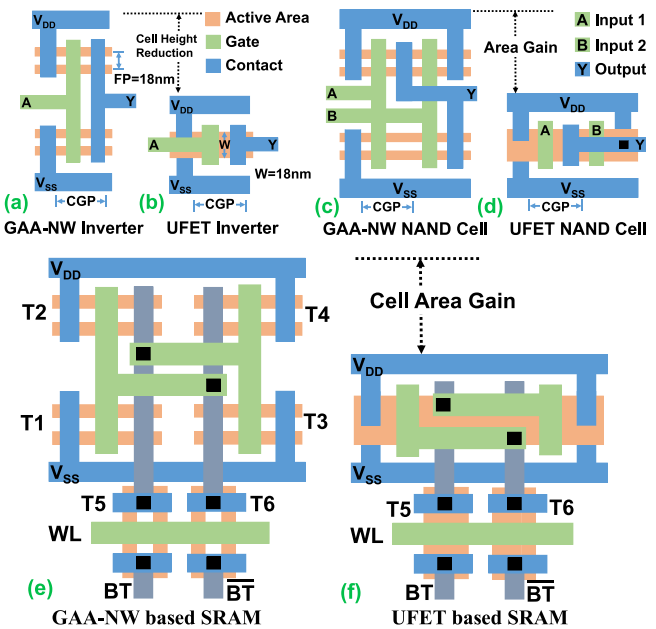


**FIGURE 10.** Layouts predicting an area gain while designing the vertical logic cell: (b) Basic Inverter, (d) NAND gate, and (f) SRAM cell.

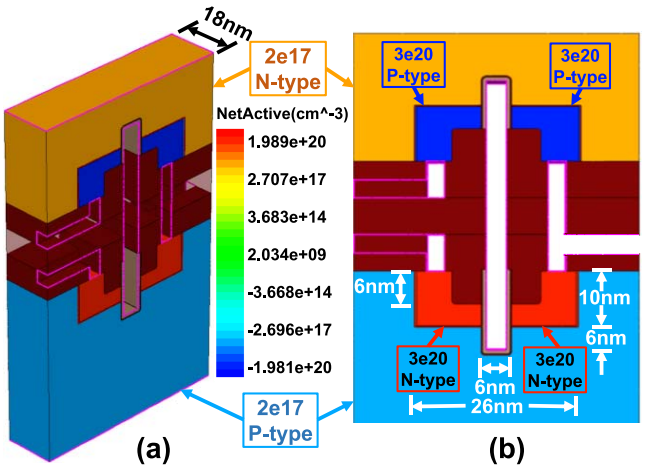


**FIGURE 11.** A simulated inverter: (a) Full 3D view, and (b) Cross-sectional 2D view showing all major device dimensions.

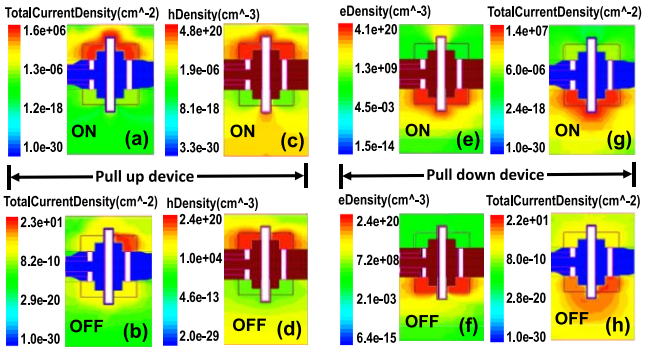


**FIGURE 12.** Simulated results showing distributions of majority carrier in both the pull up and the pull down devices at ON and OFF state condition.

approach will provide a significant area gain (Fig. 10(b)) especially for the beyond 5nm node when the footprint ($L_g$) scaling would be limited by the gate trench fill process. Continuing with this vertical design, the layout schematic in Fig. 10(d) and Fig. 10(f) shows cell height reduction in 4T NAND cell and in 6T SRAM cell. The layouts show in this paper are simplistic and area calculation will change considering the impact of contacts, isolation etc. on the actual layout design. Similar to this logic cell, other true logic gates such as transmission gate and pass gate can also be designed.

Current development of monolithic 3D integration has enabled a new direction of CMOS integration. The vertical stacking [25]–[27] along with many technological breakthroughs in TSV [28] and ultra-thin FDSOI [29], [30] process, would help to accomplish the proposed UFET based vertical integration. Novel vertical design with two transistor inverter is simulated using the Sentaurus-Device. Specifying all the major dimensions, the 3D schematic inverter is shown in Fig. 11. The footprint gate length of 6nm and trench depth of 16nm is considered, in where the CGP is scaled down to less than 24nm.

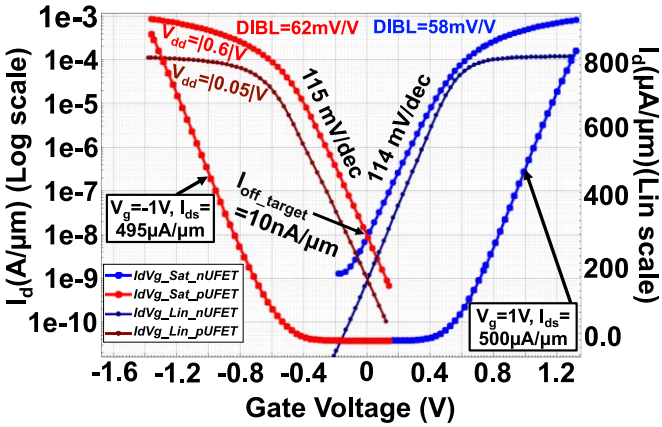


**FIGURE 13.** The transfer characteristics ($I_dV_g$) for both the pull-up and pull down UFET.

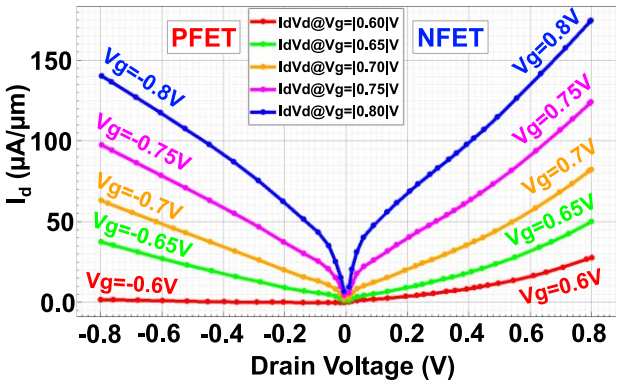


**FIGURE 14.** Output characteristics ($I_dV_g$) for both the n-channel and p-channel UFET.

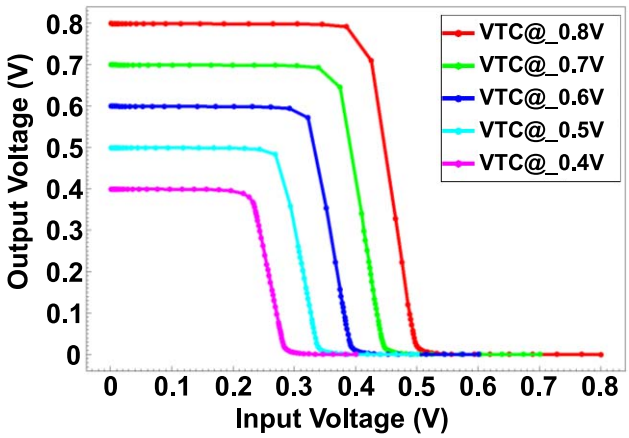


**FIGURE 15.** The voltage transfer characteristics (VTC) of proposed vertical inverter at different drive voltages.

While analyzing the electrical behavior of this compact inverter, the distributions of majority carriers during ON and OFF state condition are shown in Fig. 12. Although the applied potential at continuously connected gate terminal may influence the opposite device, the lower potential at source/drain will mitigate the impact, similar to the

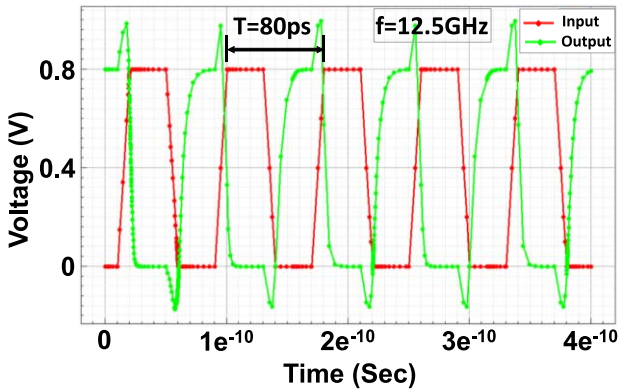


**FIGURE 16.** **Transient behavior of the vertical inverter with a pulsed input signal.**

planar MOSFET based circuit design. The transfer ($I_dV_g$) and output ($I_dV_d$) characteristics for both the pull-up and pull-down devices are plotted in Fig. 13 and in Fig. 14. Sound transition of voltage transfer characteristics (VTC) for the inverter operation even at a lower operating voltage of 0.4V is shown in Fig. 15. Along with a sharper VTC, the transient output (Fig. 16) predicts a proper inverter circuit.

In order to investigate the full AC behavior of this device, detailed studies are required. The proposed novel device can be a potential candidate for scaling the 3nm node and beyond CMOS transistors. At current situation, there is a very limited space to scale down the device size further in lateral direction, hence this vertical integration enables a novel trend of CMOS scaling for the next generation technology.

## V. CONCLUSION

An alternative device architecture has been presented in this paper for the future trend of CMOS scaling. Using a recessed channel UFET architecture, the CGP can be scaled down to 24nm, leading to a transistor where scaling in size and lowering the leakage might be achieved together. The advantage of having a flat surface in UFET enables the vertical integration of an inverter. Finally, the vertical logic gate has the possibility of achieving significant (∼50%) area gain for ultimate scaling of CMOS technology.

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