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High-Performance LPCVD-SiN_x/InAlGaN/GaN MIS-HEMTs With 850-V 0.98-mΩ·cm^2 for Power Device Applications

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ABSTRACT We demonstrate the electrical performances of the quaternary InAlGaN/GaN MIS-HEMTs with high quality SiN_x gate dielectric and surface passivation layer deposited by low pressure chemical vapor deposition (LPCVD) at 780 °C. Excellent LPCVD-SiN_x/InAlGaN interface and SiN_x film quality were obtained, resulting in very high output current density, a very small threshold voltage hysteresis and steep subthreshold slope. The LPCVD-SiN_x/InAlGaN/GaN MIS-HEMT device exhibited high on/off current ratio, large gate voltage swing, high breakdown voltage, and very low dynamic on-resistance (R_{ON}) degradation, meaning effective current collapse suppression compared to the plasma enhanced chemical vapor deposition -SiN_x/InAlGaN/GaN MIS-HEMTs. The corresponding specific on-resistance ($R_{ON,sp}$) for LPCVD-SiN_x device was as low as 0.98 mΩ·cm^2, yielding a high figure of merit of 737 MW/cm^2. These results demonstrate a great potential of the LPCVD-SiN_x/InAlGaN/GaN MIS-HEMTs for high-power switching applications.

INDEX TERMS InAlGaN/GaN, MIS-HEMT, LPCVD, SiN_x, figure of merit.

I. INTRODUCTION

InAlGaN/GaN high electron mobility transistors (HEMTs) have attracted much attention owing to the combination of AlGaN and InAlN to form a quaternary barrier layer (InAlGaN), which provides a narrower immiscibility gap. High electron mobility and high two-dimension electron gas (2DEG) density in the channel were obtained due to much stronger spontaneous polarization and ultrathin barrier layer [1]–[3]. Therefore, lattice-matched InAlGaN barrier HEMTs have been extensively studied as alternatives to the conventional AlGaN/GaN HEMTs for RF and millimeter-wave power applications [4]–[6].

Despite the excellent properties, excessive gate leakage current remains a challenge for the development of InAlGaN/GaN HEMTs due to the strong polarization-induced electric field in the InAlGaN barrier [7]–[9]. The high gate leakage degrades the output power efficiency and the breakdown voltage of the devices. In addition, the current collapse increases the dynamic ON-resistance (R_{ON}), which leads to the potential instability of the devices. Thus, the high quality gate dielectric and effective surface passivation become important issues for GaN power devices.

Silicon nitride films deposited by plasma enhanced chemical vapor deposition (PECVD) [10], plasma enhanced atomic layer deposition (PEALD) [11] or *in-situ* grown by metal-organic chemical vapor deposition (MOCVD) [12] have been widely used as the gate dielectrics for the GaN MIS-HEMTs. Recently, several studies report that the high quality SiN_x film grown by low pressure chemical vapor deposition (LPCVD) at high deposition temperature (>600 °C) is free of plasma-induced damages and can be used as gate dielectric and passivation layer for GaN HEMT devices since the LPCVD-SiN_x film has high thermal stability and excellent electric strength [13]–[17].

In this study, we use LPCVD-SiN_x film as gate dielectric and passivation layer prior-to-ohmic process for the InAlGaN/GaN MIS-HEMTs fabrication. The performances of these devices are compared to the performances of the InAlGaN/GaN MIS-HEMT devices with PECVD-SiN_x passivation films.

II. DEVICE FABRICATION

The quaternary InAlGaN/GaN heterostructure was grown by MOCVD on a sapphire substrate. Trimethylindium (TMIn), trimethylaluminum (TMAl), trimethylgallium (TMGa), and ammonia (NH_3) were used as the precursors for In, Al, Ga, and N, respectively. The epitaxial structure consisted of a 4-nm InAlGaN barrier layer, a 1-nm AlN spacer, a 2.5-μm Fe-doped GaN buffer layer, and a 120-nm AlN nucleation layer. Hall measurements at room temperature revealed a 2DEG sheet charge density of 1.7×10^{13} cm^{-2} and an electron mobility of 1600 cm^2/V·s, resulting in a sheet resistance of 210 Ω/square.

LPCVD-SiN_x layer was deposited on the wafer first before the ohmic and gate metal depositions for the MIS-HEMT fabrication. Prior to the device fabrication, the epitaxial wafer was cleaned by a standard RCA treatment and subsequently loaded into the LPCVD chamber. A 20-nm LPCVD-SiN_x film was deposited as the gate dielectric and passivation layer at the temperature of 780 °C and the pressure of 180 mTorr with a dichlorosilane (SiH_2Cl_2) flow of 67 sccm and an ammonia (NH_3) flow of 200 sccm, yielding a deposition rate of 4 nm/min. After ICP dry etching of the LPCVD-SiN_x film in the source and drain contact regions, Ti/Al/Ni/Au (20/120/25/100 nm) ohmic contact was formed by the electron beam evaporation and lift-off process, followed by rapid thermal annealing (RTA) at 850 °C for 30 s in N_2 ambient. The contact resistance was 0.45 Ω·mm as extracted by the transfer length method (TLM). Planar device isolation was achieved by multi-energy nitrogen ion implantation. The gate electrode was formed by depositing Ni/Au (50/300 nm) and lift-off process. The InAlGaN/GaN MIS-HEMTs with 20-nm PECVD-SiN_x gate dielectric were also fabricated on the same epitaxial wafer for performance comparison. The PECVD-SiN_x was deposited at the temperature of 300 °C after ohmic contact formation. A dilute HF (1:10) wet cleaning and an *in-situ* N_2 plasma pretreatment were performed before the PECVD-SiN_x gate dielectric deposition [10], [18].

Fig. 1(a) shows the cross-sectional view of the fabricated InAlGaN/GaN MIS-HEMT. The gate-to-drain spacing L_{GD}, gate-to-source spacing L_{GS}, gate length L_G, and gate width W_G were 15 μm, 3 μm, 2 μm, and 25 μm, respectively.

III. RESULT AND DISCUSSION

The surface morphology of the quaternary InAlGaN/GaN heterostructure was characterized by atomic force microscopy (AFM) over a 5 × 5 μm^2 scan region, as shown in Fig. 1(b). The atomic steps were observed on the InAlGaN surface [5] and the root-mean-square (RMS) roughness was 0.35 nm with no surface pits, indicating high quality of InAlGaN barrier layer.

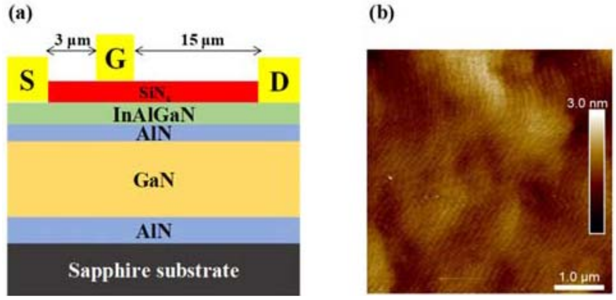

FIGURE 1. (a) Schematic cross-sectional view of the InAlGaN/GaN MIS-HEMT with 20-nm SiN_x as gate insulator. (b) AFM image of the surface morphology of the InAlGaN/GaN film. The scan area is 5 × 5μm^2.

TABLE 1. Characteristics of InAlGaN/GaN Structure After Different Surface Passivation.

Passivation	w/o	PECVD-SiN_x	LPCVD-SiN_x
R_{SH} (Ω/sq.)	210	227	194
μ (cm^2/V·s)	1600	1620	1650

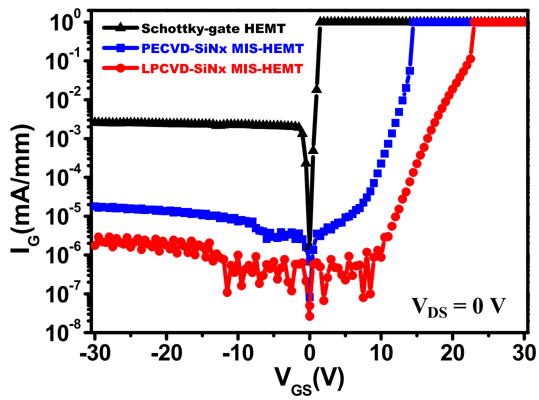

FIGURE 2. Gate leakage current of the Schottky-gate InAlGaN/GaN HEMT, PECVD-SiN_x/InAlGaN/GaN MIS-HEMTs and LPCVD-SiN_x/InAlGaN/GaN MIS-HEMTs.

The influences of PECVD-SiN_x passivation and LPCVD-SiN_x passivation on the sheet resistance (R_{SH}) and mobility (μ) of InAlGaN/GaN structure were investigated. Table 1 lists the characteristics of InAlGaN/GaN structure after different surface passivation. For the InAlGaN/GaN structure with LPCVD-SiN_x passivation, both the R_{SH} and μ were improved, proving the benefits of LPCVD-SiN_x passivation for InAlGaN/GaN structure.

Fig. 2 compares the gate leakage currents under both reverse and forward gate biases for the Schottky-gate InAlGaN/GaN HEMT, PECVD-SiN_x/InAlGaN/GaN MIS-HEMTs and LPCVD-SiN_x/InAlGaN/GaN MIS-HEMTs. As results, MIS-HEMTs exhibited great effects on suppressing leakage current, compared with Schottky-gate

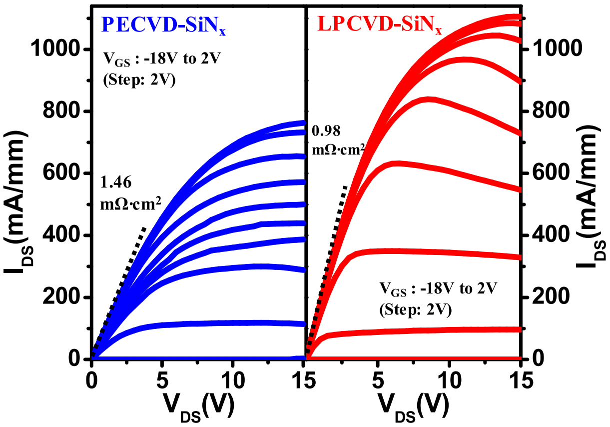

FIGURE 3. DC characteristics of the PECVD-SiN$_X$/InAlGaN/GaN MIS-HEMTs and LPCVD-SiN$_X$/InAlGaN/GaN MIS-HEMTs.

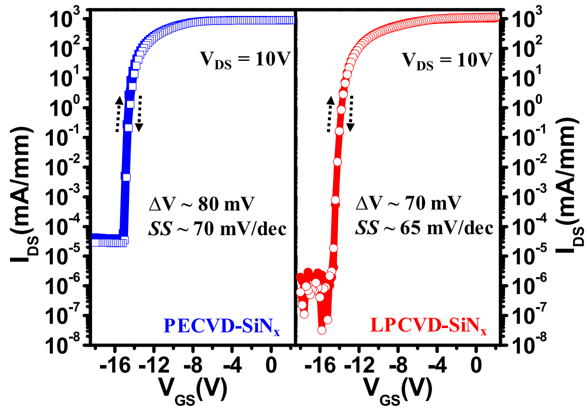

FIGURE 4. Transfer characteristics of the PECVD-SiN$_X$/InAlGaN/GaN MIS-HEMTs and LPCVD-SiN$_X$/InAlGaN/GaN MIS-HEMTs.

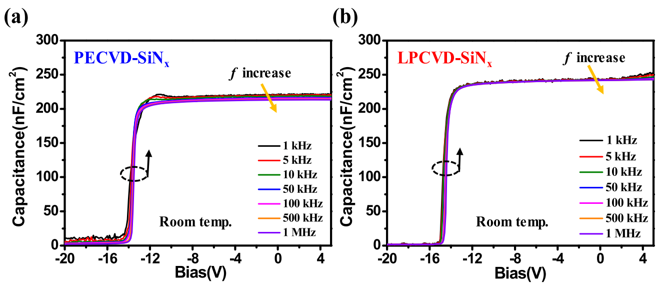

FIGURE 5. ***C-V*** characteristics of (a) the PECVD-SiN$_X$/InAlGaN/GaN MIS diode and (b) the LPCVD-SiN$_X$/InAlGaN/GaN MIS diode with frequencies varying from 1 kHz to 1 MHz.

HEMTs. Especially, LPCVD-SiN$_x$ MIS-HEMTs showed more reduction in the gate leakage current at both reverse ($I_G \sim 2 \times 10^{-6}$ mA/mm at $V_{GS} = -30$ V) and forward ($I_G \sim 8.7 \times 10^{-7}$ mA/mm at $V_{GS} = 10$ V) bias regions, which is mainly due to the larger barrier height. Besides, the forward gate breakdown voltage of LPCVD-SiN$_x$ MIS-HEMTs was 23.5 V, indicating that LPCVD-SiN$_x$ has better quality and higher electric field strength compared to the PECVD-SiN$_x$ [19].

Fig. 3 shows the DC output characteristics of the PECVD-SiN$_x$/InAlGaN/GaN MIS-HEMTs and LPCVD-SiN$_x$/ InAlGaN/GaN MIS-HEMTs. The devices with LPCVD-SiN$_x$ gate dielectric exhibited a much higher $I_{DS,max}$ of 1.1 A/mm with a lower specific ON-resistance ($R_{ON,sp}$) of 0.98 mΩ·cm^2. The specific ON-resistance is determined using the following equation: $R_{ON,sp} = R_{ON} \times W_G (L_{SD} + 2 \times 1.5 \mu m)$, where R_{ON} is extracted at a current level of 200 mA/mm when $V_{GS} = 2$ V from the output curves, W_G is gate width, and L_{SD} is source-drain spacing. The transfer length for each ohmic contact is 1.5 μm for calculating the device effective active area. This performance is much better than the MIS-HEMTs with PECVD-SiN$_x$ gate dielectric ($I_{DS,max} = 760$ mA/mm and $R_{ON,sp} = 1.46$ mΩ·cm^2).

Fig. 4 shows the transfer characteristics of the fabricated devices in the semilog scale with V_{DS} of 10 V, where the gate voltage was up-sweep from −18 V to 2 V and down-sweep from 2 V to −18 V. The LPCVD-SiN$_x$ devices exhibit very small threshold hysteresis (ΔV_{TH}) of ∼70 mV, low sub-threshold slope (*SS*) of ∼65 mV/dec and high I_{ON}/I_{OFF} ratio in the order of $\sim 10^9$, suggesting that LPCVD-SiN$_x$/InAlGaN has better interface quality and lower leakage due to the LPCVD-SiN$_x$ gate dielectric. These performances are also much better than the reported AlGaN/GaN and InAlN/GaN device data. Further improvement could be achieved by using *in-situ* pre-deposition plasma nitridation process for the LPCVD-SiN$_x$ deposition [17].

To investigate the PECVD-SiN$_x$/InAlGaN and LPCVD-SiN$_x$/InAlGaN interface quality, capacitance-voltage (*C-V*) measurements were performed on the MIS diode with different frequencies varying from 1 kHz to 1 MHz at room temperature, as shown in Fig. 5 (a) and (b). In Fig. 5 (b), a smaller frequency dispersion and a steeper *C-V* curve for LPCVD-SiN$_x$/InAlGaN/GaN MIS diode can be observed, indicating the gate dielectric/barrier layer interface has low interface trap density.

The dynamic R_{ON} is generally used to examine the trapping effects caused by the surface and interface states in the GaN device structure. Therefore, the dynamic R_{ON} can be used to investigate the effectiveness of the passivation. The measurement setup is similar to the previous report [20]. The Agilent B1505A power device analyzer system was used to investigate the dynamic switching characteristics of the InAlGaN/GaN MIS-HEMT devices with high drain voltage. First, the device was turned off with 3s hold time at stress voltage (V_{stress}), while the gate bias was set at $V_{GS} = -18$ V. Then, the device was turned ON at $V_{GS} = 1$ V and $V_{DS} = 1$ V. The ON-state resistance was sampled at the end of 0.1 s to calculate the dynamic R_{ON}. The switching time was set to be 20 μs by Agilent High Voltage / High Current Switch component. As results shown in Fig. 6, the two samples exhibited similar dynamic R_{ON} when the OFF-state drain bias stress (V_{stress}) was below 120 V; however, they started to show large difference when the V_{stress} exceeded 120 V. The dynamic R_{ON} increased only 1.34 times at the V_{stress} of 400 V for the LPCVD-SiN$_x$ MIS-HEMT device,

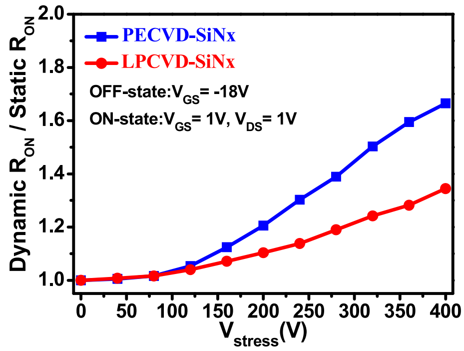

FIGURE 6. The normalized dynamic R_{ON} of PECVD-SiN_x/InAlGaN/GaN MIS-HEMTs and LPCVD-SiN_x/InAlGaN/GaN MIS-HEMTs with OFF-state drain bias stress voltage (V_{stress}) up to 400 V.

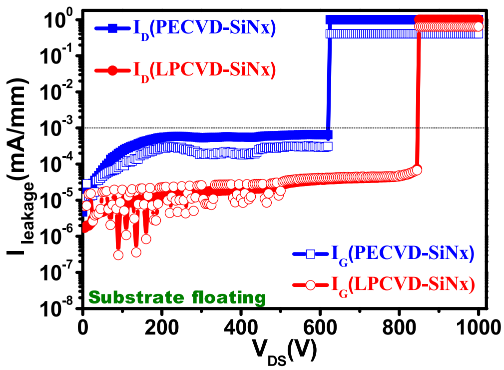

FIGURE 7. Three terminal OFF-state breakdown characteristics of the PECVD-SiN_x/InAlGaN/GaN MIS-HEMTs and LPCVD-SiN_x/InAlGaN/GaN MIS-HEMTs.

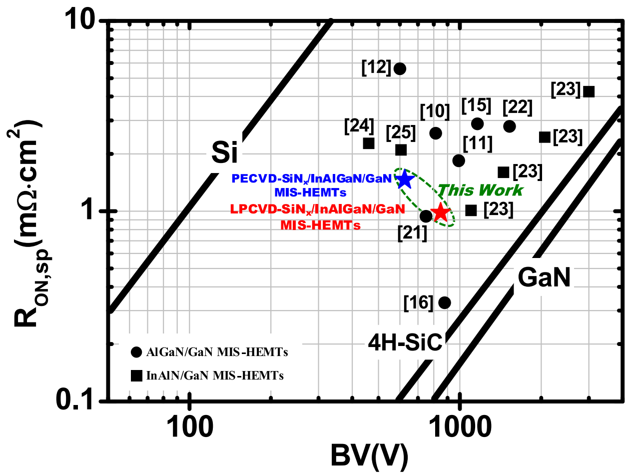

FIGURE 8. Benchmark of specific ON-resistance and breakdown voltage for GaN-based MIS-HEMTs with different barrier layers. The star marked data represent the fabricated PECVD-SiN_x/InAlGaN/GaN MIS-HEMTs and LPCVD-SiN_x/InAlGaN/GaN MIS-HEMTs with L_{GD} = 15 μm in this study.

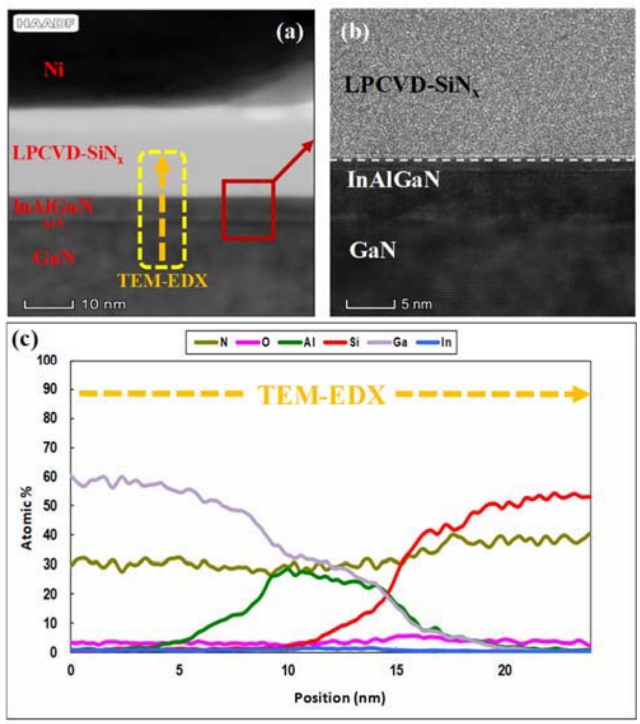

FIGURE 9. (a) Cross-section HAADF-STEM of the LPCVD-SiN_x/InAlGaN/GaN MIS-HEMTs in the gate region. (b) Cross-section TEM micrograph of the LPCVD-SiN_x/InAlGaN/GaN interface marked in the red square of (a). (c) Corresponding TEM-EDX line scan of the LPCVD-SiN_x/InAlGaN/GaN interface.

suggesting that the high quality of gate dielectric and passivation layer can effectively suppress the current collapse.

The three-terminal OFF-state breakdown characteristics of the fabricated InAlGaN/GaN MIS-HEMTs are shown in Fig. 7. It can be observed that the breakdown voltage (BV) improved and the leakage current was lower for the device with LPCVD-SiN_x film compared to the device with PECVD-SiN_x film. For the LPCVD-SiN_x MIS-HEMTs device, the BV of 850 V at a leakage current of 1 μA/mm was achieved, yielding a high figure of merit (FOM) = $BV^2/R_{ON,sp}$ of 737 MW/cm^2. In Fig. 8, the specific ON-resistance versus breakdown voltage data of the PECVD-SiN_x passivated and LPCVD-SiN_x passivated MIS-HEMTs devices were plotted and benchmarked with other reported AlGaN/GaN MIS-HEMTs and InAlN/GaN MIS-HEMTs data. It can be clearly observed that the fabricated LPCVD-SiN_x/InAlGaN/GaN MIS-HEMTs with L_{GD} = 15 μm exhibited much better performances than other reported GaN MIS-HEMT devices.

The microstructure of the LPCVD-SiN_x/InAlGaN/GaN MIS-HEMT is characterized with high-resolution transmission electron microscopy (TEM). The high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image in Fig. 9(a) shows the cross section of LPCVD-SiN_x/InAlGaN/GaN MIS-HEMTs in the gate region. From this micrograph, we can confirm that the thickness of LPCVD-SiN_x, InAlGaN barrier layer, and AlN spacer were 20 nm, 4 nm, and 1 nm, respectively. Fig. 9(b) shows the TEM micrograph of the LPCVD-SiN_x/InAlGaN/GaN stack, and a sharp interface between the LPCVD-SiN_x and InAlGaN barrier layer has been obtained. In addition, the continuous crystalline structure maintains well-ordered without obvious defects at the LPCVD-SiN_x/InAlGaN interface, indicating LPCVD-SiN_x passivates the dangling bonds on InAlGaN surface [26]. The energy dispersive x-ray spectroscopy (EDX) line scan was performed across the LPCVD-SiN_x/InAlGaN/GaN interface, as shown in Fig. 9(c). The composition of oxygen-contaminated at the LPCVD-SiN_x/InAlGaN interface is revealed to be less than 5%, indicating the InAlGaN surface was effectively protected by LPCVD-SiN_x during the critical processes such as ohmic contact annealing [14].

IV. CONCLUSION

The LPCVD-SiN_x/InAlGaN/GaN MIS-HEMT device fabricated in this study shows a remarkable enhancement on the electrical performances compared to the InAlGaN/GaN MIS-HEMT with conventional PECVD-SiN_x passivation. Besides, the performance of LPCVD-SiN_x device is also much better than that reported data of AlGaN/GaN or InAlN/GaN devices. Excellent bulk and interface properties of the LPCVD-SiN_x film were achieved, resulting in high drain current density and a very small threshold voltage hysteresis for the devices. The fabricated LPCVD-SiN_x MIS-HEMTs exhibited improvements in on/off current ratio, leakage current, gate voltage swing, breakdown voltage, and dynamic R_{ON}. Thus, the LPCVD-SiN_x/InAlGaN/GaN MIS-HEMTs are extremely promising for the new generation of power electronic applications.

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