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Vacuum Nano-Triode in Nothing-On-Insulator Configuration Working in Terahertz Domain

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ABSTRACT This paper presents for the first time a new configuration of the nothing on insulator (NOI) structure: a vacuum NOI-triode. The main novelty of the new structure consists in the gate that is now part of the vacuum region as in conventional triodes. Each NOI-triode is introduced by a technological plan, followed by the concept validation and characteristics analysis. On the other hand, these NOI-triodes evolve from the NOI-transistor configuration. Consequently, some specific parameters to transistors are improved and permanently compared to some fabricated vacuum nano-transistors that are proposed in literature. For instance, the sub-threshold swing is suddenly decreased from 0.65. . .4 V/dec to 0.090 V/dec. A low swing is responsible to a high cutoff frequency. The paid price for the NOI-triode is a non-null gate current. To preserve the gained advantages and to keep as low as possible the I_{Gate}/I_{Anode} ratio, a special work regime must be selected. This paper devotes a large static and dynamic analysis to find the convenient work regime and possible technological solutions. The drive voltages can be decreased to 1 V, I_{ON} current of micro-amperes and excellent I_{OFF} current of atto-amperes. The internal capacitances of 0.9 aF recommend the NOI-triodes to 0.35 ... 4 THz working regime.

INDEX TERMS Nano-scale triode, THz device, vacuum tunneling, simulations.

I. INTRODUCTION

The electron transport in vacuum is used in vacuum tubes [1] or in newer integrated semiconductor devices [2], [3]. In vacuum, the carriers travel faster, without frictions in solid-state materials, offering high-power electronics [3], high-speed [4], and high-frequency operation regime [4]–[7]. In 1999 Park *et al.* [2] proposed a lateral field emitter triode with 500nm thick n^+ doped polysilicon as cathode material, using a SOI substrate. The electrical characteristics were: anodic turn-on voltage of 14V, an emission current of 92μA, a gate leakage current ratio ($I_A/I_G>400$) and a transconductance of 57μS. In 2008 Subramanian *et al.* [3] developed a vacuum transistor with nanodiamond emitter, 500μm anode-cathode distance, with a gate turn-on voltage of 40V, anode current of 1.1μA, less than 0.001% gate current, transconductance of 22nS/finger and a saturation anodic voltage of 210V. In recent years, a triode based on a Si-film of 50nm thickness, using 1μm anode-cathode distance, reduced the gate operation voltage up to 0.5 . . . 1.7V, while the saturation occurred at 30 . . . 40V, [8].

Pushing the vacuum devices towards co-planar technology [9], some MOSFET parameters find their dual meaning in vacuum device, like *sub-threshold swing* SS - a key switching parameter, the *threshold gate voltage*, V_T that allows the OFF - ON states transition or the *cutoff frequency*, f_T. From 2005, a vacuum nano-transistor known as Nothing On Insulator (NOI), has been continuously optimized, [10]–[14]. The NOI-transistor with size sub-50nm presents less than 20V operation voltages [12] and poor *gate swing* SS = 5 . . . 1V/dec, [13].

The related devices are: (i) a field-effect transistor as MOS capacitor with an ITO intermediate gate metal, [5]; here the vacuum channel was fabricated by focused-ion-beam etching; however, the anodic current is given by the electrons transport within the lateral vacuum channel, plus the tunneling current thru the MOS oxide and suffers from high gate current; (ii) a gate-insulated vacuum transistor with

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10nm vacuum gap, fabricated by the standard silicon technology, [9]; here the threshold voltage was $V_T = 8.8V$ and the sub-threshold swing was SS = 4.2V/dec, [9]; (iii) an optimized vacuum transistor with cylindrical gate developed by the same NASA group of Han and collaborators, [6]. These authors claim that this class of transistors made by "Nothing" cover the terahertz gap of 0.1-10THz spectrum [15], which is not well served by the traditional semiconductor devices, [16]. This high frequency operation regime is directly linked to the ON/OFF switching speed that means a sub-threshold swing, SS, as low as possible.

Recent studies found out a swing SS = 650mV/dec for a rectangular NOI-transistor made in Si [14] and 260mV/dec, only if the NOI-transistor gets a narrow shape [17]. So, the main objective of this paper is to conserve a rectangular shape - suitable for a realistic Si-technology and to suddenly reduce the *gate swing, SS,* by a new NOI structure. In this sense, the metallic gate is middle placed, so that the NOI device is changed, for the first time, into a vacuum NOI-triode, Fig. 1. The gate electrode can be deposited as thin film onto oxide, (full lines in Fig. 1) and can be back-side contacted by an extension that trickles to the substrate (dotted lines in Fig. 1). For the NOI-triode, the paid price of the SS lowering is a non-null gate current. But this is inherent in any triode, [1]–[3]. To be in agreement with the vacuum device terminology, the source - drain electrodes are renamed, as cathode - anode, respectively.

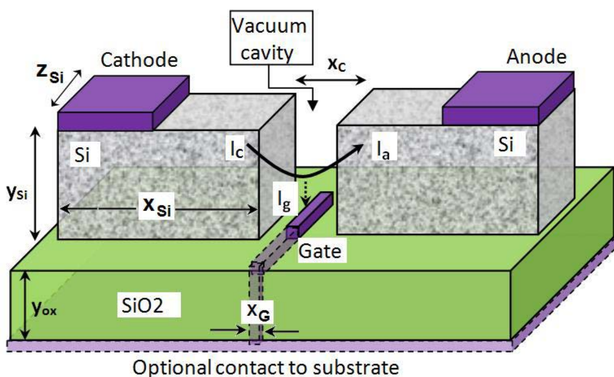

FIGURE 1. **The principle of the vacuum NOI-nano-triode.**

In Fig. 1, the length, thickness and depth are measured respectively on Ox, Oy and Oz axis. All the geometrical notations are suggested in Fig. 1. For instance x_{Si} is the Si-island length, x_C is the vacuum cavity length, y_{Si} is the Si-island thickness and z_{Si} is the Si-island depth.

The paper is structured as: the II-nd section is dedicated to the simulation of a NOI-triode1 structure with higher sizes and 14nm gap, having in mind a realistic technological plan for the nowadays facilities; the III-rd section is dedicated to an avant-garde NOI-triode2 structure with 3nm gap that reaches SS = 90mV/dec; here a planar technology is drafted; the IV-th section approaches some dynamic aspects; the V-th section summarizes the NOI-triode features and briefly discusses some comparisons; the VI-th section is devoted to conclusions. The technological simulations of all NOI-triodes are performed by ATHENA tool from Silvaco, while the functional simulations are performed by ATLAS from Silvaco, which are usual tools of the microelectronics industry.

II. THE NOI-TRIODE-1 VARIANT

A. CONCEPT AND SIMULATION SET-UP

The selection of a NOI-triode architecture balances between a realistic Si-technology and prior NOI device features. Firstly, to be closer to the actual nowadays technological processes, a NOI-triode1 structure with global sizes of 100nm × 80nm × 50nm and $x_C = 14$nm gap length, is presented. Secondly, in the next Section III, a smaller NOI-triode2 structure, with similar sizes to a NOI-transistor [13], [14], is analyzed.

From previous studies [11]–[14], a bottom oxide of $y_{ox} = 10$nm is thick enough to isolate the top active device. Over oxide, the cathode/anode n^+-type film can be configured as a Silicon On Insulator (SOI) layer of $y_{Si} = 50$nm thickness and $x_{Si} = 43$nm length, with 7×10^{20} uniform doping concentration, [12]–[14], [18]. The prior simulations have shown a minimal influence of the fixed interface charge, Q_F [11]. So, an average value $Q_F = 7 \times 10^{10}$e/cm^2 is considered, only to be connected to real conditions. Cathode, anode and gate contacts are Al to ensure ohmic contacts. A Tamm states density of 10^{12}cm^{-2} is activated by the Heiman model in the INTTRAP statement, [19], to include as real as possible the Si-surface properties.

Beneath the Si-islands there is an etched gap in nitride of $x_N = 20$nm and $y_N = 10$nm to allow a better positioning of the gate electrode. As a main novelty of this paper, the gate position confers a *triode* set-up. The gate metal is deposited in the middle of the cavity, so that the gate fulfills the role of a grille from a vacuum tube, [1]–[3] and consequently allows a leakage current through itself. For the NOI-triode1 structure, the thickness of the gate electrode over the oxide is $y_G = 3$nm and the lateral length is $x_G = 10$nm, Fig. 2.

B. TECHNOLOGICAL DISCUSSIONS

This paragraph proposes a technological flow that is based on the Si-technology from Athena/Silvaco. An actual process, able to produce few nm thin films is ADL technique, [20]. But the critical point in this device is not the thickness, but the lateral dimensions. A gap 3nm wide and a conducting gate metal 1nm wide that are considered for the conceptual NOI-triode2 variant are possible only by a future nano-lithography resolution, [21]. Therefore, the selected sizes for the NOI-triode1 variant appeal to a gate metal 10nm wide and 3nm thickness. These metallic traces and etching resolutions are possible in the nowadays VLSI integrated circuits [22], [23].

The technological process of the NOI-triode1 variant starts in Athena from an oxide substrate of 10nm thickness. On this surface, Al of 3nm thickness is deposited through a mask of

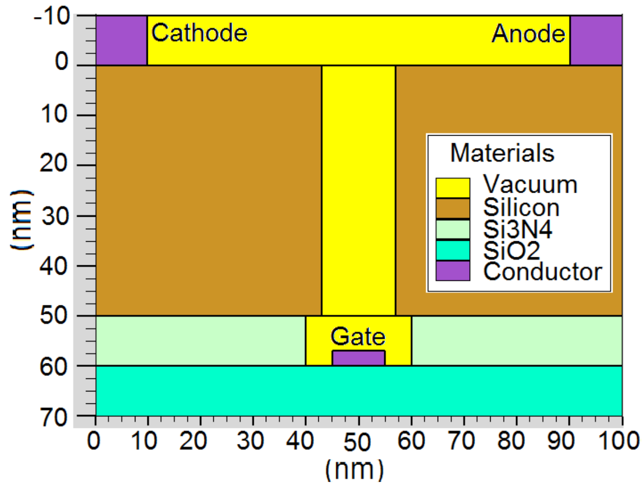

FIGURE 2. The NOI-triode-1 variant as input structure in Atlas.

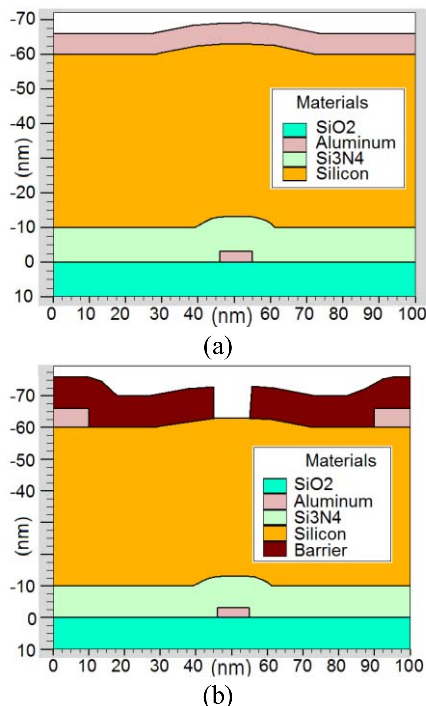

FIGURE 3. (a)-(b) Different simulation stages during the technological processing of the NOI-triode1 device.

10nm width. Three depositions follow over the entire structure: 10nm nitride, then 50nm Silicon, then 6nm Al, Fig. 3a. A 10nm mask for the anode/cathode electrodes configuration allows the lateral Al etching off. A barrier layer is deposited above. The mask for the vacuum cavity configuration is performed, Fig. 3b. Next step is the Silicon dry etching process, with over-etching under barrier and 85° angular etching, while the nitride acts as etch stop layer.

During the last step, Athena simulates the nitride etching under 75° angle and 5nm undercut, to create the beneath cavity. Now, the bottom oxide acts as etch stop layer.

The final structure looks like Fig. 2. Alternatively in Athena, the anode/cathode walls can be complete vertically created, if the coordinates of the removed Si are specified, Fig. 2.

C. FUNCTIONAL ESTIMATIONS

The electron emission from a semiconductor edge into vacuum was experimentally demonstrated by Srisonphan and collab. [5]. In NOI-triode, as in etched MOS capacitor [5], the charge neutrality is maintained by relatively remote charges of opposite polarity, induced across the insulator layer (thin oxide in MOS or vacuum cavity in NOI), so that a Columbic repulsion occurs among accumulated electrons in the Si-island edge. This repulsion is suspected to significantly foster the electrons emission from Si into vacuum, [5].

All vacuum devices with field emission, including vacuum transistors or NOI triodes are dominated by the FN (Fowler–Nordheim) conduction mechanism, [2]–[10]. Hence, in the present simulations, the Atlas models include FN tunneling, CVT Lombardi mobility model for non-planar devices, Shockley-Read-Hall recombination rate, Fermi carrier distributions, Band Gap Narrowing (BGN) in heavily doped cathode-anode regions and Selberherr's ionization model.

A maximum current density of 1.6×10^6 A/cm^2 is admitted for all NOI-triodes, to conventionally adopt a stop criterion for the anodic voltage increasing. This limit value is considered from power dissipation reasons, by comparison with other devices: MOSFETs with similar sizes has the maximum drain current of 100nA/nm or 100μA/μm [24], while special FETs support 850μA/μm, [25]. Consequently, in next simulations, the applied voltages are limited up, to command a maximum current of 800μA/μm that means a limit current density of 1.6×10^6 A/cm^2 considering $y_{Si} = z_{Si} = 50$nm for NOI-triode1 and $y_{Si} = z_{Si} = 12$nm for NOI-triode2.

D. OUTPUT CHARACTERISTICS

For the output characteristics analysis, I_A-V_A, the anode voltage is varied from 0V to 35V, while the gate voltage takes different values: $V_G = -20$V; -15V; -7V; 0V; $+7$V. Figure 5 comparatively presents the simulated I_A-V_A curves of the NOI-triode1, besides to some experimental picked points from literature of some vacuum devices, [2], [6], [8], [9]. Because the anodic currents are dominated by the Fowler-Nordheim component, as in any vacuum triodes [2], [3], [5], [9], the exponential dependence, I_A-V_A, is fulfilled in Fig. 4, too.

The characteristics reveal a drive current $I_{A\text{-}ON}$ for $V_A \geq V_{A\text{-}ON}$ voltage, accordingly to the *anode turn-on voltage* of any vacuum device [2], admitting the convention:

$$V_{A-ON} = V_A|_{I_A-ON=1\%\cdot I_{A,max}}. \quad (1)$$

For the NOI-triode1 from Fig. 4, the extracted pairs ($I_{A\text{-}ON}$, $V_{A\text{-}ON}$) are: (0.6μA, 20V) at $V_G = +7$V; (0.9μA, 17V) at $V_G = 0$V; (1.4μA, 14V) at $V_G = -7$V; (1.8μA, 11V) at $V_G = -15$V; (2.1μA, 6V) at $V_G = -20$V. The fabricated

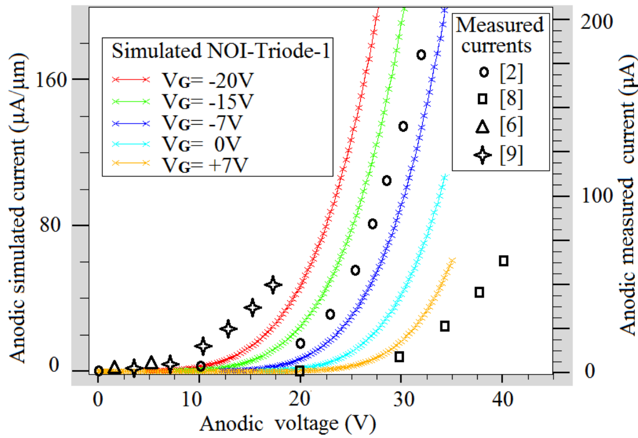

FIGURE 4. **The output characteristics, I_A-V_A of the NOI-triode1 in comparison with some experimental picked point from vacuum devices.**

vacuum devices present similar I_A-V_A experimental shapes, with $V_{A\text{-}ON}$ chronologically decreasing, but losing also in the $I_{A\text{-}ON}$ value. The experimental pairs ($I_{A\text{-}ON}$, $V_{A\text{-}ON}$) are: (200µA, 20V) for triodes with larger gaps [2], [8], (0.4µA, 5V) for a vacuum nanotransistor with 10nm gap [9], up to (0.03µA, 0.5V) for vacuum transistor with cylindrical gate [6].

In Atlas, the simulated anodic currents are expressed in Amperes on a default depth of 1µm. Admitting a depth of the Si-island of 50nm, the anodic current is 160µA/1µm or 8µA for z_{Si} = 50nm. These values are reached both for the NOI-triode1 at $V_G = -20V \ldots -7V$ and vacuum nanotransistor, [9]. A further observation concerns the gate bias. Simulations reveal that positive gate voltages produce lower currents, Fig. 4. So, in next paragraph, only negative gate voltages are applied.

E. TRANSFER CHARACTERISTICS

The I_A-V_G analysis starts from the strong and weak tunneling regimes that are encountered in NOI-transistors, too [14]. In this scope, the anode voltage is kept by turn to +0.7V, 1V or 2V, to allow a weak Fowler-Nordheim tunneling; for a strong tunneling, the anode voltage is maintained to 15V or 30V, while the gate voltage is ramped from 0V to −25V, taking care to avoid current densities over 1.6×10^6 A/cm^2 or 800µA/µm. The range is in agreement with the measured range of the current density in the ON-state, $J = 1 \times 10^5$ A/cm^2 of the vacuum MOS field-effect transistor with ITO intermediate gate, [5]. The transfer characteristics, I_D-V_G, are presented at logarithmic scale, besides to the gate currents, Fig. 5.

As in the NOI-transistor case, the strong tunneling regime ensures highest currents up to 600µA/µm in maximum bias conditions, offering a maximum transconductance of 2µS and low enough gate currents with $I_A/I_G = 10^3$ at V_A = 30V.

An ON-OFF states transition becomes visible only in weak tunneling regime, when $V_A < 3V$. For $V_A = 2V$ the transfer characteristics present: $I_{OFF} = 10^{-17}$A/µm, $I_{ON} = 1.8 \times 10^{-7}$A/µm, while the gate current is extremely low, $I_A/I_G = 10^{10}$ at $V_A = 2V$.

The parameters of the NOI-triode device must be similarly defined to those of the solid-state transistors, in order to compare their performances. In any vacuum triodes, the I_A-V_G characteristics reveal a drive current over a *gate turn-on voltage* $V_{G\text{-}ON}$ [3], [9], equivalent to a general threshold voltage. Let be the convention:

$$V_{G-ON} = V_T = V_G|_{I_A=1\%\cdot I_{A,max}}. \quad (2)$$

The *sub-threshold swing* (SS) is computed in sub-threshold conditions, after its traditional definition:

$$SS = \frac{\Delta V_G}{\Delta(\lg I_A)}[mV/Decade]\Big|_{|V_G|<|V_T|}. \quad (3)$$

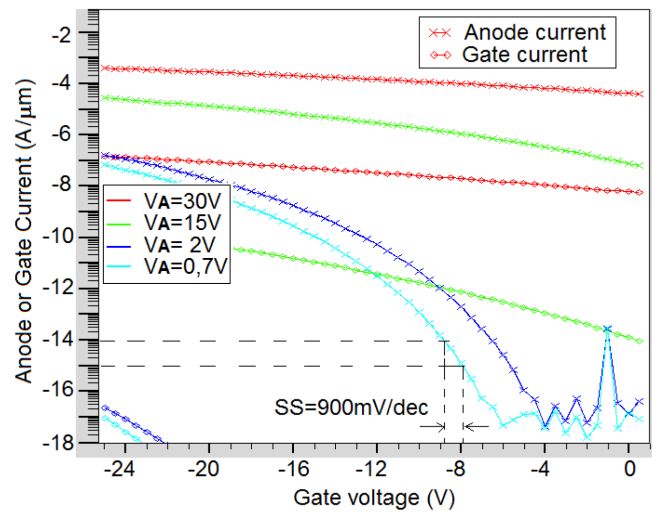

FIGURE 5. **A family of the I_G, I_A-V_G simulated curves of the NOI-triode1.**

Unfortunately, this NOI-triode1 variant with higher sizes than the studied NOI-transistors [14], [17], offers inferior swing. An optimum SS is extracted at V_A = 0.7V as 900mV/dec, Fig. 5. The next target is to find other arrangement of the electrodes and vacuum gap, so that the SS parameter decreases under 200mV/dec. A first optimization direction is to decrease the gap length x_C from 14nm (Fig. 6a) to 8nm or to 4nm (Fig. 6c).

Another algorithm is to keep x_C = 14nm, but to approach the gate metal, increasing its thickness from 3nm (Fig. 6a) to 11nm (Fig. 6b). Combining both strategies, the gate metal thickness is increased to 9nm and the gap length is decreased to 4nm, (Fig. 6d). Details of the NOI-triode1 variants, beneath the vacuum cavity, for each strategy, are presented in Fig. 6.

Figure 7 comparatively presents the I_A, I_G-V_G curves simulated for each variant of NOI-triode1 from Fig. 6(a)-(d). The gate current is monitored, because a closer gate position to the anode/cathode regions can trigger a higher leakage.

A successful solution is to place the gate in the way of the anodic flow, as is suggested in Fig. 1. So, a thicker gate

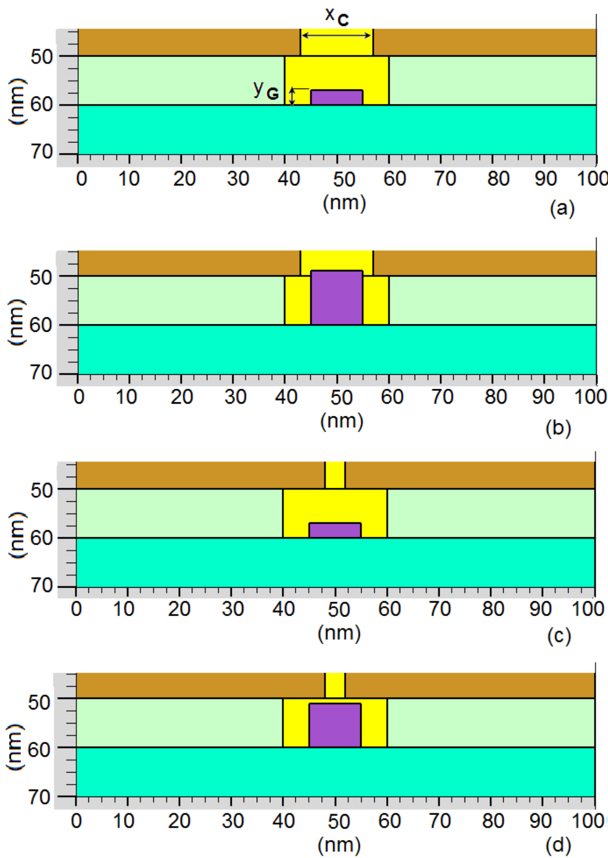

FIGURE 6. Details of the gate position in respect to the anode-cathode corners.

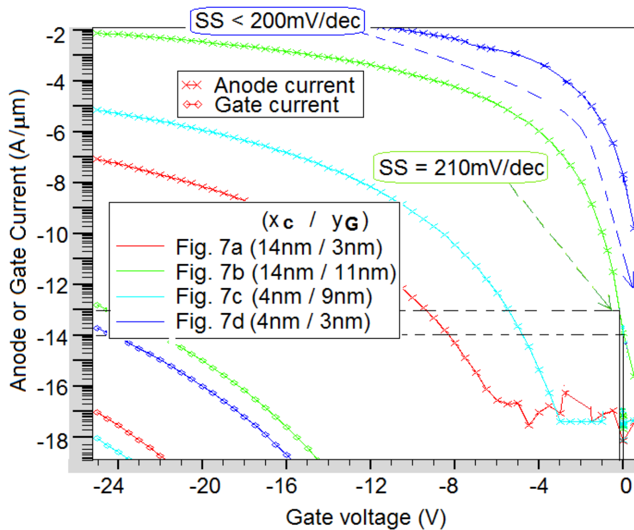

FIGURE 7. The I_A-V_G comparisons at V_A = 2V, showing the SS decreasing from Fig. 6(a, c) to Fig. 6 (b) and Fig. 6 (d).

electrode up to $y_G = 11$nm (Fig. 6b), offer attractive parameters: SS = 210mV/dec, $I_A/I_G = 10^{10}$ and $V_T = -3$V. The NOI-triode1 variant from Fig. 6d that benefits from thicker gate electrode and lower gap, offers the best parameters: SS = 195mV/dec, $V_T = -1$V, keeping $I_A/I_G = 10^{11}$ ratio still affordable.

III. THE NOI-TRIODE-2

A. THE DEVICE EFFICIENCY AND COMPARISONS WITH LITERATURE

The NOI-triode2 sizes are inspired by the previous conclusions and are connected to the prior NOI devices, accepting $x_C = 3$nm for nano-cavity and $x_G = 1$nm for the gate metal, $y_{Si} = 10$nm, $x_{Si} = 12$nm and $z_{Si} = 12$nm for the Si-islands, in agreement with the NOI demands, [13], [17]. The other construction parameters are conserved from the NOI-triode1 variant: oxide thickness, film doping, fixed interface charge, ohmic contacts, Tamm states, beside to the Atlas models.

This NOI-triode2 structure is presented in Fig. 8.

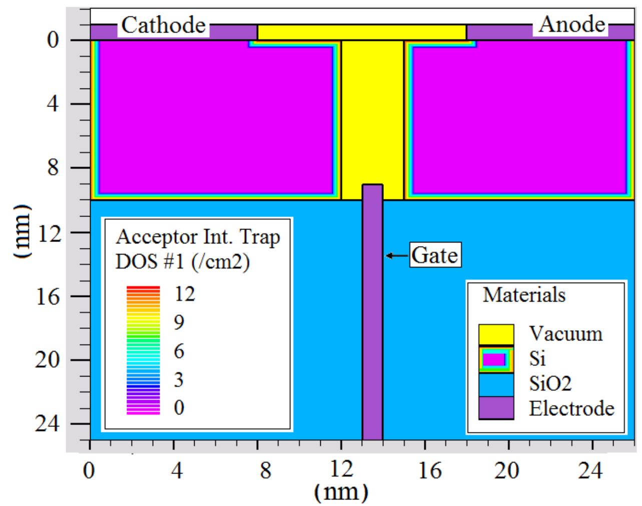

FIGURE 8. Simulated NOI-triode2 structure with DOS traps density in Si-islands.

Figure 9 comparatively presents the simulated transfer characteristics of the NOI-triode2 and NOI-transistor, besides to experimental picked points from [5], [6], [9]. In order to have the intensity of the gate stimulus on the Ox axis, for so many devices, some of them negative biased and others positive biased, the gate voltage is represented in modulus in figure 10. For the NOI-triode2 device, figure 10 firstly shows that the NOI-triode2 offers better parameters than the NOI-transistor: $SS_{NOI\text{-}triode2} = 90$mV/dec $<$ $SS_{NOI\text{-}transistor} = 650$mV/dec [14], improved I_{ON} current - $I_{ON\text{-}NOI\text{-}triode2} = 10^{-4}$A $>$ $I_{ON\text{-}NOI\text{-}transistor} = 10^{-5}$A and comparable I_{OFF} current, in agreement with prior results [11]–[12]. The main disadvantage of the NOI-triode2 device is its higher gate current, with $I_A/I_G = 20$ at $|V_{G,max}| = 10$V and $I_A/I_G = 1000$ at $V_G \approx 0$V. Working at lower voltages, (e.g., $|V_{G,max}| = 8$V), the ratio I_A/I_G is improved to 250. The comparisons of performances among the experimental vacuum devices, simulated NOI-transistor and NOI-triode2 from Fig. 9, prove.

- strong points for the NOI-triode2 devices are: (1) best SS parameter among all devices, reaching 90mV/dec; (2) best I_{ON}/I_{OFF} ratio with highest I_{ON} and lowest I_{OFF} values, working in weak tunneling regime, at low $V_A = 0.6V$; (3) taking into account the power limitation, the NOI-triode2 configuration efficiently work at low gate voltage, $|V_G| < 1.5V$, offering a strong drive current of $1 \ldots 100\mu A/\mu m$.
- strong points of the experimental vacuum transistors: (1) lowest threshold voltage, reaching $V_T \cong 0.5V$ [5]; (2) excellent $I_A/I_G = 10^6$, only for the insulated gate configuration [9]; (3) lowest gate currents [6], [9].

However, the field-effect transistor with MOS capacitor and ITO intermediate gate metal [5] benefits on sensitive current acted by extremely low gate voltages up to 2V, but suffers from a huge $I_G/I_A = 10^{-1}$ ratio, Fig. 10 and [5] and offers extremely poor drive current around 80nA, [5].

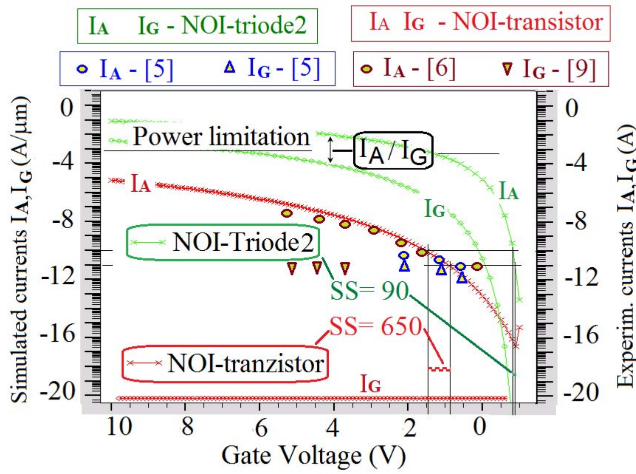

FIGURE 9. Comparative curves I_A-V_G and I_G-V_G at $V_A = 0.6V$ for the NOI-transistor with SS = 650mV/dec and NOI-triode2 with SS = 90mV/dec; experimental picked points are measured at $V_A = 1V$ for [5], [6].

The simulated NOI-Triode2 transfer characteristics I_A-V_G, for different anode voltages indicate a SS improving, if the anode voltage is decreased, so that the minimum SS = 85mV/dec is accomplished at $V_A = 0.4V$. This behavior is in agreement to the entire theory of weak tunneling regime presented for the NOI-transistor, [18], and completely justifies the relationship of the NOI-triode with the NOI devices.

B. TECHNOLOGICAL SOLUTIONS, PLANAR TECHNOLOGY

A technological solution to fabricate the NOI-triode2 structure is to rotate the NOI-triode2 structure by 90°. In this way, the lateral width problem is converted into thickness problem, being more convenient for the nowadays technologies.

So, in this section, a planar technology is proposed to achieve the 1nm gate thickness, inside the vacuum cavity of 5nm thickness. The successive technological steps are simulated by Athena from Silvaco.

The start wafer is a SOI wafer with 20nm Si-film on 20nm buried oxide. Over the Si-film surface follows the subsequent depositions: 2nm SiO2; next 1nm Al deposition; next 2nm SiO2 deposition; next 20nm Si-film growing.

The subsequent etching processes are distinctly applied to different materials: top-Si-film is left etched from x = 30nm, Fig. 10a; the upper oxide is left etched underneath Si; then Al-gate is left etched underneath Si, achieving an intermediate structure, Fig. 10a. The second oxide layer is left etched at the same coordinate as the upper oxide. This is possible in Athena, specifying the removal coordinates. By a selective mask, the anode and cathode Al-contacts can be deposited. Optionally, a thermal oxidation can laterally convert a half part of the top Si-film toward the right, to accomplish a lateral isolation of the anodic island, Fig. 10b.

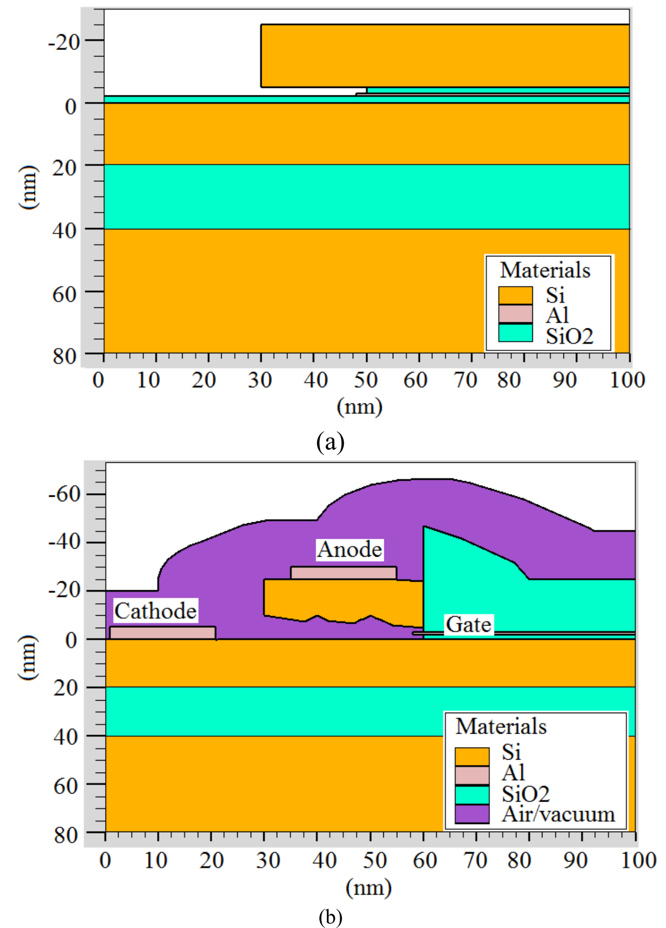

FIGURE 10. (a) An intermediate result of a planar variant of the NOI-triode2 device, after the Athena simulations; (b) the final structure.

IV. DYNAMIC CONSIDERATIONS

The dynamic analysis starts from the estimated transconductances: 2μA/V for the NOI-triode1, Fig. 5 and 20μA/V for the NOI-triode2, selecting $V_G = 2V$, Fig. 9. The frequency performance of a vacuum triode can be characterized by the cutoff frequency, f_T. A model of this frequency depends

on the gate-cathode, gate-anode capacitances, C_{GC}, C_{GA}, of a field emission triode, [26], or only to C_{GC} for a vacuum field effect transistor [9]:

$$f_T = \frac{g_m}{2\pi C_{GC}} \tag{4}$$

Figure 11 presents capacitances C_{GC}, C_{GA}, for both structures NOI-triode1 and NOI-triode2, biased in weak tunneling to $V_C = 0V$, $V_A = 2V$ and $V_G = -8V$, during the frequency rising. The simulations show $C_{GC} = C_{GA} = 18 \times 10^{-18}$ F/µm or 0.9aF for $z_{Si} = 50$nm in the NOI-triode1 case and $C_{GC} = 82 \times 10^{-18}$ F/µm or 0.8aF and $C_{GA} = 87 \times 10^{-18}$ F/µm or 0.84aF for $z_{Si} = 12$nm in the NOI-triode2 case. Accordingly to eq. (4), the cutoff frequency is 0.35THz for NOI-triode1 and 4THz for NOI-triode2.

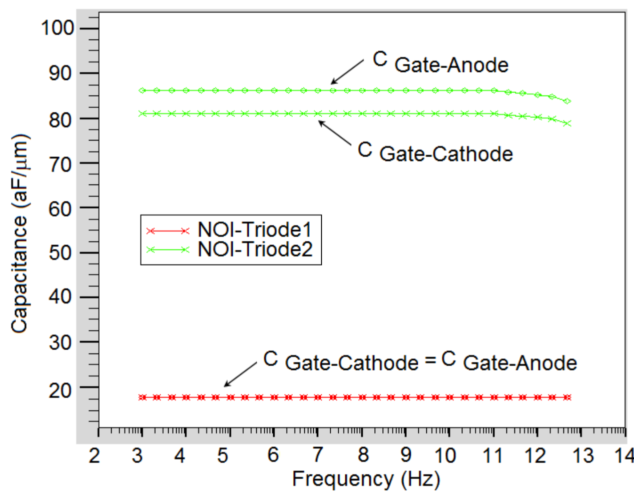

FIGURE 11. The variation with frequency of the capacitances - C_{GC}, C_{GA}, for the NOI-triode1 and NOI-triode2.

V. DISCUSSIONS

Table 1 comparatively summarizes the performances of the NOI-triode1 or NOI-triode2, NOI-transistor [27] and few related devices, including extremely low SS tunnel-FETs, [28].

The NOI-triode1 or NOI-triode2 devices excel by (see Table 1): (i) the anode/gate turn-on voltages are low enough among the vacuum devices, going to the MOSFET or Tunnel-FET [29] threshold voltages, especially for the NOI-triode2 case; (ii) maximum I_{ON}/I_{OFF} ratio among all devices; (iii) extremely low OFF current for NOI-triode1 or 2 at low V_A; (iv) a swing between 90 to 210mV/dec for the NOI-triodes, more compatible with MOSFETs than NOI-transistor or vacuum triodes [2]–[9], [11], [12]; (v) a high I_A/I_G ratio is ensured by a weak tunneling work regime at V_A sub-2V, [14]; (vi) the *command voltages* are in agreement with the *reduced sizes* of the proposed NOI-triodes2 and are lower compared to a NOI-transistor of similar sizes or vacuum transistors [9].

Conventionally adopting a maximum simulated current of 800µA/µm, a maximum applied voltage for the NOI-triode goes up to 30V. However, not these limits up voltages are the drive voltages that can go down up to 1...3V. For instance, for NOI1-triode, Fig. 4 shows $I_A = 100$µA/µm that means 5µA for $z_{Si} = 50$nm, at the same voltage $V_A = 30$V, as experimental older literature [8]. From the I_A-V_G point of view (see Fig. 5), the anodic voltage must be under 3V to allow an ON/OFF transition, suitable for a field transistor effect. For NOI1-triode, Fig. 5 shows a current $I_A = 1$pA/µm that means 0.05pA, much lower than recent literature results: 10pA [5], 100pA [6], for the same applied voltage around 2V. The presented NOI1-triode has a larger gap of 14nm than the transistor from [6] and a device peculiarity that still persists to the NOI2 -triode: flat walls and two corners of 90° for the electron emission. The anode /cathode narrowing that improves the Fowler Nordheim emission was presented elsewhere [17] and it is not the aim of this paper. Obviously, the experimental vacuum transistors with sub-10^0 tips posses optimized shape factor that allows emission currents of 10µA at 10V [9], or even less, 100pA at 2V [6]. Fortunately, the NOI2-triode simulations show much less drive voltage: $V_A = 0.6$V and $V_G = 2$V that ensure $I_A = 800$µA/µm (Fig. 9) that means 10µA drive current, superior to the newest experimental vacuum device [6], which provides 0.1nA at the same $V_G = 2$V. This allows a drive voltage sub-1V to command 10nA in the NOI2-triode, better than in the vacuum transistor from [6].

TABLE 1. Different Performances for Different Devices.

Devices → Parameter ↓	NOI-triode 1 / 2 14nm /3nm gap	NOI-Transistor 2nm gap	Vacuum, MOS, related devices
$V_{G\text{-}ON}$ or V_T [V]	-16 / -1	-10 [12] -2 [17] +10 [17]	8.8 [9] 0.4 [29] 0.5 [5]
$V_{A\text{-}ON}$ [V]	20...6/ 1	2.3 [12] 2.4 [13] 3 [11]	14 [2] 2 [6] 1 [5]
$I_{ON,\,max}$ [µA]	40 / 10	0.012 [11] 8 [17]	0.080 [5] 3 [6]
I_A / I_G	10^{10} / 10 ... 250	$>10^3$ [12] 10^{30} [17]	10 [5] $>10^3$ [6, 9]
I_{ON} / I_{OFF}	10^4 / 10^{14}	10 [11] 10^8 [14]	10^5 [9] 500 [5] 10^4 [6]
SS [mV/dec]	900 / 85	650 [14] 210 [17]	4400 [6, 9] 55 [29]
g_m [µS]	2 / 20	0.025 [12]	57 [2] 0.02...2 [5]
f_T [THz]	0.35 / 4	0.1...1[13]	0.1....10 [9, 15]

A cutoff frequency of 0.35THz for NOI1 is a relative poor value, but it is in a complete agreement to the experimental value of 0.4THz [9], of a similar fabricated vacuum nano-device of 10...14nm gap, based on the same model (4).

A better cutoff frequency of 4THz is estimated for the NOI2-triode, which is closer to the capability of the experimental newer device from 2017, [6]. All values are placed in the predicted interval of the frequencies served by the transistors made from "Nothing" [15]: 0.1...10THz.

VI. CONCLUSION

This paper proposed a triode configuration for a NOI device. Some poor parameters of the previous NOI-transistors were improved by this triode configuration: SS decreased from 650mV/dec to 85mV/dec comparable to a MOSFET swing, g_m increased from 25nS to an average value of 2μS, offering a tera-hertz cutoff frequency around 0.35THz.

For the NOI-triode1 variant with 14nm gap, the performances were obviously inferior to a NOI-triode2 variant with 3nm gap or NOI-transistor with 2nm gap, but further improvements concerning the gate metal position, were discussed. The Athena simulation tool from Silvaco provided a fluent technological plan for the NOI-triode1 variant, anchored as much as possible in the nowadays processes. For NOI-triode2 variant, a technology was only drafted, based on a planar solution.

The simulated features of the NOI-triode 1 and 2 structures were permanently compared to the others vacuum devices. The turn-on anodic voltage was reduced from 20V to 2...6V. To ensure minimum I_G/I_A ratio, maximum I_{ON}/I_{OFF} ratio and minimum SS swing, the NOI-triode must be operated in the weak tunneling regime, at low operation voltages, like $V_C = 0V$, $V_A < 1.2V$ and $V_G = -3V$. The dynamic analysis also recommends the NOI-triode for the high-frequency operation up to 4THz.

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