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Simulation Study of a Super-Junction Deep-Trench LDMOS With a Trapezoidal Trench

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ABSTRACT A super-junction (SJ) deep-trench (DT) lateral double-diffused metal-oxide-semiconductor transistor improved by tilting the DT sidewalls is proposed. The incline of sidewalls introduces some vertically varying charges into the SJ drift regions on both sides of the DT. Therefore, the adverse effect of the DT on the surface electric field distribution is withstood, and the device can approach an ideal state of charge-balance. Simulation results show compared with a conventional device, which has the same drift region concentration and the same size but the perpendicular sidewalls, the proposed device presents a better figure of merit over 2.5 times higher. Besides, a feasible fabrication process for the proposal is presented and discussed.

INDEX TERMS Deep-trench, LDMOS, super-junction, power MOSFET, power semiconductor devices.

I. INTRODUCTION

It is well-known that the Super-Junction (SJ) technique can improve the electric properties of Lateral Double-diffused MOS (LDMOS) [1], [2]. However, since the traditional LDMOS in a lateral form relies on a large cell pitch to sustain surface voltage, the benefit brought by SJ is limited. This has been addressed by the Deep-Trench (DT) technique, in which a DT filled with dielectric is utilized to sustain most of the surface voltage [3]–[7]. Because the critical electric field of dielectric is much higher than that of silicon, the cell pitch is greatly curtailed. To further optimize the DT-LDMOS by SJ, a design concept of variation-vertical-doping (VVD) is proposed [8]. It aims to overcome the adverse impacts of the capacitive DT, and promotes the device into an ideal state of charge-balance. However, the process to realize the VVD is complex and costly.

In this paper, a design concept of tilting the DT sidewalls is proposed for the SJ-DT-LDMOS. The simulation results show that, by incline of sidewalls, the adverse effect of the DT is withstood, and the charge-balance is approached. Moreover, compared with the sophisticated process to realize the VVD, the process for the proposal can be practical.

II. STRUCTURE AND THEORY

Fig. 1(a) and (b) show the conventional and proposed devices, respectively. At the top of them, there are electrodes of Gate (G), Source (S), and Drain (D). Between S and D, a DT filled with dielectric curtails the cell pitch. Beside the DT, two SJ regions, which consist of two pairs of n^- and p^- pillars, act as the drift regions, and are connected by an n^- layer at the bottom of the DT. Below the n^- layer, a p-substrate is linked to S.

In Fig. 1(a), when the device is off, the electric flux emitted by the depleted n^- pillar is absorbed by the depleted p^- pillar. If we provisionally ignore the impact of the DT, when the doping concentrations of the two pillars are equal, the absorption of electric flux would be sufficient, even though all the pillars are heavily doped. In this case, the drift regions can act as intrinsic regions to sustain a breakdown voltage (BV) as high as possible and, meanwhile, present an on-resistance as low as possible. This is the well-known

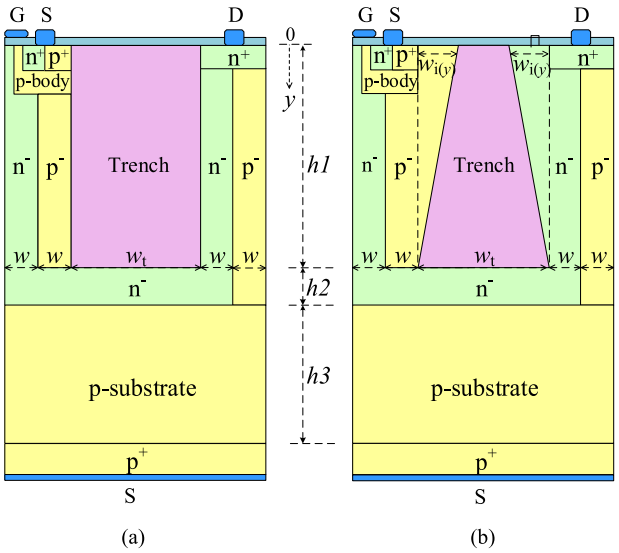

FIGURE 1. **(a) Conventional SJ-DT-LDMOS with perpendicular sidewalls. (b) Proposed SJ-DT-LDMOS with a trapezoidal trench.**

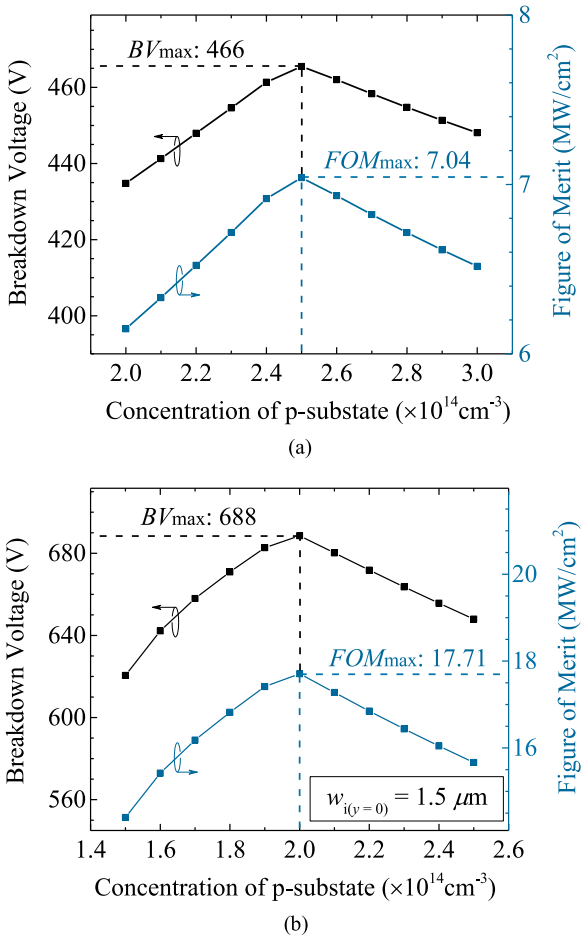

FIGURE 2. **Optimization for the (a) conventional and (b) proposed devices. The compared devices have the same drift region concentration of 8×10^{15} cm^{-3}, and the same sizes of $w = h_2 = 1.5$ μm, $w_t = 7$ μm, $h_1 = 15.5$ μm, $h_3 = 43$ μm. By linearly tilting the DT with $w_{i(y=0)} = 1.5$ μm, the proposed device achieves a considerably improved breakdown voltage and *FOM*.**

state of charge-balance in the SJ devices. However, the DT is narrow, and would form a big capacitance with plates of the left p^- and the right n^- pillars. At the top of the DT, the voltage across the capacitance equals *BV*, and at the DT bottom, it is small (due to the n^- layer is not SJ but is doped as heavily as the n^- pillar). Hence, the capacitive DT inevitably induces plenty of charges with vertically varying distribution into the adjacent pillars, which break the charge-balance.

To address that, it is proposed to tilt the DT sidewalls, as shown in Fig. 1(b). The incline of sidewalls broadens the adjacent pillars and accordingly introduces some vertically varying charges beside the DT. If these charges meet the requirement of the DT capacitance, they can protect the SJ drift regions, and make them approach the charge-balance.

III. OPTIMIZATION AND COMPARISON

The devices are optimized and compared by simulation with a tool of MEDICI. The models, which are commonly used in the simulation of power devices, include FLDMOB, CONMOB, SRFMOB2, CONSRH and IMPACT.I. The comprehensive utilization of these models has been proved to be valid to make the simulation results agree well with the experimental results [4], [9]–[11]. Besides, a widely used Figure of Merit (*FOM*), which equals the square of the breakdown voltage divided by the specific on-resistance ($R_{on,\,sp}$), is adopted to evaluate the device performance [5]. $R_{on,\,sp}$ is simulated when the gate voltage is 10 V and the on-state voltage drop between D and S is 0.5 V. For an impartial comparison, the devices are allocated the same size and the same drift region concentration.

First, the tilted width at the surface of the proposed device, as well as $w_{i(y=0)}$, is optimized based on a rough calculation. More specifically, if we ignore the small voltage across the bottom of the DT, when the device is charge-balanced, the integral concentration of the charges induced by the capacitive DT ($D_{1(y)}$) can be inferred by referring to [8]. The difference ($\Delta D_{(y)}$) between $D_{1(y)}$ and that introduced by the slope ($D_{2(y)}$) is:

$$\Delta D_{(y)} = D_{1(y)} - D_{2(y)} = \frac{\varepsilon_0\varepsilon_t(BV)\,(h_1 - y)}{q\left(w_t - 2w_{i(y)}\right)h_1} - N_0 w_{i(y)} \quad (1)$$

where ε_0 is the vacuum permittivity; ε_t is the relative dielectric permittivity; q is the electron charge; N_0 is the concentration of the drift region; w_t, $w_{i(y)}$, h_1 and y have been marked in Fig. 1(b).

According to (1), to reduce $\Delta D_{(y)}$ as far as possible, $w_{i(y)}$ should be non-linearly varied with y. But a non-linear sidewall is difficult to control in the Deep Reactive Ion Etching (DRIE) process, which is usually used for etching DT [12]. Therefore, the sidewalls are set to vary with y linearly, and the optimized value of $w_{i(y=0)}$ to get the minimum

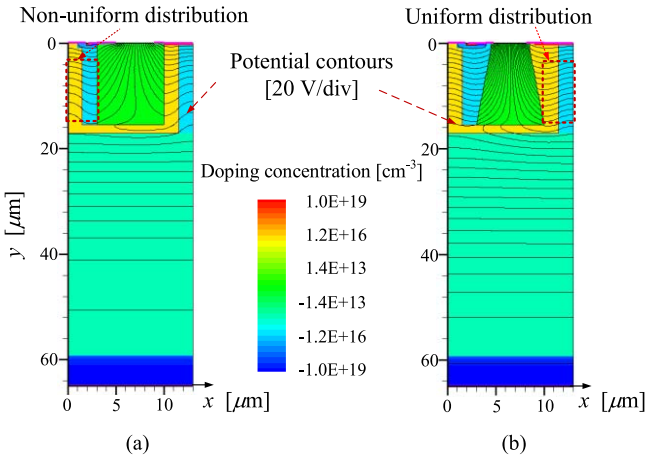

FIGURE 3. **Comparison of the potential distribution between the (a) conventional and (b) proposed devices, when they are both at the moment of critical breakdown. The potential contours (20 V/div) in the drift region are distributed more uniform in the proposed device than in the conventional one.**

$\Delta D_{(y=0)}$ is solved as:

$$\begin{cases} \text{if } w_t = \sqrt{8A}, \text{ when } w_{i(y=0)} = \frac{w_t - \sqrt{w_t^2 - 8A}}{4}, \Delta D_{(y=0)} = 0 \\ \text{if } w_t < \sqrt{8A}, \text{when } w_{i(y=0)} = \frac{w_t - \sqrt{2A}}{2}, \Delta D_{(y=0)} \text{ is minimum} \end{cases} \quad (2)$$

where $A = \varepsilon_0 \varepsilon_t (BV)/qN_0$.

The dielectric filled in the DT can be various materials [4], [8], [13]–[14]. In this paper, the PolyTetraFluoroEthylene (PTFE) with "$\varepsilon_t = 2$" is employed as an example. After putting the other specific values of "$\varepsilon_0 = 8.854 \times 10^{-12}$ F/m", "$w_t = 7$ μm", "$BV = 650$ V", "$N_0 = 8 \times 10^{15}$ cm^{-3}" and "$q = 1.602 \times 10^{-19}$ C" into (2), "$w_{i(y=0)} \approx 1.38$ μm" is calculated. Finally, through some fine-tuning in simulation, $w_{i(y=0)} = 1.5$ μm is selected.

Then, the p-substrate concentration (N_{p-sub}) is optimized for both of the devices. It is easy to understand that, to make the most of the bilateral drift regions, they had better sustain the approximate voltages when the device is in breakdown. During the turn-off, as soon as the n$^-$ layer is completely depleted, its potential will be clamped, and the voltage sustained by the left drift region will be roughly fixed. After that, further increased reverse voltage is mostly sustained by the right drift region. As N_{p-sub} greatly impacts the depletion of the n$^-$ layer, it should be optimized for better device performance. As indicated in Fig. 2, the conventional device, with an optimized N_{p-sub} of 2.5×10^{14} cm^{-3}, presents a maximum BV of 466 V and a maximum FOM of 7.04 MW/cm^2. The proposed one, with an optimized N_{p-sub} of 2.0×10^{14} cm^{-3}, presents a maximum BV of 688 V and a maximum FOM of 17.71 MW/cm^2. Namely, through the incline of the sidewalls, the FOM is improved over 2.5 times, and is higher than that of 11.4 MW/ cm^2 obtained by the previously published result [5].

Fig. 3 compares the potential distribution in the drift region when the devices are both facing breakdowns. The

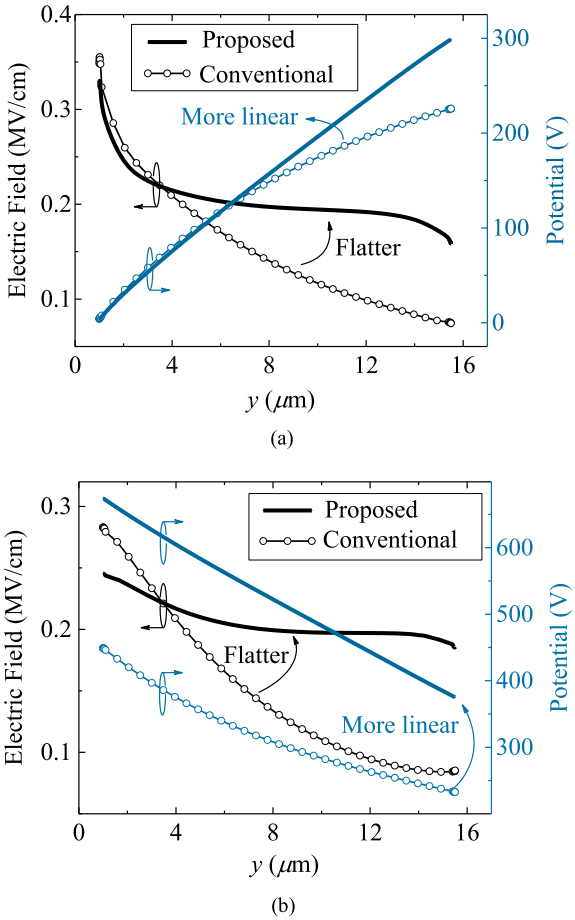

FIGURE 4. **Comparisons of the electric field and the potential distributed (a) at $x = 1.5$ μm as well as along the left drift region and (b) at $x = 11.5$ μm as well as along the right drift region. The proposed device presents flatter electric field distribution and more linear potential distribution than the conventional one.**

distribution in the proposed device is more uniform than that in the conventional one. To get a more evident view, the distributions of the electric field and the potential, along $x = 1.5$ μm and $x = 11.5$ μm, are shown in Fig. 4(a) and (b), respectively. Distinctly, the proposed device presents flatter electric field distribution, as well as more linear potential distribution, in both of the bilateral drift regions. These comparisons mean the proposed device is much more approaching to the charge-balanced state.

IV. PROCESS AND DISCUSSION

A process flow to fabricate the proposed device is showed in Fig. 5 (a) to (e). First, based on a wafer in (a), a round of epitaxy and ion-implantation is performed to form the n$^-$ layer, as shown in (b). Next, to get the SJ region, the multistep epitaxies and implantations are executed in (c). Then, a trapezoidal DT is etched and filled in (d). Finally, some processes compatible with the common CMOS technology are implemented to form the active region in (e). In the prior art of using VVD to gain the charge-balance, the step (d) should be replaced by (f) [8]. By using multistep

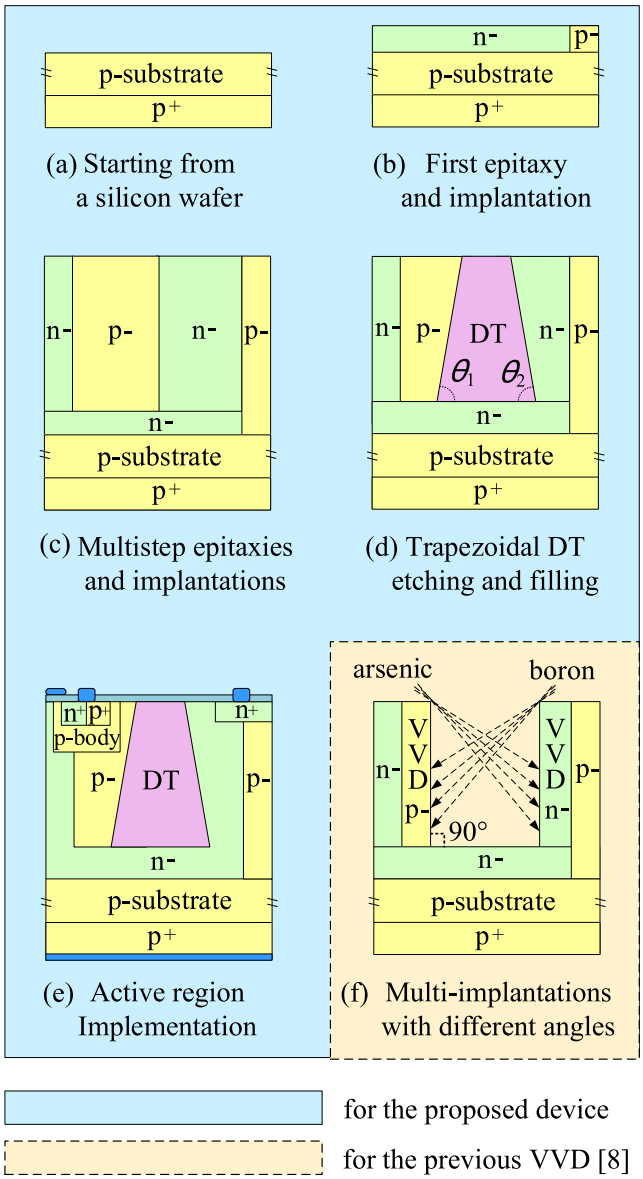

FIGURE 5. **(a) - (e) Key processes for the proposed device. In (d), the trapezoidal DT is etched and filled. Compared with the prior art of using VVD to gain the charge-balance, which relies on multistep implantations with different angles as shown in (f), the process for the proposal is more feasible.**

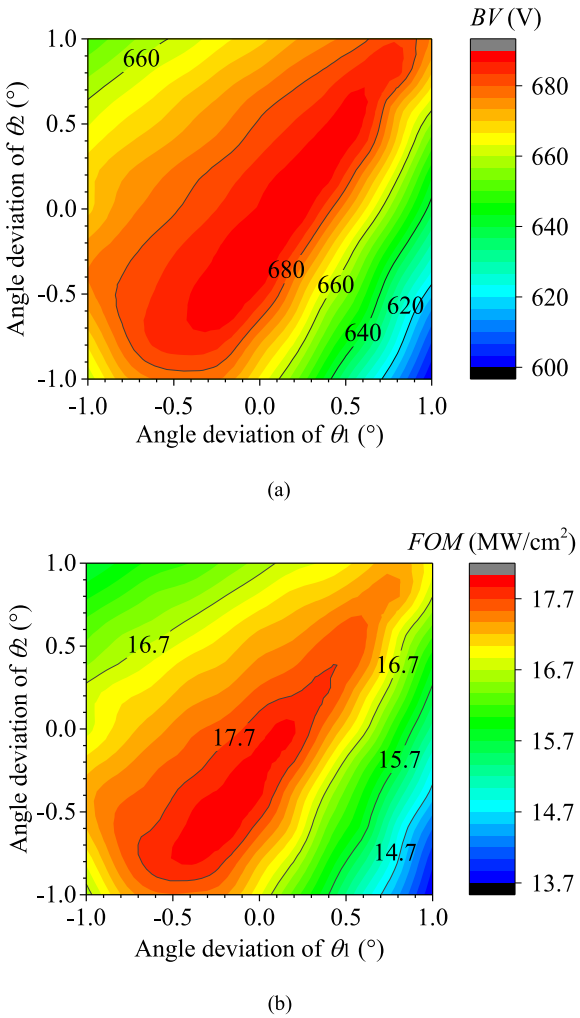

FIGURE 6. **Impact of the sidewall-angle deviation on the (a) *BV* and (b) *FOM*, where θ_1 and θ_2 are marked in Fig. 5(d). When the angles independently vary within (84° ± 1°), the device has the *BV* ≥ 600 V and *FOM* ≥ 13.7 MW/cm^2.**

angle-implantations, the charges with suitable distribution can also be introduced in both of the left p^- and right n^- pillars. But in (f), the sidewall is required to be perfectly vertical, which is demanding in practice. Moreover, to ensure both of the pillars get VVD likewise, the implantations had to be symmetrically repeated, which are complex and costly [15]. It should be noted that although the process for the proposal can be more practical, the process control to tilt the sidewall and to fill the DT in the step (d) is significant. Some discussions concerning these two issues are expounded.

For the DT etching, the process of DRIE is recommended, which has been also used in VVD [8]. DRIE is an extension of the well-known Reactive Ion Etching (RIE) technique. Its mechanism is using the repeated RIE and sidewall passivation to get a trench with high aspect ratio. Moreover, by tailoring the balance between deposition and erosion, the sidewall-angle can be tailored over a wide range, from positive to negative, meanwhile with high accuracy [16]. In 1998, RIE was already able to etch a trench with the aspect ratio of 30, while the sidewall-angle is varying within ±1° [17]. In 2010, DRIE improved the aspect ratio up to 50, with more uniform sidewall-angle (varying within ±0.3°) [16]. In the proposed device, the trench aspect ratio is less than 4, and the standard sidewall-angle is 84°. These parameters are able to be realized by the existing DRIE technique. Assuming the trench may be asymmetrically etched within a wide deviation range of 84±1°, as well as the left and right sidewall-angles (θ_1 and θ_2 marked in Fig. 5(d)) are different, the device still presents an acceptable performance in simulation, as shown in Fig. 6. Thus, DRIE is able to meet the requirement of trench etching for the proposal.

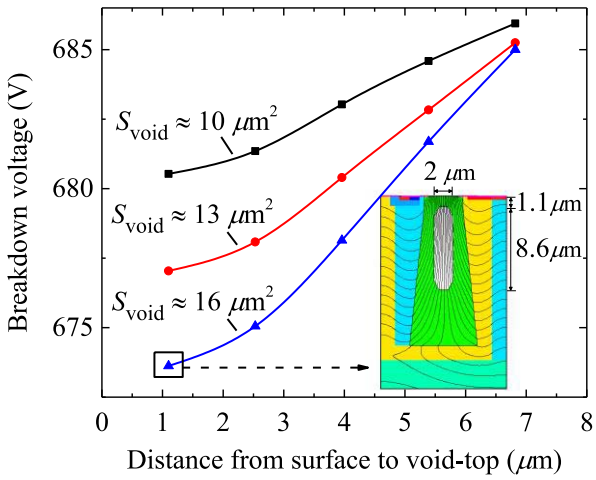

FIGURE 7. Impact of the void in the DT on the *BV*. In the simulation, the relative permittivity of the keyhole-shaped void is defined to be one. When the void approaches the surface more, or its area (S_{void}) is increased, the *BV* is decreased. But even when the distance between the void-top and the surface is only 1.1 μm, and the S_{void} reaches 16 μm^2, the *BV* is larger than 670 V. The attached picture displays the potential distribution at this situation (20V/div).

To fill the DT well, the High Density Plasma Chemical Vapor Deposition (HDP-CVD) is suggested. HDP-CVD has been extensively used to deposit dielectric since the 1990s [14]. It mainly relies on the mechanism of synchronized deposition and etching. Specifically, on one hand, the plasma directly contacts the wafer in low pressure to deposit dielectric into the trench. On the other hand, the deposited material around the trench entrance is uninterruptedly removed by argon bombardment to avoid voids. Hence, HDP-CVD has the ability to fill the trench with a complicated shape and high aspect ratio [18]. The speed ratio of deposition to etch ($r_{d:e}$) is important. If it is increased, the production output will be enhanced, but a void usually with a keyhole shape might be formed due to the blocked entrance. Although the simulation results showed in Fig. 7 illustrate the void has little impact on the *BV*, it is still a destabilizing factor for manufacturing. Therefore, the $r_{d:e}$ in the HDP-CVD is usually controlled to be less than 3:1 [19].

V. CONCLUSION

An improved SJ-DT LDMOS is proposed and studied in simulation. By tilting the DT, the device approaches the charge-balance, and gains a significantly improved relationship between the *BV* and $R_{on,sp}$. Moreover, compared with the prior art of VVD, the process for the proposal is preliminarily demonstrated to be more feasible. Therefore, the proposal is believed to be attractive to researchers in the related field.

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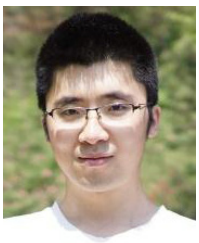

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