Received 1 June 2018; revised 20 July 2018; accepted 20 July 2018. Date of publication 16 August 2018; date of current version 31 August 2018.
The review of this paper was arranged by Editor L. Zhang.

Digital Object Identifier 10.1109/JEDS.2018.2862916

Modeling of Carrier Trapping and Its Impact on Switching Performance

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The content has been originally presented at EDTM'18 [20].

ABSTRACT Requirements for compact modeling to predict circuit power loss accurately are the focus of this investigation. Most important is the capturing of the differences between an ideal carrier reaction within the used devices and the reality during circuit operation. For this purpose the carrier trapping/detrapping, which occurs during circuit operation, has to be modeled accurately in addition to the conventional device characteristics. Carrier trapping events prevent device operation according to the ideal carrier dynamics and result in energy losses. It is verified that the influence of the carrier trapping, extracted by dc measurements, is not sufficient. Additionally, the dynamic switching performance must be precisely analyzed to extract the time constants involved in the carrier-trapping events. This is achieved by compact modeling based on solving the complete Poisson equation, which provides a simple and accurate modeling approach.

INDEX TERMS Carrier trapping, compact model, circuit simulation, power-loss prediction, carrier dynamics, Poisson equation.

I. INTRODUCTION

The carrier trapping phenomenon during device operation is becoming more serious due to the elevated requirements for high performance applications [1]. New substrate materials such as SiC and GaN are still suffering from a high crystal-defect density, which is an additional reason for the increasing importance of carrier trapping [2]–[4]. The device aging is a further non-negligible concern caused by the carrier trapping as well. Many investigations have been undertaken to characterize the crystal defects as well as the trapping events [5]–[11]. However, the difficulty is that characterization of the crystal defects is microscopically very complicated. Additionally, the measured microscopic features of the carrier trapping are not always applicable for real circuits due to the individually different operation conditions to which each device is subjected. It is known that the carriers require time to complete the trapping/detrapping events. This required time is called the trap time constant [12], [13]. It has been demonstrated that the power loss is dependent on this trap time constant, and that DC measurements alone cannot reproduce the power loss accurately [14], [15].

Mostly macroscopic characterizations have been performed to understand the trapping effect of real devices. To predict its influence on circuits, the trapping effect must be incorporated in circuit simulation. Historically, the device aging, which is a result of long-term carrier trapping, is modeled by a threshold voltage shift in combination with a mobility reduction [16]. However, there exists a gap between the microscopic features of carrier trapping and the macroscopic observations under real device application in circuits. Here, a compact model based on the device-internal potential distribution, obtained by solving the Poisson equation, is combined with the microscopic carrier-trapping properties [17]–[19]. The dynamically changing trap density is included in the Poisson equation, which realizes self-consistent inclusion of the dynamic trapping effects during device operation in circuits. It has been demonstrated that the trap density of states and the corresponding trap-time constant, which can be extracted from simple *I-V* and

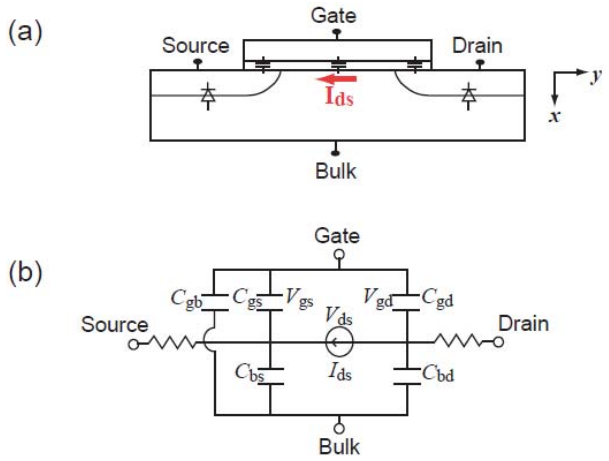

FIGURE 1. **(a) Schematic of a MOSFET, and (b) its equivalent circuit developed by Meyer [20].**

switching-characteristics measurements, provide sufficient information for compact modeling, so that circuit-design reliability can be secured [20]. In this article the carrier trapping feature is precisely investigated, and its applied voltage dependence is discussed.

II. SWITCHING CHARACTERISTICS OF MOSFETS

Active devices in circuits utilize their switching function. Fast switching is the target of any device development. As schematically shown in Fig. 1, MOSFETs consist of several capacitances and show corresponding current flows [21]. When a current flows, charges must be stored on these capacitances up to a certain amount, which is determined by the applied bias conditions. During device switching the total charge in the semiconductor substrate is varied according to the bias changes. The charge flow for storing the required amount of the charges is called the displacement current and is observed during the switching time

$$I(t) = I\left(V(t)\right) + \frac{\mathrm{d}Q}{\mathrm{d}t} \tag{1}$$

These charge/discharge events require time for their completion. The required time is usually called response delay and depends strongly on the fields applied within the device. The involved dynamic carrier reaction is the target, which has to be accurately considered to realize accurate prediction of the power loss in circuits. The observed transient device characteristics is exactly the result of the carrier dynamics happening within the device. The power loss is the required integrated energy [22]

$$Power = \int I(t) \cdot V(t)\mathrm{d}t. \tag{2}$$

III. ORIGINS OF ALL OBSERVED DEVICE FEATURES

There usually exist many inherent crystal defects either at the insulator/substrate interface or even in the substrate [23]. The influence of the defects at or near the interface dominates in the MOSFET characteristics. Fig. 2 shows measured

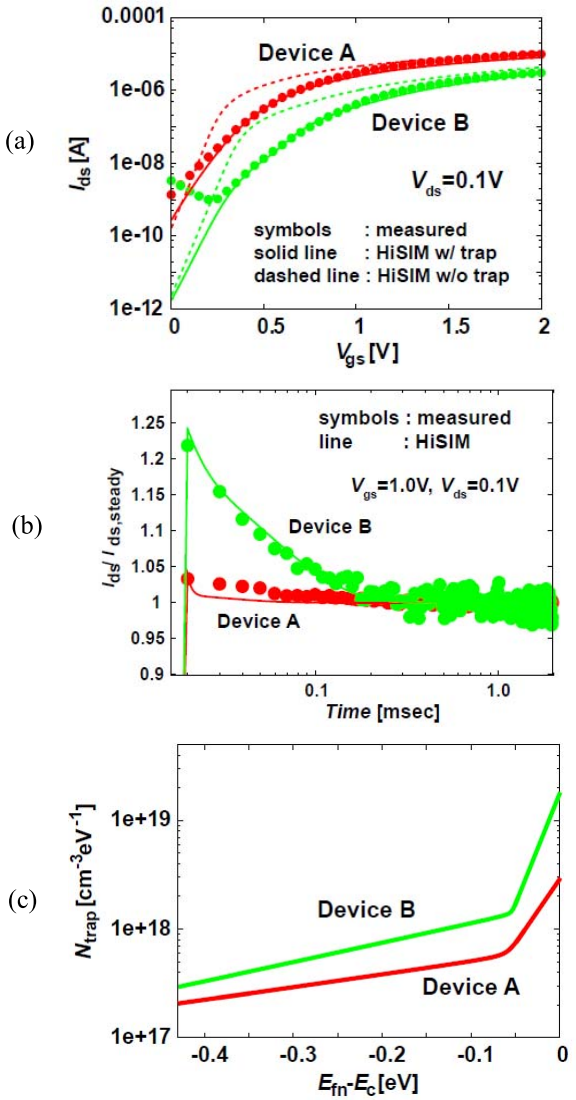

FIGURE 2. **(a) I_{ds}-V_{gs} comparison of HiSIM calculation results (lines) with measurements (symbols) for two different MOSFETs, (b) transient characteristics, (c) extracted density of states (DOS) [17].**

I-V characteristics of poly-Si MOSFETs, which suffer from Si grains induced below the gate during the crystallization process [24], [25]. Due to non-homogeneously distributed remaining grain boundaries, the *I-V* characteristics show large variations as can be seen in Fig. 2a. The switching performance of the depicted two identically-designed devices are quite different as can be seen in Fig. 2b [17]. The crystal defects at the grain boundaries cause carrier trapping during device operation, which results in the current degradation effect. In particular, the device B in Fig. 2a shows an enhanced carrier trapping effect. This trapping effect can be modeled by considering the trap density explicitly in the Poisson equation

$$\nabla^2\phi = -\frac{q}{\varepsilon_s}\left(p - n + N_D - N_A - N_{trap}\right) \tag{3}$$

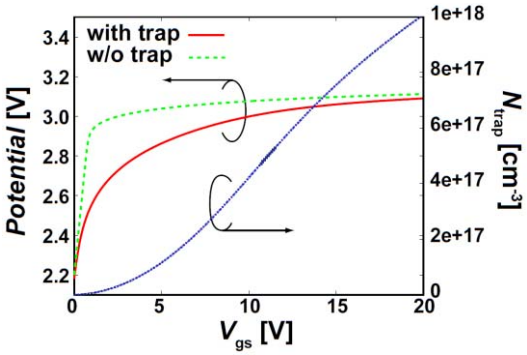

FIGURE 3. Potential modification as a function of V_{gs} due to increased trap density N_{trap} as extracted from the SiC-MOSFET measurements.

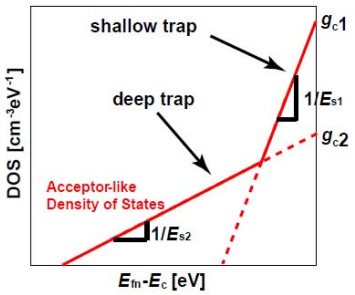

FIGURE 4. Schematic of density of states (DOS) on logarithmic scale as a function of the quasi-Fermi energy E_{fn} measured from the conduction band edge E_c.

where N_{trap} refers to the trap density, which is mostly trapped at the gate-insulator/substrate interface. By considering N_{trap} explicitly, the calculated potential values are modified, which is shown in Fig. 3 as a function of the gate voltage V_{gs}. This potential change leads to a degradation of the device characteristics such as the mobility or the threshold voltage. Capacitances are determined by charges induced by the potential-distribution change. Therefore the *C-V* characteristics are automatically changed according to the trap-density change.

IV. COMPACT MODELING OF CARRIER TRAPPING

The trap density of state is simplified by an exponential function as schematically shown in Fig. 4 [26]–[28]

$$N_{trap} = N_0 \exp\left(\frac{E_f - E_c}{E_s}\right)$$
$$N_0 = g_c E_s \frac{\frac{kT}{E_s}}{\sin\left(\frac{kT}{E_s}\right)} \tag{4}$$

where the conduction band edge and the Fermi level are denoted by E_c and E_f, respectively, while E_s and g_c are model parameters describing the trap-state density. Since E_f is a function of V_{gs}, the trap-state density detected by the given V_{gs} is changed as depicted schematically in Fig. 5. This property is exploited to extract the trap density of states from either measured *I-V* or 1/*f*-noise characteristics [18].

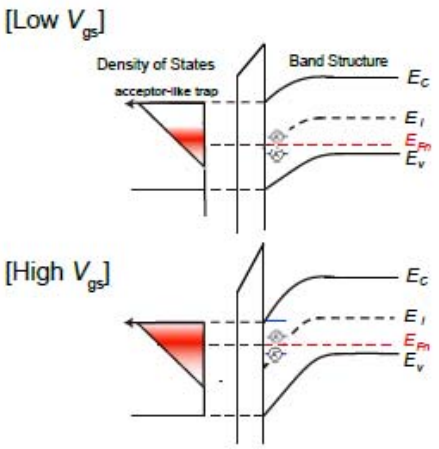

FIGURE 5. Schematic relationship between the trap-density distribution and the energy bending in the bulk, as induced by V_{gs}.

The correct capturing of the V_{gs}-dependent N_{trap} is important to reproduce measured *I-V* aging characteristics, as shown in Fig. 6. Fig. 6a verifies that the aging is not reduced to a simple parallel shift of the *I-V* characteristics. Fig. 6b shows the extracted density of states at different energy levels under different stress conditions and durations, as a function of the accumulated I_{sub} that is induced by the stress conditions times their durations [18], [19]. The origin for the carrier trapping is the carrier energy obtained from the induced fields due to the applied V_{ds} and V_{gs}. The V_{ds} fields result in so-called hot carrier (HC) trapping and the V_{gs} fields are the origin for the bias-temperature instability (BTI) effect [29]–[31]. The HC trapping is written as a function of the substrate current, which is a measure of the hot-electron amount. The BTI effect is written as a function of E_{ox}. The V_{gs}-dependence of E_f leads to a V_{gs} dependence of the aging as seen in Fig. 6a. The temperature dependence of N_{trap} is also described as shown in Fig. 7.

Two switching characteristics due to different capture cross-section values are obtained by 2D-device numerical simulation and are compared in Fig. 8 [32]. These results reveal that not only the trap density but also the capture cross-section is an important physical quantity to characterize the switching performance, as can be clearly seen in Fig. 8c. For the compact modeling purposes, we introduced the trap time constant τ_d [17]

$$\tau_d = \frac{A}{n \cdot v_{th,n} \cdot \sigma} \tag{5}$$

where A, n, $v_{th,n}$, and σ are a model parameter, the carrier density, the thermal voltage, and the capture cross section, respectively. Eq. (5) incorporates the trap-property changes resulting from changed bias conditions or temperatures. Consequently, just two physical quantities (density of states (DOS) and τ_d) are sufficient to describe the trap-effect features under any operation condition. The dynamically increasing trap density, as depicted in Fig. 6, is included into the Poisson equation together with the inherent traps,

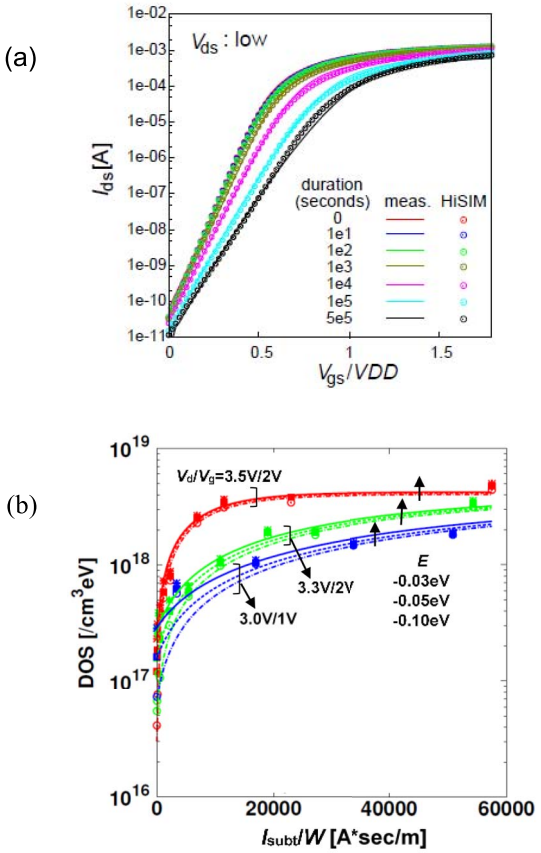

FIGURE 6. (a) Comparison of measured *I-V* aging characteristics under different stress conditions and durations, (b) extracted trap densities from the measured results shown in Fig. 6a [18].

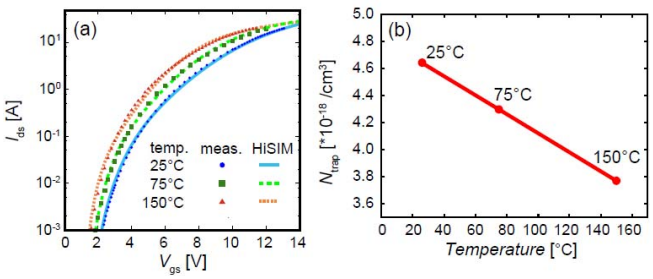

FIGURE 7. (a) Comparison of measured temperature dependence of I_{ds} - V_{gs} to simulation results with HiSIM_HV_SiC (V_{ds} = 10V), and (b) the temperature dependence of N_{trap}. Temperature dependence of N_{trap} is calculated using eqs. (4) and (5) [14].

and is solved iteratively to preserve the model consistency. Here, the trap time constant is explicitly considered as

$$N_{\text{trap}}(t_{\text{i}}) = N_{\text{trap}}(t_{\text{i}-1}) + \frac{\Delta t}{\Delta t + \tau_{\text{d}}}\left[N_{\text{trap,steady}}(V(t_{\text{i}})) - N_{\text{trap}}(t_{\text{i}-1})\right] \tag{6}$$

which is the same treatment as for the non-quasi-static effect modeling of the carrier transit delay as demonstrated in Fig. 9, where $N_{\text{trap,steady}}$ $(V(t_{\text{i}}))$ is the value under the steady-state condition of the bias condition

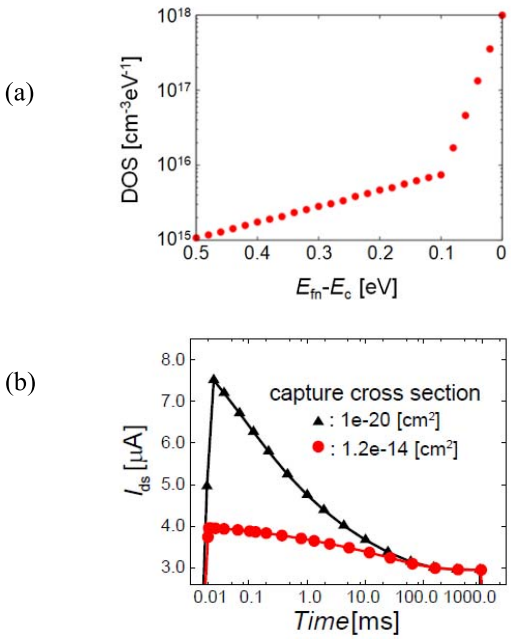

FIGURE 8. 2D-device simulation results, (a) studied trap density of states and (b) transient current characteristics with two different capture cross sections [17].

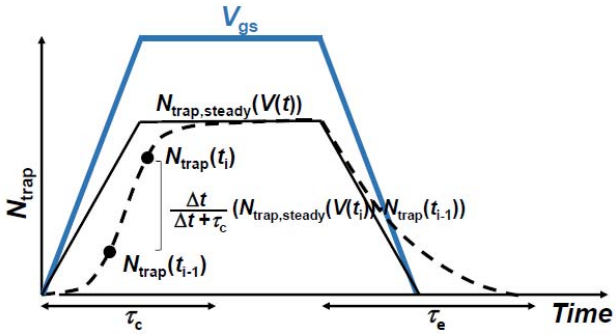

FIGURE 9. Transient features of the trap density N_{trap} according to the switching condition of V_{gs}.

at t_{i} [33], [34]. Different time constants for trapping and detrapping (τ_{c} and τ_{e}) are important to reproduce the frequency dependence of the switching response. The τ_{c} and τ_{e} values are strongly dependent on temperature as well as bias condition applied [12], [35]. Though measured results by Ralls *et al.* [35] are under different conditions from the conventional operation condition, it has been demonstrated that the time constant difference can be easily order of magnitude different. Our observation shows that the difference could be easily the two order of magnitude [36]. Since carriers require time for being trapped/detrapped (τ_{c} / τ_{e}), the trapped-carrier density does not immediately reach the value determined by the DOS, but remains at a much lower level during fast switching (see Fig. 9).

The compact carrier-trapping model has been implemented into the industry-standard MOSFET model HiSIM [37],

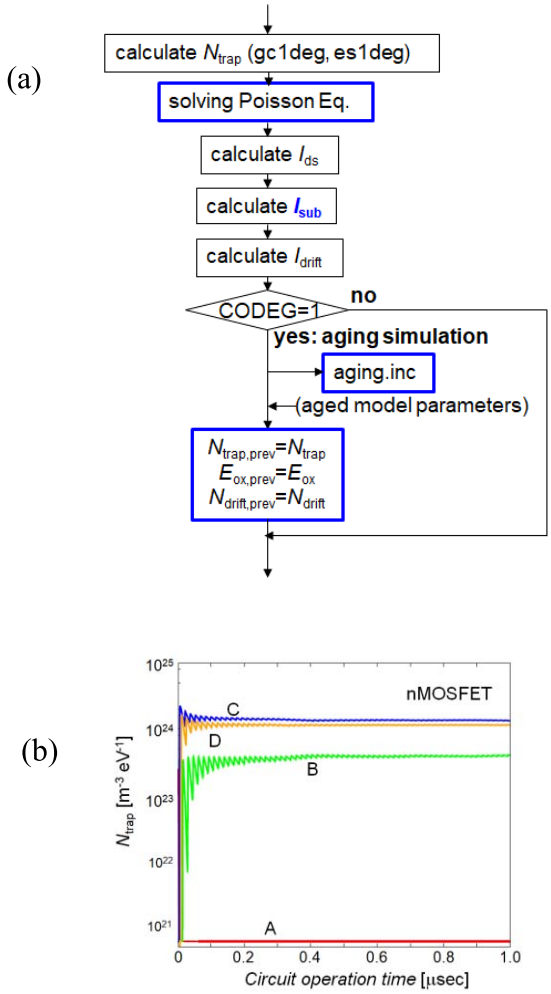

FIGURE 10. **(a) Model implementation into HiSIM, and (b) convergence features, which happen during circuit simulation iteration [31], where A∼D are MOSFETs in the studied circuit.**

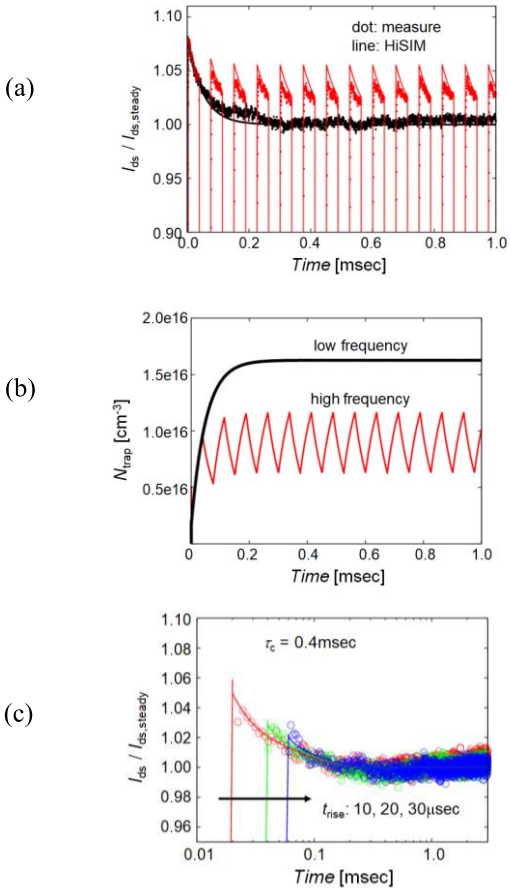

FIGURE 11. **(a) Comparison of measured transient drain currents for two different pulse frequencies (10Hz and 10kHz) to those simulated with HiSIM [18]. (b) Trap density change as a function of time under the two pulse frequencies. (c) Comparison of rise time dependence in switching characteristics, where symbols are measurements and lines are HiSIM results.**

according to the scheme shown in Fig. 10 (left side). As can be seen in Fig. 10 (right side), the trap density is self-consistently determined during circuit simulation. By using the developed model, DC and AC measurements are well reproduced as demonstrated in Figs. 2 and 11. The difference observed for the two devices shown in Fig. 2, are correctly modeled by the N_{trap} and trap-time constant differences. Fig. 11c demonstrates that a fast switching (short rise time t_{rise}) results in a large current peak. This is because the carrier trapping events are not completed during the V_{gs} increase but continue until a stable amount of trapped charge is reached [17]. Therefore, the switching measurement provides the information about the trap-time constant. Fig. 12 shows the long-term aging phenomenon together with the trapping/detrapping effect under repeated switching operation [31]. It is seen that the on/off switching reduces the threshold voltage shift drastically in comparison to the DC stress, because detrapping event happen during switch-off status. This is closer to the reality under the real circuit operation.

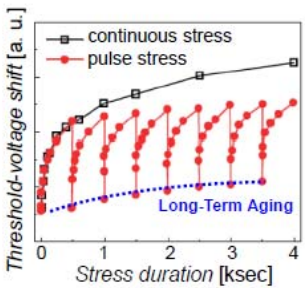

FIGURE 12. **Simulation results comparing DC and pulse conditions as a function of stress duration [30].**

V. CARRIER TRAPPING EFFECT ON CIRCUITS

Fig. 13 shows a DC fitted result of a SiC device, where the measurements verify very strongly degraded *I-V* characteristics in the subthreshold region, which is attributed to the trapping effect [14]. The trap density is extracted from the *I-V* measurements as shown in Fig. 13b. Fig. 14 depicts the test circuit to verify the developed model. Fig. 15 compares the corresponding measured switching characteristics

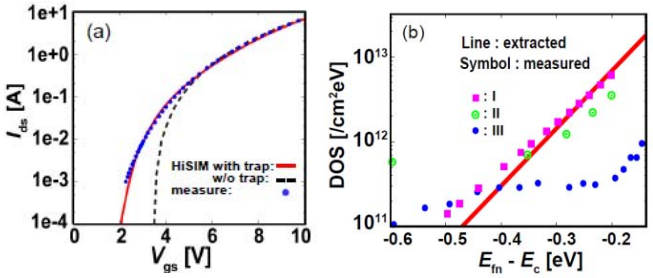

FIGURE 13. (a) Comparison of measured I_{ds}-V_{gs} characteristics to simulation results with and without trap model, and (b) trap density of states (DOS) applied for the calculation. I, II, and III refer to [38]–[40], respectively.

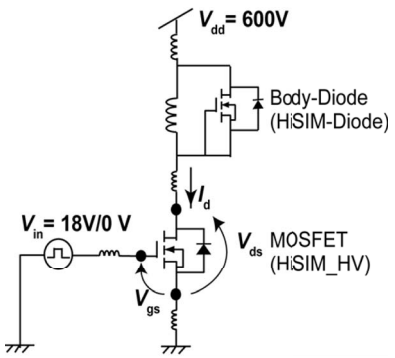

FIGURE 14. Test circuit used for model evaluation of a SiC-MOSFET [14].

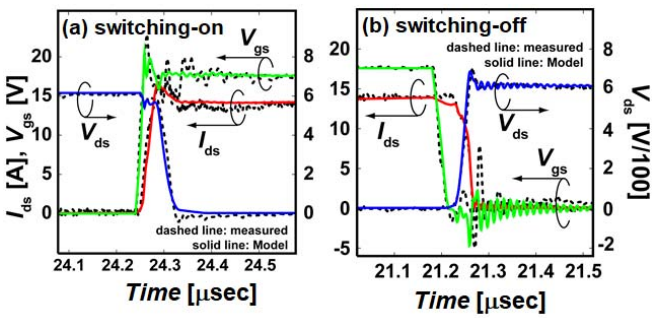

FIGURE 15. Comparison of HiSIM results (solid) to measurements (dashed) during (a) switching-on of a test circuit for a SiC-MOS, and (b) switching-off.

with model results. To reproduce these measurements, the trap-time constants are extracted, which turn out to be different for the carrier trapping (τ_c) and for the carrier detrapping (τ_e). Fig. 16 compares the switching results with and without traps. Since the extracted τ_e is much longer than that of τ_c, no difference between the cases with/without traps is observed during the switching-off, which mean that the switching speed is much faster than the time required for detrapping.

By using the developed model, the switching loss can be accurately calculated as verified in Fig. 17. It is seen that the switching loss becomes larger for higher carrier trapping.

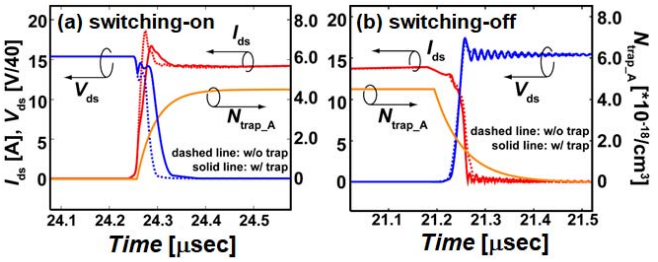

FIGURE 16. Comparison of simulation results during switching-on with traps (solid) and without traps (dashed).

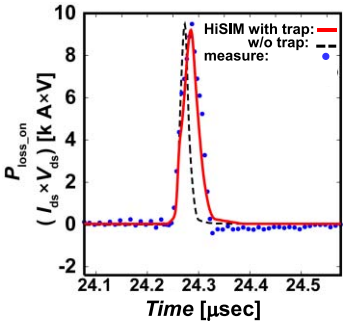

FIGURE 17. Comparison of simulation results for switching-on loss to measurements with traps and without traps.

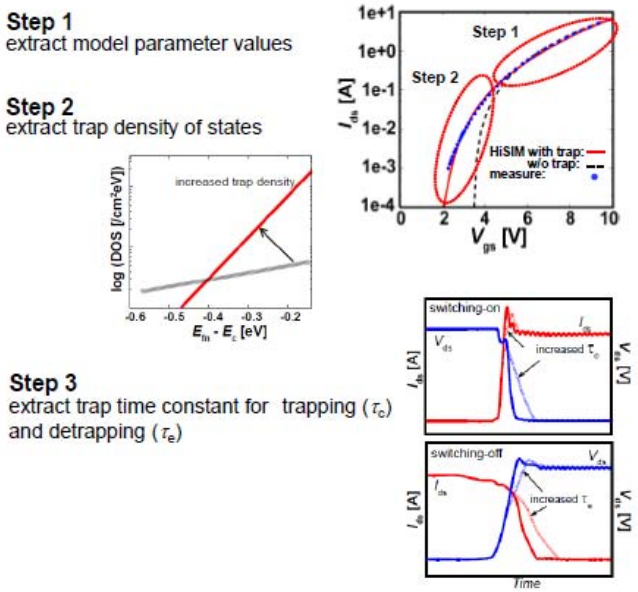

FIGURE 18. Parameter extraction steps for accurate prediction of the power loss in circuits.

VI. DISCUSSION

The goal for circuit simulation is to predict circuit performances accurately, and especially the power loss is an urgent task. To realize accurate prediction, compact modeling is getting more complicated. In spite of the model complexity the model parameter extraction must be done

correctly. Usually measured phenomena are written by simplified model equations with model parameters. Therefore, the model parameters can be extracted with the designated measurements together with the designed device parameter values. Conventionally, *I-V* characteristics together with AC measurements have been used for the extraction. However, accurate prediction of the power loss requires carrier-trap consideration. Therefore it is recommended to extract in steps. The first step is to extract DC-level parameters and then switching measurements are used for the time constants as summarized in Fig. 18. Namely, the DC condition is so specific, that it is actually never observed in real circuit operations. Therefore, the trap density required in the simulation of the *I-V* characteristics is not necessarily the value required for the real circuit operation. This concludes that it is hard to predict the power loss accurately without measured switching performances. Practically, the trap density is reduced during improvements of the fabrication processes, which results in an improvement of the power loss. Consequently, monitoring of the transient device features is suggested as an important addition to the usual monitoring of the threshold voltage.

VII. CONCLUSION

Important features of compact modeling for a new era device and circuit design were discussed. The focus was given on the accurate prediction of the power loss in circuits. It has been demonstrated that reproduction of *I-V* characteristics is not sufficient, but that the transient carrier dynamics must be modeled additionally based on the underlying physics. Here, a compact model for this purpose was proposed by solving the Poisson equation together with the trap density. Though the trap density can be extracted by the *I-V* measurements, the trap-time constant has to be additionally extracted with the measured switching performance. The developed compact model is applicable both for rather short-term dynamically generated traps and also for long-term trapping events which are the origin of the device aging.

ACKNOWLEDGMENT

The authors gratefully acknowledge STARC for long-tern support. Sincere thanks are expressed to Rohm, ams, and Fujitsu for sharing their knowledge about device aging. The authors would like to acknowledge also CMC for its evaluations and evocations of important device problems.

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