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Simulation Study on the Design of Sub- kT/q Non-Hysteretic Negative Capacitance FET Using Capacitance Matching

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ABSTRACT In this paper, approaches to obtain the sub- kT/q non-hysteretic operation mode in negative capacitance (NC) field-effect-transistors for a wide band of applied gate voltages, using capacitance matching, were systematically investigated using TCAD simulation. Unlike certain previous studies, in which the desired operation conditions were received for specific structures and materials, this study presents for the first time a general approach for matching arbitrary MOSFETs with various ferroelectric (FE) materials. This study shows that depending on the initial capacitance matching which represents the best possible subthreshold slope for the preliminary chosen base structure and FE material, any further optimization process can be different. Additionally, for the first time, FE materials were grouped with respect to the shape of their C - V curves in the NC region. This paper shows that with respect to the base structure, certain types of FEs are more preferable to obtain the sub- kT/q operation in a non-hysteretic manner for the wide band of applied voltages. In addition, the impacts of various parameters including the depletion capacitance, supply voltage, gate oxide capacitance, buried oxide capacitance on the capacitance matching were systematically investigated.

INDEX TERMS Negative capacitance, NCFETs, capacitance matching, non-hysteretic, Landau-Khalatnikov equation.

I. INTRODUCTION

Negative capacitance (NC) field-effect-transistors (FETs), with a ferroelectric (FE) layer, connected in series to a conventional MOSFET (base structure), have been widely investigated over the past 10 years [1]–[10]. The NC effect leads to an internal amplification of the input gate voltage, which is proportional to the charge in the FE, and a consequential increase of the drain on-current (in the NC region only), while typically remaining off-current the same. As a result, a sub-60-mV/decade subthreshold slope (SS) can be obtained at room temperature with a slight process modification from the conventional CMOS technology.

The key to obtaining the desired operation mode is the appropriate capacitance matching, during the design procedure, between the capacitance of the FE layer (C_{FE}), the

buffer oxide capacitance (C_{ox}), and the total capacitance of the underlying base MOSFET (C_{MOS}) shown in Fig. 1. The required capacitance relations have been explained in detail in [2] and [11]–[17], giving the sub- kT/q condition as

$$|C_{FE}| < C_{ox}, \quad (1)$$

while the non-hysteretic one is

$$|C_{FE}| > C_{MOS}, \quad (2)$$

In the case when C_{FE} is negative. Keep in mind that condition (1) is necessary, however, not sufficient, because it is based on the conventional equation of SS , and does not take into account the impact of parasitic effects, which also will not be investigated in this study. It is important to fulfill conditions (1)–(2) for the wide band of applied gate

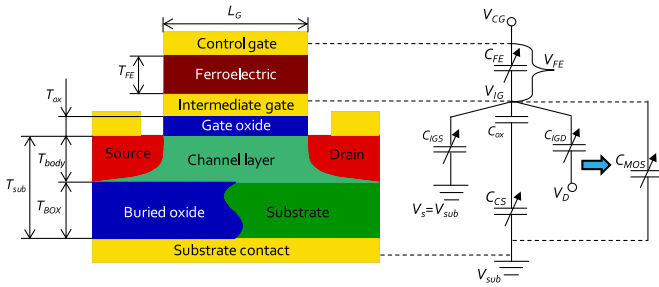


FIGURE 1. Schematics of the investigated bulk and SOI NCFETs (left) and their equivalent capacitance model (right).

voltages, especially for the subthreshold region of the base structure. However, satisfying these conditions at the same time can be extremely difficult, therefore, an overwhelming numbers of reported structures have hysteresis [3]–[10] and/or have a sub- kT/q slope for only a few decades of drain current [6], [18], [19].

In this study, we systematically investigated approaches to obtain a non-hysteretic sub- kT/q operation regime using capacitance matching. With respect to the shape of the capacitance characteristics, the FE materials were grouped together. It has been shown that approaches to perform capacitance matching for different types of FE materials can be different. Additionally, the impacts of various factors including the depletion capacitance, supply voltage, gate oxide capacitance, and buried oxide capacitance on the capacitance matching conditions were systematically investigated. Unlike some previous studies, in which the desired operation conditions were achieved for specific structures and materials [2], [11]–[13], [16], [18], [20], [21], this study presents, for the first time, a general approach to match arbitrary MOSFETs, such as bulk or semiconductor-OI FETs that can be used in ultra-thin-body FETs even for monolithic 3D integration (M3D) [22], [23], with various FE materials. As a result, this paper provides an outline to design sub- kT/q non-hysteretic NCFETs.

II. INVESTIGATED STRUCTURE AND SIMULATION METHOD

The schematic of the investigated NCFETs and corresponding capacitance model are shown in Fig. 1. In this study, mainly n-channel structures were investigated; however, the simulation approach is also valid for p-channel NCFETs because according to [3], [5], [8], and [10], the operation principle and equivalent capacitance models of the p-type NCFETs are same as for the n-type structures. It will additionally be proven in chapter VI. That the C_{CS} represents the total capacitance between the channel and substrate contact. In the case of the “on-insulator” (–OI) FET, the C_{CS} in the depletion and weak inversion region should be calculated as a series connection for the semiconductor layer and buried oxide (BOX).

In the general case, capacitance can be defined as follows:

$$C = \frac{dQ}{dV}, \quad (3)$$

where Q is the charge stored on the capacitor’s conductive plates, and V is the applied voltage. Therefore, C_{MOS} can be calculated as follows:

$$C_{MOS} = \frac{dQ_t}{d(V_{IG} - V_{Sub})}, \quad (4)$$

where Q_t is the total charge of the intermediate gate (absolute value is equal to the charge stored in channel layer Q_i), which equals the charge in the FE layer: $Q_t = Q_{FE} = |Q_i|$. Similarly, the FE layer capacitance can be defined as follows:

$$C_{FE} = \frac{dQ_t}{dV_{FE}}, \quad (5)$$

where V_{FE} is the voltage drop in the FE given by the Landau-Khalatnikov (L-K) equation (in the static state) [1]:

$$V_{FE} = \left(2\alpha Q_t + 4\beta Q_t^3 + 6\gamma Q_t^5\right) T_{FE}, \quad (6)$$

where α , β , and γ are the Landau coefficients of the FE material, and T_{FE} is the FE thickness. Using (5-6), the C_{FE} can be calculated as follows:

$$C_{FE} = \frac{1}{(2\alpha + 12\beta Q_t^2 + 30\gamma Q_t^4) T_{FE}}. \quad (7)$$

The simulation approach was divided into two phases similarly to [13]–[16], [20], [21], and [24]: the first step was the 2D simulation of the base FET in the commercial TCAD software, from which the potential and charge distribution Q_i vs V_{IG} as well as the transfer characteristics were determined. The second phase was a capacitance matching procedure to fulfill conditions (1)–(2), using (7), with further calculation of V_{CG} using the L-K equations as follows:

$$V_{CG} = V_{IG} + V_{FE}, \quad (8)$$

in order to receive the transfer characteristic of the NCFET. Unlike [12], [14], [19], and [21], we used the C - V characteristics for the capacitance matching instead of C - Q , which, as we believe, makes understanding the matching more intuitive.

Additionally, for our investigation, we neglected the impact of the T_{FE} on P - E characteristic of the FE and as a result, on the Landau coefficients. However, for real FE layers, such a dependence might exist [25]–[27]. Therefore, to increase the probability of accurate matching during the design procedure, the dependence of the hysteresis curve on the T_{FE} should be investigated separately.

III. INITIAL CAPACITANCE MATCHING

The NCFET design process should start by choosing the desired base MOSFET and FE material. In this study, the initial capacitance matching was defined as a procedure to calculate the ideal FE thickness $T_{FE} = T_i$, such that the non-hysteretic condition (2) is fulfilled for the whole operation band of V_{IG} , while single or multiple values of V_{IG} exist,

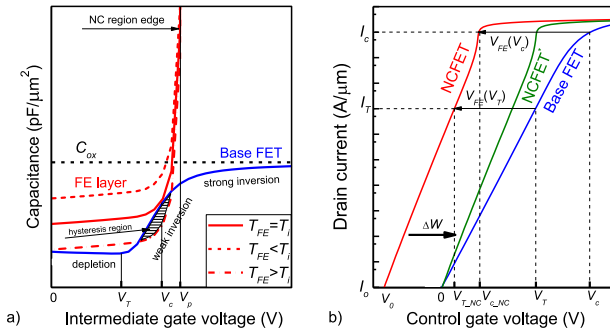


FIGURE 2. Outline of the capacitance (a) and transfer (b) characteristics of the NCFET with respect to the base FET, obtained during the initial matching with key voltage designations.

where $|C_{FE}| = C_{MOS}$. Such a voltage was designated as the critical voltage V_c shown in Fig. 2 (a). In the case of multiple values, V_c should be the closest point to the strong inversion region.

If V_c is situated in the weak inversion region, it helps to improve the slope of the transfer characteristic in that part of the weak inversion region too. To take into account such an improvement, we introduced the extended slope (*ES*) — the average slope of the transfer characteristic for both the depletion (*SS*) and part of the week inversion characteristic, where $V_{CG} < V_c$. Using *ES* instead of the average *SS* is more informative for the transfer characteristics, which have an additional improvement of the slope at least for 1 decade and do not have saturation of the slope between the threshold voltage V_T and V_c . Therefore, with respect to Fig. 2 (b), the *ES* can be calculated as follows:

$$ES = SS \cdot \frac{\#dec1}{\sum dec} + \frac{V_{c_NC} - V_{T_NC}}{\log(I_c) - \log(I_T)} \cdot \frac{\#dec2}{\sum dec} = \frac{V_{c_NC} - V_0}{\log(I_c) - \log(I_0)}, \quad (9)$$

where V_0 and I_0 correspond to the control gate voltage and drain current at the beginning of the depletion region, and $\#dec1$ and $\#dec2$ are the numbers of decades for the *SS* and weak inversion extension, while $\sum dec = \#dec1 + \#dec2$.

In cases when the work function of the intermediate gate contact W_{IG} is smaller than the work function of the channel layer W_c , a significant negative charge Q_i can be induced at $V_{IG} = 0$ V, resulting in the increase of the off-current. To keep the off-current the same, additional work function engineering can be performed [28], changing the control gate work function by ΔW , such as $V_{FE} = 0$ V at $V_{IG} = 0$ V (green line in Fig. 2 (b)). The engineering of the gate work function does not impact the mutual arrangement of the capacitance characteristics.

A change in the T_{FE} does not change the shape of C_{FE} according to (7), and only shifts its vertical position, as shown in Fig. 2 (a). If $T_{FE} > T_i$, the non-hysteretic condition (2) is not fulfilled in a certain area; however, the *SS* in this area can significantly improve because of the bigger amplification of the applied voltage according to (6). On the

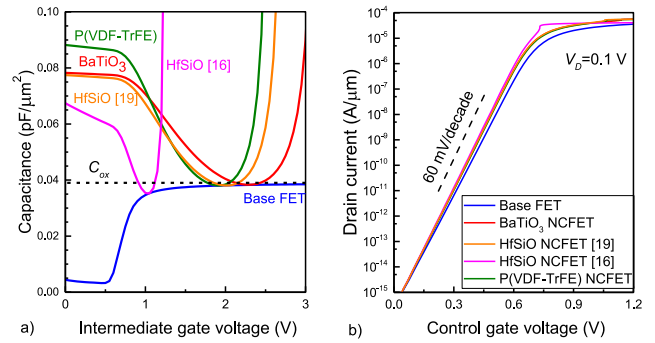


FIGURE 3. Capacitance characteristics of the T1-based NCFETs' FE layers: BaTiO₃ [1] ($T_{FE} = 635$ nm), HfSiO [20] ($T_{FE} = 16$ nm), HfSiO [16] ($T_{FE} = 5$ nm), P(VDF-TrFE) [4] ($T_{FE} = 3$ nm), with respect to the C_{MOS} of base FET (a). Transfer characteristics of the T1-based NCFETs (b), with respect to the base FET. Values of ΔW are presented in Tab. 2.

other hand, if $T_{FE} < T_i$, condition (2) is still valid; however, the improvement of the *SS* is reduced compared to the ideal case. Thus, the initial matching corresponds to the best possible *SS* for the preliminary chosen base structure and FE, in the case when the non-hysteretic condition is fulfilled for the whole band of the applied gate voltages. Such a procedure is necessary to evaluate the possibility of a desired operation regime. If achieved during the initial matching, the *SS* is not satisfactory, and its improvement can only be achieved by modification of the base structure or by using another FE material. Depending on the initial position of V_c as well as the shape of the capacitance characteristic of the FE material, further actions to achieve the desired operation mode can be different, and will be discussed in the next section.

IV. SHAPE OF THE C-V CHARACTERISTICS

The shape of the C_{MOS} vs V_{IG} characteristic does not change with respect to the geometry of the base FET. With an increase of the applied gate voltage, the capacitance C_{MOS} moves through the accumulation, depletion, weak, and strong inversion regions. However, with respect to the shape of the C_{MOS} , the C_{FE} vs V_{IG} characteristics can be grouped mainly in accordance with the Landau coefficients. Use of such a grouping is a helpful and important approach for FE selection, to achieve the desired operation regime.

A MOSFET with a relatively long channel ($L_G = 500$ nm) was chosen as a base structure to avoid parasitic effects, which hides the prediction of the intrinsic performance of the NC-FET. The impact of the short-channel effects, as well as other parasitic parameters, such as the interface and volume defects, will be left for future discussions. The other parameters of the base FET were as follows: $T_{ox} = 5$ nm, $\epsilon_{ox} = 22$ (EOT = 1.13 nm), $T_{body} = 10$ nm, $T_{sub} = 500$ μ m, $n+$ source/drain doping concentrations $N_{S/D} = 1 \cdot 10^{20}$ cm⁻³, Si channel and substrate with p doping concentration $N_{ch} = N_A = 1 \cdot 10^{18}$ cm⁻³, $L_{S/D} = 250$ nm, and $W_{IG} = 4.71$ eV. The average *SS* of the base MOSFET is 67.5 mV/dec for 7 decades. Because our main goal is the

TABLE 1. Landau Coefficients of the FE Materials, Used in (6-7) to Calculate the Voltage Drop in the FE Layer and FE Capacitance.

FE type	Material	Landau coefficients			Ref.
		α [m/F]	β [m ⁵ /F/C ²]	γ [m ⁹ /F/C ⁴]	
1	BaTiO ₃	$-1 \cdot 10^7$	$-8.9 \cdot 10^8$	$4.5 \cdot 10^{10}$	[1]
	HfSiO (1)	$-4 \cdot 10^8$	$-5.1 \cdot 10^{10}$	$3.7 \cdot 10^{12}$	[20]
	HfSiO (2)	$-1.45 \cdot 10^9$	$-2.5 \cdot 10^{12}$	$2.45 \cdot 10^{15}$	[16]
	P(VDF-TrFE)	$-1.98 \cdot 10^9$	$-3.75 \cdot 10^{11}$	$3.16 \cdot 10^{13}$	[4]
2	PZT (1)	$-4.24 \cdot 10^8$	$2.3 \cdot 10^8$	$3.8 \cdot 10^{10}$	[19]
	HZO	$-7 \cdot 10^8$	$1 \cdot 10^{12}$	0	[11]
	SBT	$-1.3 \cdot 10^8$	$1.3 \cdot 10^{10}$	0	[15]
	Y-HfO ₂	$-1.23 \cdot 10^9$	$3.28 \cdot 10^{10}$	0	[12]
3	PZT (2)	$-1.48 \cdot 10^8$	$-3 \cdot 10^7$	$2.47 \cdot 10^8$	[29]
	Pb(Nb _{0.04} Zr _{0.28} Ti _{0.68})O ₃	$-5.37 \cdot 10^7$	$-3 \cdot 10^7$	$2.47 \cdot 10^8$	[30]

sub- kT/q operation for the wide band of applied voltages, the average SS for the whole depletion region was considered.

• The first type (T1) of FEs mostly includes first order phase transition materials with negative α and β Landau coefficients, and $|\beta| > |\alpha|$. With an increase of V_{IG} in the NC region, the value of $|C_{FE}|$ for such materials decreases until it reaches its' minimum:

$$|C_{FE(\min)}| = \left[T_{FE} \left(2\alpha - \frac{6\beta^2}{5\gamma} \right) \right]^{-1}, \quad (10)$$

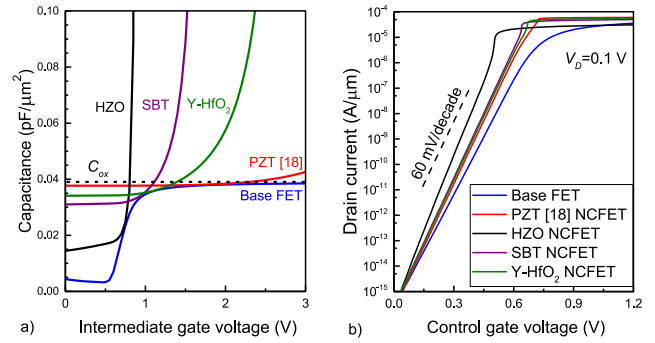
and then starts increasing until the end of the NC region. Fig. 3 shows the capacitance (a) and transfer (b) characteristics obtained during initial matching of the NCFETs, based on T1 materials such as: BaTiO₃ [1], P(VDF-TrFE) [4] and HfSiO from [16] and [20] with respect to the base FET. For the FE layers, only absolute values for the capacitances in the NC region will be shown because the desired operation can be obtained only in this region. For the BaTiO₃, P(VDF-TrFE) and HfSiO [16] NCFETs, the critical voltages are situated in the strong inversion region, resulting in a very short band of voltages, where the sub- kT/q condition (1) is fulfilled, while for the HfSiO [19] NCFET, it is situated closer to the weak inversion region, making the sub- kT/q band slightly wider. However, in the depletion region, such a condition does not fulfill all of the abovementioned NCFETs. Therefore, the slope of the transfer curve can be significantly improved only in the strong inversion region, while the average SS remains bigger than 60 mV/decade; however, it improves compared to the base FET due to the NC effect (see Table 2). Thus, the base structure should be optimized to shift V_c closer to the depletion region and extend the sub- kT/q band towards the depletion area.

• The second type (T2) differs from the previous case by a continuous increase of the absolute value of $|C_{FE}|$ with an increase of V_{IG} until the end of the NC region. Such a shape can be achieved when β is positive (second order transmission materials), as well as negative, while $|\beta| < |\alpha|$ and $\gamma \gg |\alpha|$.

Fig. 4 shows the corresponding capacitance (a) and transfer (b) characteristics after the initial matching of the T2-based NCFETs with the FE layers made of PZT [19], HZO [11], SBT [15], and Y-HfO₂ [12] with respect to the

TABLE 2. Comparison of NCFET Efficiencies Based on Different Types of FEs.

FE type	Material	V_D [V]	Output parameters of NCFETs			
			$SS(ES^*)$ [mV/dec]·#decades	V_T [V]	ΔW [eV]	I_{on} [A/ μ m] at $V_{CG} = 1.2$ V
—	w/o FE	0.1	$67.5 \cdot 7$	0.5	0	$3.58 \cdot 10^{-5}$
1	BaTiO ₃	0.1	$64.0 \cdot 7$	0.475	0.043	$5.63 \cdot 10^{-5}$
	HfSiO (1)	0.1	$64.0 \cdot 7$	0.475	0.043	$5.55 \cdot 10^{-5}$
	HfSiO (2)	0.1	$63.0 \cdot 7$	0.468	0.05	$4.08 \cdot 10^{-5}$
	P(VDF-TrFE)	0.1	$64.4 \cdot 7$	0.479	0.038	$4.45 \cdot 10^{-5}$
2	PZT (1)	0.1	$60.7 \cdot 7$	0.465	0.095	$6.1 \cdot 10^{-5}$
	HZO	0.1	$50.3 \cdot 7 (47.3 \cdot 10^*)$	0.377	0.28	$3.1 \cdot 10^{-5}$
	SBT	0.1	$59.0 \cdot 7$	0.44	0.112	$4.99 \cdot 10^{-5}$
	Y-HfO ₂	0.1	$60.0 \cdot 7$	0.446	0.1	$5.56 \cdot 10^{-5}$
3	PZT (2)	0.1	$61.0 \cdot 7$	0.452	0.085	$6.45 \cdot 10^{-5}$
	Pb(Nb _{0.04} Zr _{0.28} Ti _{0.68})O ₃	0.1	$61.0 \cdot 7$	0.453	0.05	$6.40 \cdot 10^{-5}$

**FIGURE 4.** Capacitance characteristics of the FE layers of T2-based NCFETs: PZT [19] ($T_{FE} = 31$ nm), HZO [11] ($T_{FE} = 60$ nm), Y-HfO₂ [12] ($T_{FE} = 11$ nm), SBT [15] ($T_{FE} = 128$ nm), with respect to the base FET (a), obtained during initial matching. Relevant transfer characteristics for T2-based NCFETs with respect to the base FET (b). Values of ΔW are presented in Tab. 2.

base FET, introduced before. All of the abovementioned NCFETs fulfill condition (1) for the whole subthreshold and weak inversion regions, helping to improve the SS and in certain cases the ES , which is a significant advantage over T1-based NCFETs.

For the investigated HZO NCFET, it shows an $SS = 50.3$ mV/dec for 7 decades ($I_D = 10^{-15}$ - 10^{-8} A/ μ m) and an $ES = 47.3$ mV/dec for 10 decades ($I_D = 10^{-15}$ - 10^{-5} A/ μ m). However, other T2-based NCFETs have $SS \approx \ln(10) \cdot kT/q$. The reason is the inappropriate relations between layers' capacitances.

According to [1], the SS of NCFET can be defined as follows:

$$\begin{aligned} SS_{NC} &= \frac{kT}{q} \left(1 + \frac{C_{CS}}{C_{ox}} \right) \cdot \frac{C_{FE} + C_{MOS}}{C_{FE}} \\ &= \frac{kT}{q} \left(1 + \frac{C_{CS}}{C_{ox}} + \frac{C_{CS}}{C_{FE}} \right) \end{aligned} \quad (11)$$

In the case of the NC regime, the FE capacitance C_{FE} can be replaced by $-|C_{FE}|$. To obtain the steepest sub- kT/q slope, C_{CS} should be the highest possible, while $|C_{FE}|$ should be as far as possible from C_{ox} , and as close as possible to C_{MOS} (until they fulfill conditions (1)-(2)). For PZT, SBT and Y-HfO₂ $|C_{FE}| \approx C_{ox}$ and $C_{CS} \ll C_{ox}$, resulting in

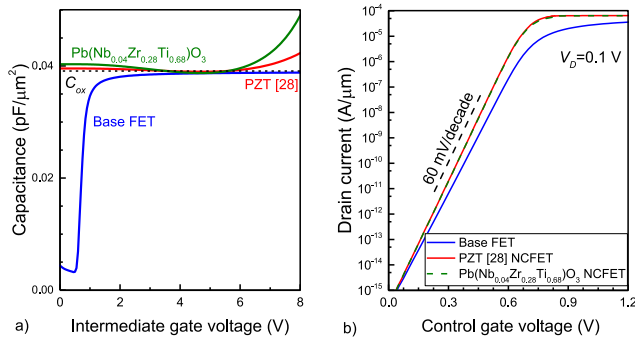


FIGURE 5. Capacitance characteristic of the T3 PZT [29] ($T_{FE} = 86$ nm) and $\text{Pb}(\text{Nb}_{0.04}\text{Zr}_{0.28}\text{Ti}_{0.68})\text{O}_3$ [30] layers ($T_{FE} = 230$ nm) (a), with respect to the capacitance of the base FET obtained during initial matching. Relevant transfer characteristics of the NCFETs with respect to the base structure (b). Values of ΔW are presented in Tab. 2.

$\frac{C_{CS}}{C_{ox}} - \frac{C_{CS}}{|C_{FE}|} \approx 0$. Therefore, certain T2-based NCFETs require additional structure optimization.

One can notice, that the SS of PZT (1) NCFET is bigger than 60 mV/dec, while according to condition (1) it should be less. The reason is the presence of parasitic capacitances between the gate and source/drain, which are present in the depletion region, increasing the actual SS of the base structure compared to the SS calculated using the conventional equation.

Additionally, of note is that the on-current of the HZO-based NCFET decreased compared to the base FET. It is related to the width of the NC region of the capacitance characteristic. The maximum intermediate gate voltage, corresponding to the transition from the negative to positive regions of the FE, has been defined as V_P and is introduced in Fig. 2 (a). For the HZO NCFET, V_P is situated in the weak inversion region, and when C_{FE} becomes positive, according to (11), SS increases, leading to saturation of the transfer characteristic as shown in Fig. 4 (b) (black line). Therefore, to have the same on-current as in the base FET, V_P should be situated in the strong inversion region.

However, for such a case, it is highly possible that V_c will also be situated in the strong inversion region resulting in a narrow sub- kT/q band for a T1-based NCFET, and $|C_{FE}| \approx C_{ox}$ for a T2-based one, which is not preferable for the desired operation mode. Thus, for certain structures, it should be a trade-off between a decrease in the SS and an increase in the on-current. We believe that the optimal solution is when V_c situated in the weak inversion region, resulting in a slight drop of the on-current, while the sub- kT/q condition is fulfilled for the whole depletion region, which enables a significantly improved SS in this region.

- The third type (T3) of FE materials is actually a particular case of T1 or T2 and differs from them by a significantly smaller dC_{FE}/dV_{IG} slope in the NC region as well as by the position of V_c which is situated far away from V_T . T3 materials have a small value for $|\alpha|$ and $|\beta|$ (both about on the order of 10^7 SI units), which can be noticed by the very gentle slope of the P - E curve in the NC region.

Fig. 5 (a) and (b) shows, respectively, the capacitance and transfer characteristics of NCFETs based on T3 PZT [29] and $\text{Pb}(\text{Nb}_{0.04}\text{Zr}_{0.28}\text{Ti}_{0.68})\text{O}_3$ [30] layers. An average SS of 61 mV/dec for 7 decades was obtained for both NCFETs. However, to achieve a sub- kT/q operation, V_c should be shifted much closer to the depletion region, which requires a significant modification of the base structure, which will be discussed in the next section.

A list of the FE materials used in this article, and their parameters are shown in Tab. 1. An efficiency comparison of the NCFETs, based on these FE materials, is presented in Tab. 2. As shown in Tab. 2, V_T and I_{on} represent structures with additional work function engineering, if $\Delta W \neq 0$.

However, further investigations have been performed on only certain materials. HfSiO , discussed in [16], has been used as a T1 material, because it required minimal modifications of the base structure, while HZO [11] and SBT [15] have been used as T2 materials. The reason why we investigated two T2 materials is the positions of their V_c situated in different operation regions (weak inversion for HZO and strong inversion for SBT) during the initial matching, while all T1 materials have V_c situated in the strong inversion region. We did not investigate T3-based NCFETs separately because the approach on their matching is the same as the other types of the FE materials; however, they require more significant modifications of the base structure.

V. FACTORS THAT AFFECT THE CAPACITANCE MATCHING

In the following section, we will discuss factors that can be used to improve matching conditions and decrease the SS . Critical voltages, used during capacitance matching procedures of modified structures, have also been referred as V_c .

A. DEPLETION CAPACITANCE C_D

The depletion capacitance in conventional bulk structure is equal to C_{CS} , while for $-OI$ structures, C_D becomes a part of C_{CS} . An increase of C_D increases V_T as well as the total capacitance C_{MOS} in the depletion region and the total gate charge Q_t . An increase of Q_t leads to an increase of the negative voltage drop in FE, according to (6), and as a result, to a shift of the C_{FE} to smaller values of V_{IG} . Consequently, V_c can also become shifted towards lower values of V_{IG} , which can lead to an extension of the sub- kT/q band, in the case when T_{FE} is increased, while conditions (1)-(2) are fulfilled. C_D can be increased by a change in the following parameters for the channel layer (for bulk epi-MOSFETs and $-OI$ MOSFETs): a decrease of thickness T_{ch} , increase of dielectric permittivity and increase of doping concentration N_{ch} as well as by the following parameters for the substrate (for all types of bulk MOSFETs): a decrease of thickness T_{sub} and increase of the opposite channel doping concentration N_A .

Fig. 6 shows the capacitance (a) and transfer (b) characteristics of the T1-based HfSiO NCFET after the second

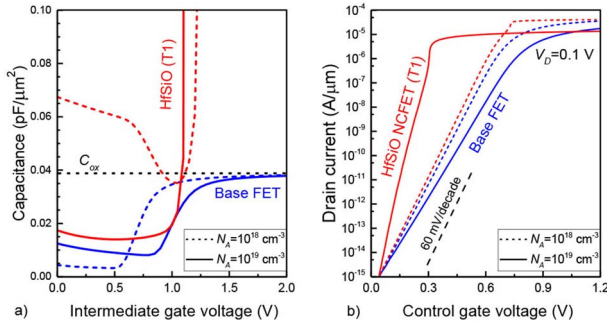


FIGURE 6. Effect of the C_D increase on the capacitance (a) and transfer (b) characteristics of T1 HfSiO NCFET ($T_{FE} = 12$ nm) with respect to the initial matching. Values of ΔW are presented in Tab. 3. To improve the visual perception of the results, the V_{CG} for the structure with $N_A = 10^{19} \text{ cm}^{-3}$ was decreased by 0.25 V. The parameters of the base structure remain unchanged.

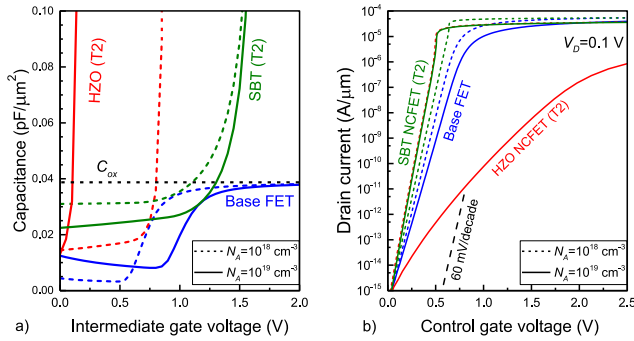


FIGURE 7. Effect of C_D increase on the capacitance (a) and transfer (b) characteristics of T2 HZO ($T_{FE} = 175$ nm) and SBT NCFETs ($T_{FE} = 183$ nm) with respect to the initial matching. Values of ΔW are presented in Tab. 3. The V_{CG} for the structure with $N_A = 10^{19} \text{ cm}^{-3}$ was decreased by 0.25 V. The parameters of the base structure remain unchanged.

capacitance matching procedure for a modified base structure with $N_A = 1 \cdot 10^{19} \text{ cm}^{-3}$, with respect to the initial matching results. The shift of the V_c to the weak inversion region as well as the increase of C_{CS} helped to improve the SS to 29.3 mV/dec for 7 decades and the ES to 28.8 mV/dec for 9 decades. However, due to the shift of V_p and the contraction of the NC band's width, the on-current decreased compared to the initial matching.

In the case of T2-based NCFETs, shown in Fig. 7, an increase of C_D led to an improvement of the SS of 49.6 mV/dec for 7 decades and the ES of 46.7 mV/dec for 9 decades for the SBT NCFET. However, for the HZO NCFET, the shift of the V_c and V_p significantly narrowed the NC region, moving V_p to the depletion region. As a result, the performance of this NCFET significantly worsened in the whole subthreshold region. Tab. 3 shows a comparison of the efficiency of the investigated T1- and T2-based NCFETs with the different N_A .

Thus, an increase of C_D is more beneficial for T1- and T2-based NCFETs, which after the initial matching have V_c situated in the strong inversion region, and by the increase

TABLE 3. Impact of N_A on Efficiency of NCFETs.

FE type	Material	Factor		Output parameters of NCFETs			
		N_A [cm^{-3}]	V_D [V]	SS (ES^*) [mV/dec] · #decades	V_T [V]	ΔW [eV]	I_{on} [A/ μm] at (V_{CG})
—	w/o FE	10^{18}	0.1	$67.5 \cdot 7$	0.5	0	$3.58 \cdot 10^{-5}$ (1.2 V)
		10^{19}	0.1	$77.6 \cdot 7$	0.8	0	$1.90 \cdot 10^{-5}$ (1.5 V)
1	HfSiO (2)	10^{18}	0.1	$63.4 \cdot 7$	0.468	0.05	$4.08 \cdot 10^{-5}$ (1.2 V)
		10^{19}	0.1	$29.3 \cdot 7$ (28.8 · 9*)	0.48	0.59	$1.37 \cdot 10^{-5}$ (1.5 V)
2	HZO	10^{18}	0.1	$50.3 \cdot 7$ (47.3 · 10*)	0.377	0.28	$3.07 \cdot 10^{-5}$ (1.2 V)
		10^{19}	0.1	218 · 7	1.71	1.73	$1.34 \cdot 10^{-6}$ (3 V)
	SBT	10^{18}	0.1	$59.1 \cdot 7$	0.44	0.112	$4.99 \cdot 10^{-5}$ (1.2 V)
		10^{19}	0.1	$49.6 \cdot 7$ (46.7 · 9*)	0.61	0.55	$3.06 \cdot 10^{-5}$ (1.5 V)

of C_D can be shifted towards the depletion region with an extension of the sub- kT/q band. It is also beneficial for T3-based NCFETs; however, they require more significant changes of C_D , compared to T1- and T2- based structures, which in certain cases cannot be implemented due to technological difficulties. However, for certain T1- and T3-based NCFETs with a narrow sub- kT/q band, when an increase of C_D is not enough to extend a such band, the SS deteriorates, similar to the conventional MOSFET. If V_c is situated in the weak inversion region, an insignificant increase of C_D can be beneficial to decrease the SS (C_{FE} becomes closer to C_{MOS}); however, it will definitely decrease the on-current. For structures that have V_c at the depletion region, an increase of C_D will lead to a significant contraction of the NC region and degradation of the SS; therefore, for such structures, a decrease of C_D is a more preferable solution to move V_c towards the weak inversion region.

B. SUPPLY VOLTAGE V_D

Supply voltage manipulation, to achieve a desired operation regime, is the most contradictory approach, because a high supply voltage is not preferable in terms of power saving and can lead to parasitic effects, such as channel length modulation, gate induced drain leakage, drain induced barrier lowering, hot carrier injection etc. as well as does not always lead to improvement of the SS. However, for certain structures, such improvement can be achieved, therefore, this factor cannot be ignored. Additionally, the choice of supply voltage is important during the design procedure of NCFETs and will be discussed later.

In the weak inversion region, after the thin channel is formed, it starts having a role as a terminal, shielding the substrate from the gate. At this time, the gate-source C_{IGS} and gate-drain C_{IGD} capacitances start increasing, and in the strong inversion region their sum will become very close to C_{ox} . By the increase of V_D , the rate of increase of C_{IGS} and C_{IGD} and as a result, the C_{MOS} vs V_{IG} curve in the weak and in the beginning of the strong inversion regions can be manipulated. Usually, after the initial matching of T1- and T2-based NCFETs, V_c is situated in one of the

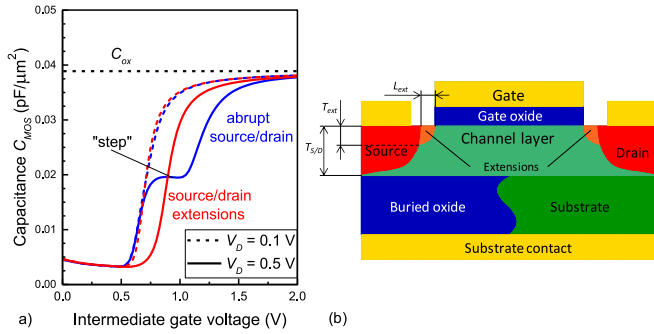


FIGURE 8. Capacitance characteristics of the initial base structure with abrupt S/D engineering and modified structure with S/D extensions, under different supply voltages (a) Parameters of extensions: $N_{ext} = 2 \cdot 10^{18} \text{ cm}^{-3}$, $T_{ext} = 5 \text{ nm}$, $L_{ext} = 2 \text{ nm}$. Schematic of base FET with improved S/D engineering (b).

abovementioned regions, therefore, with high probability, a change of V_D will affect the position of V_C .

The shape of C_{MOS} vs V_{IG} in the weak inversion region under different supply voltages depends on the source/drain (S/D) engineering. The base FET, shown in Fig. 1, has abrupt transitions between the highly doped $n+$ S/D regions and p -doped channel. Depending on the values of $N_{S/D}$, T_{ch} and V_D , the capacitance characteristic of such a structure in the weak inversion region can have an area with a significantly smaller dC_{MOS}/dV_{IG} slope compared to the characteristic obtained for $V_D \approx 0 \text{ V}$. Such an area is shown in Fig. 8 (a), and will be referred as the “step”. It appears that the electric field, created by the supply voltage and highly doped S/D regions, can produce an area with a high hole concentration, situated close to the edge of a highly doped drain region.

Another type of S/D engineering is shown in Fig. 8 (b). Such a shape is used to suppress parasitic short-channel effects, which is achieved by the creation of extensions with $N_{ext} = N_{S/D}$. In our case, even extremely thin extensions with $T_{ext} = 1 \text{ nm}$, $L_{ext} = 10 \text{ nm}$ and $N_{ext} = N_{S/D}$ still cause the “step”. Therefore, the following parameters for the extensions were used for further investigations: $N_{ext} = 2 \cdot 10^{18} \text{ cm}^{-3}$, $L_{ext} = 2 \text{ nm}$ and $T_{ext} = 5 \text{ nm}$. The capacitance characteristics of the base FETs with abrupt S/D engineering and extensions under different supply voltages are shown in Fig. 8 (a). As we can see, for the structure with the extensions, the “step” in the weak inversion region is absent.

Fig. 9 shows the capacitance matching of the HfSiO FE layer and original base FET for $V_D = 0.1 \text{ V}$ and $V_D = 0.5 \text{ V}$. With the increase of V_D , the sub- kT/q band is expanded. However, this band still has not covered the depletion region completely, and the insignificant improvement of the SS from 63.4 to 62.0 mV/dec for 6 decades, happened because of the decrease of $|C_{FE}|$ in the depletion region.

The corresponding characteristics of a NCFET, based on a modified structure with S/D extensions, are shown in Fig. 10. Due to the presence of the extensions, the depletion width slightly decreased, making the SS of such a base

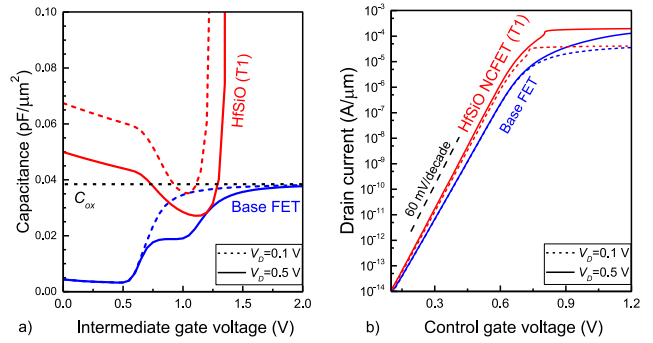


FIGURE 9. Effect of the supply voltage change from 0.1 V to 0.5 V on the capacitance (a) and transfer (b) characteristics of the T1 HfSiO NCFET ($T_{FE} = 6 \text{ nm}$) with respect to the initial matching. Values of ΔW are given in Tab. 4. The base structure remains unchanged.

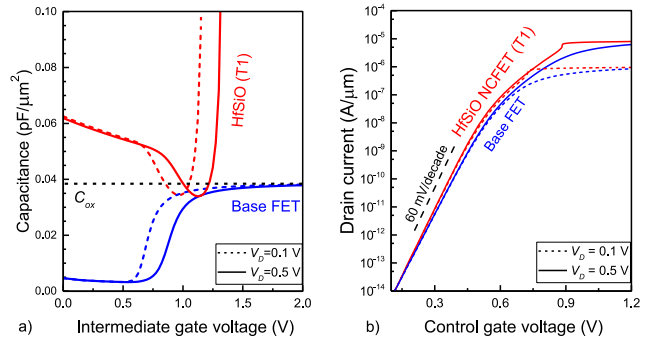


FIGURE 10. Effect of the supply voltage change from 0.1 V to 0.5 V on the capacitance (a) and transfer (b) characteristics of the T1 HfSiO NCFET ($T_{FE} = 5 \text{ nm}$), based on a MOSFET with S/D extensions with the following parameters $L_{ext} = 2 \text{ nm}$ and $N_{ext} = 2 \cdot 10^{18} \text{ cm}^{-3}$. Values of ΔW are presented in Tab. 3. The other parameters of the base FET remains unchanged.

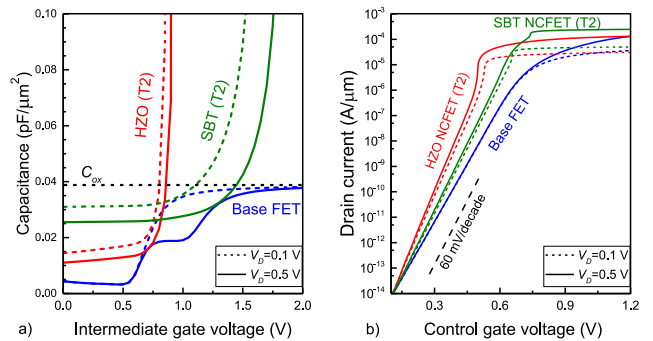


FIGURE 11. Effect of the supply voltage change from 0.1 V to 0.5 V on the capacitance (a) and transfer (b) characteristics of the T2 HZO ($T_{FE} = 73 \text{ nm}$) and the SBT ($T_{FE} = 155 \text{ nm}$) NCFETs with respect to the initial matching. Values of ΔW are presented in Tab. 4. The base structure remains unchanged, relative to Figs. 3-9.

structure bigger — 69.1 mV/dec for 6 decades. As a result, the SS of NCFETs, based on such a structure, also becomes bigger. With an increase of V_D from 0.1 V to 0.5 V, the SS was improved from 66.3 to 65.3 mV/dec, for 6 decades.

For T2-based NCFETs, based on the original base structure with abrupt S/D engineering, the increase of V_D also led to an improvement of the SS shown in Fig. 11. For the

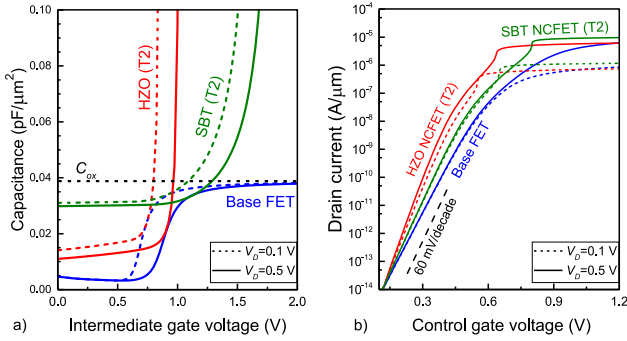


FIGURE 12. Effect of the supply voltage change from 0.1 V to 0.5 V on the capacitance (a) and transfer (b) characteristics of the T2 HZO ($T_{FE} = 73$ nm) and SBT ($T_{FE} = 130$ nm) NCFETs, based on the MOSFET with S/D extensions same to Fig. 10. Values of ΔW are given in Tab. 4.

SBT NCFET, it decreased from 59.1 to 56.9 mV/dec for 7 decades. However, due to the presence of “step”, relation $(1 - C_{MOS}/|C_{FE}|)$ in the weak inversion region increased, as well as due to elongation of the weak inversion region of base structure, steepness of transfer characteristic in this region decreased. As a result, ES improvement became negligibly small: from 57.6 to 57.2 mV/dec for 9 decades. For the HZO-based NCFET, which had V_c in the weak inversion region, the ES has been diminished from 46.7 mV/dec to 42.5 mV/dec for 9 decades.

The NCFETs, based on modified the base structure with the S/D extensions, showed a negligible improvement in the SS for the SBT-based structure from 62.5 to 61.6 mV/dec, while for the HZO-based one, the improvement was more significant: 54.5 vs 49.2 mV/dec, both for 6 decades, shown in Fig. 12. However, unlike the structure with the “step”, improvement of the ES was not achieved.

In general, improvement of the SS for NCFETs with extensions is commensurate with structures that have abrupt S/D engineering. However, in the case of T2-based NCFETs with a “step” shape in the C - V characteristic, an additional improvement in the ES can be achieved, if the V_c is situated in the weak inversion region because near to the “step,” a relatively wide area with $|C_{FE}| \approx |C_{MOS}|$ can exist, which is beneficial for the increase of the steepness of the transfer curve. Tab. 4 shows the impact of the supply voltage increase on the performance of the NCFETs with different S/D engineering.

As seen from the capacitance characteristics, in Figs. 9-12 (a), to avoid the hysteretic operation, the matching should be performed for the minimum intended supply voltage. In such a case, an increase the supply voltage will only decrease the steepness in the weak inversion region and the ES , as a result, while the SS remains the same. This can be seen in Figs. 9-12 (a) by picking the dashed line for C_{FE} ($V_D = 0.1$ V) and the solid line for C_{MOS} ($V_D = 0.5$ V), which increases the $C_{FE} - C_{MOS}$, deteriorating the slope. However, if capacitance matching has been performed for a higher supply voltage, which can be seen by the solid

TABLE 4. Impact of V_D on the Efficiency of the NCFETs.

FE type	Material	Factor		Output parameters of NCFETs			
		S/D engineering	V_D [V]	SS (ES^*) [mV/dec] · #decades	V_T [V]	ΔW [eV]	I_{on} [A/μm] at ($V_{CG} = 1.2$ V)
—	w/o FE	abrupt	0.1	67.5 · 7	0.5	0	3.58 · 10 ⁻⁵
				69.1 · 6	0.5	0	8.52 · 10 ⁻⁷
		extensions	0.5	67.5 · 6	0.5	0	1.30 · 10 ⁻⁴
				69.1 · 6	0.5	0	6.20 · 10 ⁻⁶
1	HfSiO (2)	abrupt	0.1	63.4 · 7	0.468	0.05	4.08 · 10 ⁻⁵
				66.3 · 6	0.477	0.061	9.49 · 10 ⁻⁷
		abrupt	0.5	62.0 · 6	0.461	0.064	1.97 · 10 ⁻⁴
				65.3 · 6	0.475	0.061	7.97 · 10 ⁻⁶
		extensions	0.1	46.7 · 9*	0.406	0.306	3.07 · 10 ⁻⁵
				54.5 · 6	0.411	0.307	7.35 · 10 ⁻⁷
2	HZO	abrupt	0.5	42.5 · 9*	0.386	0.371	1.32 · 10 ⁻⁴
				49.2 · 6	0.388	0.395	6.12 · 10 ⁻⁶
		extensions	0.1	59.1 · 7	0.46	0.130	4.99 · 10 ⁻⁵
				62.5 · 6	0.45	0.130	1.17 · 10 ⁻⁶
		abrupt	0.5	56.9 · 6	0.448	0.156	2.46 · 10 ⁻⁴
				61.6 · 6	0.453	0.135	9.63 · 10 ⁻⁶

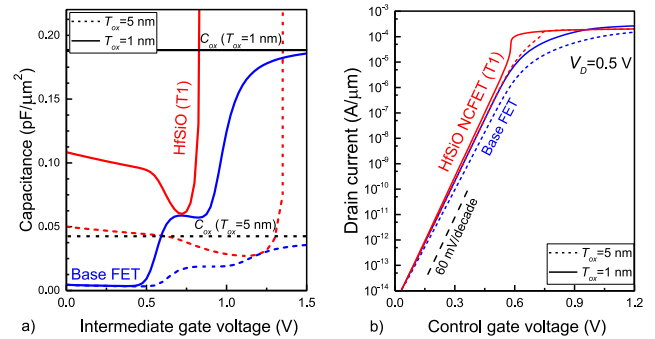


FIGURE 13. Effect of the C_{ox} increase on the capacitance (a) and transfer (b) characteristics of the T1 HfSiO NCFET ($T_{FE} = 3$ nm) with respect to the initial matching. The base structure remains unchanged, relative to Figs. 3-9, 11. Supply voltage $V_D = 0.5$ V. Initial FE thickness $T_{FE} = 6$ nm. Values of ΔW are given in Tab. 5. V_{CG} of structure with $T_{ox} = 5$ nm was decreased by 0.076 V.

line for C_{FE} ($V_D = 0.5$ V) and the dashed line for C_{MOS} ($V_D = 0.1$ V), the area where $|C_{FE}| < C_{MOS}$ can appear results in a hysteretic behavior (see Fig. 2 (a)). Additionally, structures, which have V_c far in the strong inversion region – T3-based MOSFETs, are not affected by this effect, because manipulations of V_D do not lead to a change in the optimal C_{FE} vs V_{IG} curve.

Therefore, as one can notice, depending on the initial position of V_c , further actions to increase the steepness of the transfer characteristic are as follows: if V_c is situated in the beginning of the strong inversion region, a high V_D is required to shift V_c close towards the weak inversion region, as well as to move C_{FE} closer to C_{MOS} ; if V_c is situated in the weak inversion region, a slight increase can be enough; if V_c situated in the depletion region or far in the strong inversion region (T3-based NCFETs), V_D should remain unchanged.

C. BUFFER OXIDE CAPACITANCE C_{ox}

As it was reported in [31], it is difficult for FE connected in series to a semiconductor to achieve a non-hysteretic sub-60 mV/dec operation, making the presence of a buffer

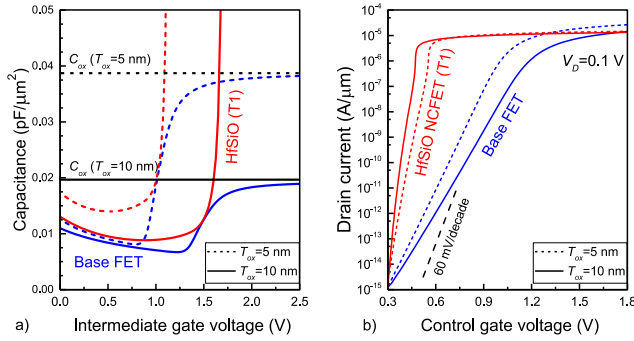


FIGURE 14. Effect of the C_{ox} decrease on the capacitance (a) and transfer (b) characteristics of the T1 HfSiO NCFET ($T_{FE} = 19$ nm) with respect to the initial matching of a modified base structure with $N_A = 1 \cdot 10^{19} \text{ cm}^{-3}$, while the other parameters remains unchanged. Initial FE thickness $T_{FE} = 12$ nm. Values of ΔW are given in Tab. 5. The V_{CC} for the structure with $T_{ox} = 10$ nm was decreased by 0.3 V.

oxide desirable. However, the impact of C_{ox} also differs from the type of FE material used as well as from the position of V_c during the initial matching. An increase of C_{ox} insignificantly shifts V_c towards the depletion region, making possible for T1-based NCFETs to extend the sub- kT/q band. Therefore, if the initial structure with T1-FE has V_c in the depletion/weak inversion region, using a bigger C_{ox} is preferable. Fig. 13 (a) and (b) shows, respectively, the capacitance and transfer characteristics of the HfSiO-based NCFET with $T_{ox} = 5$ nm and $T_{ox} = 1$ nm. To demonstrate the impact of C_{ox} , the supply voltage was changed to 0.5 V. Both factors enabled the decrease of the SS from 62.0 mV/dec (7 decades) and the ES from 70.5 mV/dec (9 decades) to 59.2 and 56.0 mV/dec for 7 and 9 decades, respectively. Because of the shift of V_p towards the opposite direction from the strong inversion region, the on-current is slightly decreased.

However, if the initial structure already has wide a sub- kT/q band, which covers the depletion region, a smaller C_{ox} is preferable because the depletion region relation $|\frac{1}{C_{ox}} - \frac{1}{|C_{FE}}|$ from (11) increases, while C_{SC} changes insignificantly, which leads to an insignificant improvement of the SS . Such an approach can be used both T1- and T2-based NCFETs. Fig. 14 (a) and (b) shows the capacitance and transfer characteristics in the case of capacitance matching for the HfSiO T1-based NCFET with $N_A = 1 \cdot 10^{19} \text{ cm}^{-3}$. An increase of T_{ox} from 5 to 10 nm improved the SS from 30.8 to 22.5 mV/dec for 7 decades and the ES from 28.8 to 19.5 mV/dec for 9 decades.

Matching for the T2 HZO NCFETs with $T_{ox} = 10$ nm led to an ES of 43.7 mV/dec (10 decades) shown in Fig. 15. For the SBT, the ES improved insignificantly from 58 mV/dec to 57 mV/dec for 10 decades, because V_c was still situated in the strong inversion region, and in the depletion region $|C_{FE}|$ was quite close to C_{ox} . The effect of the T_{ox} increase on T3-based NCFETs would be even less perceptible. Tab. 5 shows the summarized impact of C_{ox} on the performance of the investigated NCFETs.

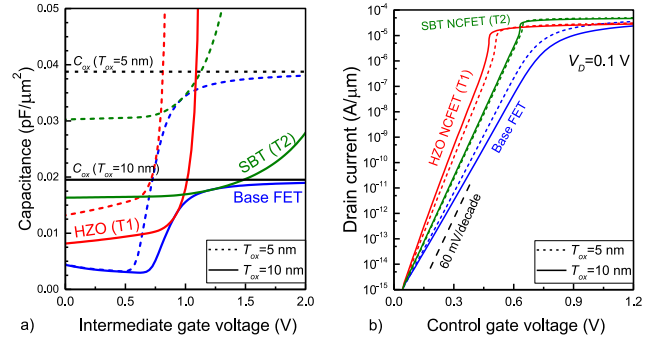


FIGURE 15. Effect of the C_{ox} decrease on the capacitance (a) and transfer (b) characteristics of the T2 HZO ($T_{FE} = 95$ nm) and SBT NCFETs ($T_{FE} = 237$ nm) with respect to the initial matching. Values of ΔW are given in Tab. 5. The V_{CC} for the structure with $T_{ox} = 10$ nm was decreased by 0.093 V. The parameters of the base structure remain the same as in Figs. 3-9, 11.

TABLE 5. Impact of T_{ox} on the Efficiency of the NCFETs.

FE type	Material	Factor			Output parameters of NCFETs			
		T_{ox} [nm]	N_A [cm^{-3}]	V_D [V]	SS (ES^*) [mV/dec] #decades	V_T [V]	ΔW [eV]	I_{on} [A/ μm] at (V_{CC})
—	w/o FE	5	10^{18}	0.5	$67.5 \cdot 6$	0.5	0	$1.30 \cdot 10^{-4}$ (1.2 V)
		1	10^{18}	0.5	$62.3 \cdot 6$	0.4	0	$2.66 \cdot 10^{-4}$ (1.2 V)
		10	10^{19}	0.1	$30.8 \cdot 7$ (28.8 · 9*)	1.25	0.59	$2.08 \cdot 10^{-5}$ (2.5 V)
			10^{18}	0.1	$72.8 \cdot 7$	0.654	0	$2.03 \cdot 10^{-5}$ (1.2 V)
1	HfSiO (2)	5	10^{18}	0.5	$62.0 \cdot 7$ (70.5 · 9*)	0.470	0.074	$1.96 \cdot 10^{-4}$ (1.2 V)
		1	10^{18}	0.5	$59.2 \cdot 7$ (56.0 · 9*)	0.387	0.033	$2.01 \cdot 10^{-4}$ (1.2 V)
		10	10^{19}	0.1	$22.5 \cdot 7$ (19.5 · 9*)	0.817	0.93	$1.42 \cdot 10^{-5}$ (2.5 V)
2	HZO	5	10^{18}	0.1	$47.3 \cdot 10^*$	0.377	0.288	$3.07 \cdot 10^{-5}$ (1.2 V)
		10	10^{18}	0.1	$43.7 \cdot 10^*$	0.466	0.457	$2.76 \cdot 10^{-5}$ (1.2 V)
	SBT	5	10^{18}	0.1	$58.0 \cdot 10^*$	0.44	0.118	$4.99 \cdot 10^{-5}$ (1.2 V)
		10	10^{18}	0.1	$57.0 \cdot 10^*$	0.549	0.219	$4.63 \cdot 10^{-5}$ (1.2 V)

Despite the fact that according to the simulation results, the increase of T_{ox} does not have any limitations in terms of the SS improvement, for real structures, a thick T_{ox} leads to an increase of the SS for the base FET, which results in a smaller gate charge density, and requires a thicker T_{FE} to maintain the same magnitude of voltage drop V_{FE} given by (6). Additionally, a thick T_{ox} leads to the degradation of dynamic characteristics as well as a worse suppression of the short-channel effects. Therefore, a certain optimal value of T_{ox} should exist, which is a trade-off between the improvement of the SS and the drawbacks of using a thick oxide.

D. BURIED OXIDE CAPACITANCE C_{BOX}

The parameters of the initial base SOI MOSFET were chosen as follows: $L_G = 500$ nm, $T_{ox} = 5$ nm, $\epsilon_{ox} = 22$, $T_{body} = 10$ nm, $T_{BOX} = 490$ nm, S/D doping concentrations $N_D = 1 \cdot 10^{20} \text{ cm}^{-3}$, Si channel with p -doping concentration $N_c = 1 \cdot 10^{18} \text{ cm}^{-3}$ and $L_{S/D} = 250$ nm.

An increase of C_{BOX} impacts only the depletion and weak inversion regions of the base structure because in

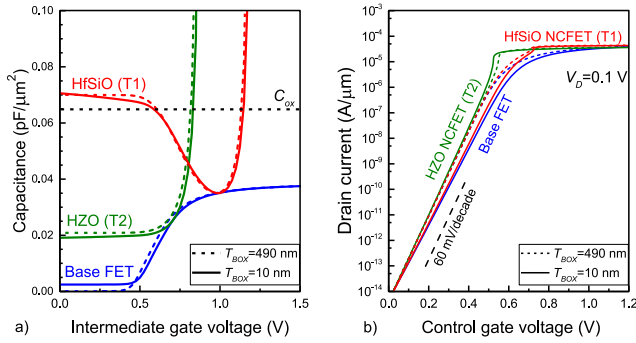


FIGURE 16. Effect of the C_{BOX} increase on the capacitance (a) and transfer (b) characteristics of the T1-based HfSiO ($T_{FE} = 5$ nm) and T2-based ($T_{FE} = 38$ nm) HZO NCFETs with respect to the initial matching (respectively $T_{FE} = 5$ and 33 nm). Values of ΔW are given in Tab. 6. The V_{CC} for the structure with $T_{OX} = 10$ nm was increased by 0.013 V.

the strong inversion region, BOX is shielded from the gate contact by the channel. Therefore, if the initial position of V_c was in the strong inversion region, its position should remain unchanged, and the sub- kT/q band cannot be extended. On the other hand, an increase of C_{BOX} also increases C_{CS} , which is beneficial for the sub- kT/q band, where $|\frac{1}{C_{ox}} - \frac{1}{C_{FE}}| < 0$, making such a factor useful for T2-based structures, while for T1- and T3-based NCFETs, it can lead to a general deterioration of the transfer characteristic steepness because of the considerable increase of the SS beyond the sub- kT/q band, according to (11). Fig. 16 shows the capacitance (a) and transfer (b) characteristics after the matching of T1-based (HfSiO) and T2-based (HZO) NCFETs with different BOX thicknesses. The decrease of T_{BOX} from 490 to 10 nm led to the degradation of SS from 60.4 to 65.0 mV/dec (7 decades) for the HfSiO-based NCFET, while for the HZO-based NCFET, the increase of C_{BOX} helped to improve the SS from 59.7 to 57.8 mV/dec for 7 decades due to the abovementioned effect.

From Fig. 16 (a) it can be noticed that the beginning of the weak inversion region for the structures with the thin BOX became shifted towards higher values of V_G , making possible the decrease of $|C_{FE}|$ in the depletion region, which is beneficial for SS improvement. For T1-based materials it can also lead to the extension of the sub- kT/q band.

Fig. 17 shows the capacitance matching of the modified HfSiO SOI NCFET with $T_{body} = 2$ nm, and $T_{ox} = 1$ nm. With the decrease of the T_{BOX} from 50 to 1 nm, the ES improves from 63.1 to 52.9 mV/dec for 8 decades because the increase of the C_{BOX} led to the extension of the sub- kT/q band over the whole depletion region. Therefore, use of a thin BOX can be beneficial for structures that during initial matching have V_c situated in the weak inversion region.

VI. P-CHANNEL NCFETS

To prove that the effects of the abovementioned factors are valid also for p-channel NCFETs, we performed an additional simulation of the most effective factor, the depletion capacitance, on the performance of a p-channel

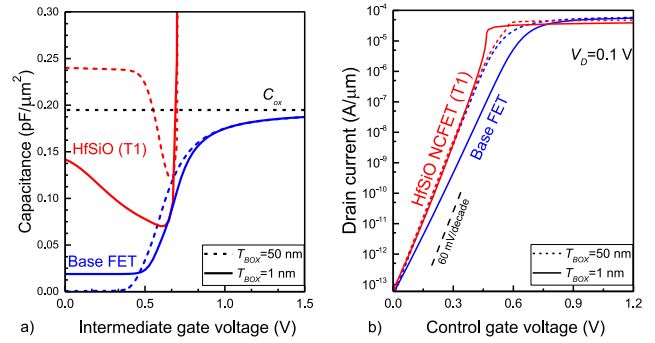


FIGURE 17. Effect of the C_{BOX} increase on the capacitance (a) and transfer (b) characteristics of the T1 HfSiO NCFET ($T_{FE} = 2.4$ nm) with respect to the initial matching. The base structure has $T_{body} = 2$ nm and $T_{ox} = 1$ nm. The other parameters remain unchanged. The initial FE thickness is $T_{FE} = 1.5$ nm. Values of ΔW are given in Tab. 6.

TABLE 6. Impact of T_{BOX} on the Efficiency of the NCFETs.

FE type	Material	Factor			Output parameters of NCFETs			
		T_{BOX} [nm]	Base structure	V_D [V]	SS (ES*) [mV/dec] · #decades	V_T [V]	ΔW [eV]	I_{on} [A/μm] at 1.2 V
—	w/o FE	490	1	0.1	60.4 · 7	0.394	0	4.015 · 10 ⁻⁵
		10			67.8 · 7	0.447	0	3.88 · 10 ⁻⁵
		50	2	0.1	64.3 · 8*	0.348	0	5.92 · 10 ⁻⁵
		1			73.6 · 7*	0.472	0	5.60 · 10 ⁻⁵
1	HfSiO (2)	490	1	0.1	60.4 · 7	0.394	0.022	4.42 · 10 ⁻⁵
		10			65.0 · 7	0.432	0.012	4.32 · 10 ⁻⁵
		50	2	0.1	63.1 · 8*	0.342	0	4.81 · 10 ⁻⁵
		1			52.9 · 8*	0.380	0	3.92 · 10 ⁻⁵
2	HZO	490	1	0.1	59.7 · 7	0.394	0.075	3.76 · 10 ⁻⁵
		10			57.8 · 7	0.389	0.07	3.61 · 10 ⁻⁵

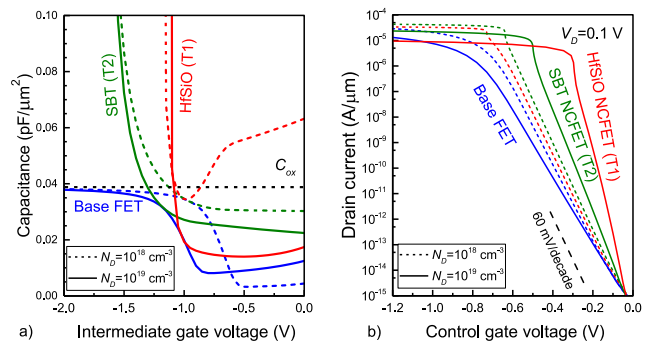


FIGURE 18. Effect of the C_D increase on the capacitance (a) and transfer (b) characteristics of the p-channel T1 HfSiO ($T_{FE} = 12$ nm) and T2 SBT ($T_{FE} = 180$ nm) NCFETs with respect to the initial matching. Values of ΔW are presented in Tab. 7. To improve the visual perception of the results, the V_{CC} for the structure with $N_D = 10^{19}$ cm⁻³ was increased by 0.27 V.

NCFET. Therefore, the doping concentrations of the base structure was changed as follows: $p+$ source/drain doping concentrations $N_{S/D} = 1 \cdot 10^{20}$ cm⁻³ and channel and substrate n doping concentration $N_{ch} = N_D = 1 \cdot 10^{18}$ cm⁻³, while the other parameters remained the same as those of a n-channel structure. HfSiO [16] and SBT [15] were used, respectively, as T1 and T2 materials. Fig. 18 shows the capacitance (a) and transfer (b) characteristics of the investigated structures. As one can see, the impact of the increase

TABLE 7. Impact of N_A on the Efficiency of the p-Channel NCFETs.

FE type	Material	Factor		Output parameters of NCFETs			
		N_A [cm ⁻³]	V_D [V]	SS (E5*) [mV/dec] · #decades	V_T [V]	ΔW [eV]	I_{on} [A/μm] at (V_{CG})
—	w/o FE	10 ¹⁸	0.1	67.5 · 6	-0.52	0	2.91 · 10 ⁻⁵ (-1.2 V)
		10 ¹⁹	0.1	76.7 · 6	-0.84	0	1.38 · 10 ⁻⁵ (-1.5 V)
1	HfSiO [16]	10 ¹⁸	0.1	63.4 · 6	-0.485	0.05	3.39 · 10 ⁻⁵ (-1.2 V)
		10 ¹⁹	0.1	30.0 · 6 (29.2 · 8*)	-0.51	0.56	9.57 · 10 ⁻⁶ (-1.5 V)
2	SBT	10 ¹⁸	0.1	59.3 · 6	-0.455	0.111	4.31 · 10 ⁻⁵ (-1.2 V)
		10 ¹⁹	0.1	50.1 · 6 (47.3 · 9*)	-0.65	0.6	2.37 · 10 ⁻⁵ (-1.5 V)

of the channel doping concentration is absolutely the same as that of the n-channel NCFET previously investigated, and the results are summarized in Tab. 7. Additionally, even the extracted values, shown in Tab. 7, are very similar to those of Tab. 3. Similarly, we can claim that the effect of the other parameters on the SS of NCFETs is same for both n- and p-channel structures.

VII. CONCLUSION

In this study, we, for the first time, systematically investigated approaches to obtain the sub- kT/q hysteresis-free operation mode of NCFETs based on arbitrary MOSFETs and FE materials for a wide range of applied voltages using a capacitance matching simulation. Depending on the position of the critical voltage V_c during the initial matching, further actions to improve the SS are as follows. If V_c is situated in the strong/weak inversion region, and needs to be shifted closer to the depletion region (to extend the sub- kT/q band), it can mainly be done by increasing the depletion capacitance C_D . An insignificant shift can be achieved by increasing the oxide capacitance C_{ox} . For SOI structures with V_c situated in the weak inversion region, it can be also obtained by an increase of the BOX capacitance C_{BOX} . In contrast, when V_c is situated in the depletion region and the NC band of the FE capacitance C_{FE} is narrow, it can be expanded by decrease of C_D , as well as by decreasing C_{ox} . In the case when V_c is situated in the depletion/weak inversion region and its position is satisfactory, further improvement of the SS can be done by decreasing C_{ox} and increasing C_{BOX} as well as by increasing the supply voltage. However, the impact of each factor is not straightforward, and they have their own saturation. Therefore, the optimal combination of factors, corresponding to the best possible SS , can be verified only by the capacitance characteristics achieved during extra simulations.

Additionally, if the NC region of the FE capacitance does not cover the whole depletion and weak inversion regions, the on-current will be smaller compared to that of the base FET. Therefore, for certain structures there could be a trade-off between the improvement of the SS and the increase of the on-current.

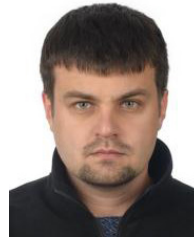
In general, a better SS can be more easily obtained for T2-based NCFETs due to a wide sub- kT/q band. Even if V_c

is situated far from the depletion region (T3-based NCFETs), $SS \approx 60$ mV/decade can be achieved for a wide band of gate voltages, while for T1-based NCFETs, the desired operation mode sometimes can be obtained only for a very short band of gate voltages, leading to an average $SS > 60$ mV/decade.

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