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A Compact Pixel Circuit for Externally Compensated AMOLED Displays

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ABSTRACT Nonuniformity and aging are two major issues with the pixel circuits of active-matrix organic light-emitting diode displays. External compensation scheme is typically employed to mitigate these two issues, since various off-panel resources, such as on-chip processors and memory arrays, can be utilized. A new pixel circuit with feedback path for the external compensation scheme is proposed in this paper. The data line and monitor line are shared for two adjacent columns of pixel circuits to increase the aperture opening ratio of display panel. The number of thin-film transistors attached to each data line is reduced by 50% with the proposed pixel circuit compared to the traditional pixel circuit. The average power consumption of the normal display operation is thereby reduced by 15%.

INDEX TERMS AMOLED, thin-film transistor (TFT), external compensation, shared data and monitor line.

I. INTRODUCTION

Active-Matrix Organic Light-Emitting Diode (AMOLED) is the next generation display technology due to the superiority in contrast ratio, response time, viewing angle, and range of working temperature compared with the currently prevailing Active-Matrix Liquid Crystal Display (AMLCD) technology. Thin film transistors (TFTs) are used to construct a programmable current source to drive Organic Light-Emitting Diode (OLED) to emit light. The threshold voltage of TFTs however shifts under voltage stress at the gate terminal. The mobility of the carriers inside TFTs also changes with temperature. The electrical characteristics of AMOLED therefore vary significantly with the variability of TFTs. A compensation scheme is essential to alleviate the impact caused by the variations of TFTs.

The existing compensation schemes are categorized as internal compensation and external compensation. The internal compensation schemes only utilize limited number (usually lower than 10) of TFTs [9]–[15]. The compensation effect is therefore also limited. Alternatively, the external compensation scheme transfers the electrical condition of every pixel circuit off the panel. On-chip processors and memory circuits are used to implement compensation algorithms to eliminate the display variations that are caused by the TFTs [1]–[6]. The internal compensation scheme can compensate well the threshold voltage shift of both driving TFT and OLED, but is difficult to precisely compensate the mobility variation of the driving TFT as well as the luminance degradation of OLED. Currently, the compensation of the mobility variation of a pixel circuit locally is done by charging or discharging the storage capacitor for a fixed amount of time. However, this fixed amount of time is impossible to achieve for all pixel circuits all over the display panel due to the effect of scan line parasitic resistance and capacitance. Alternatively, in the external compensation scheme, the coordinate of the pixel circuit can be a parameter input of the compensation algorithm. In the internal compensation scheme, the luminance degradation compensation can only be carried out by measuring the absolute anode voltage of the OLED as a parameter. Alternatively, for the external compensation, not only the absolute anode voltage of OLED can be measured, the change of the anode voltage of the OLED over a period can also be measured and used as a parameter for more precise compensation of luminance degradation of the OLED.

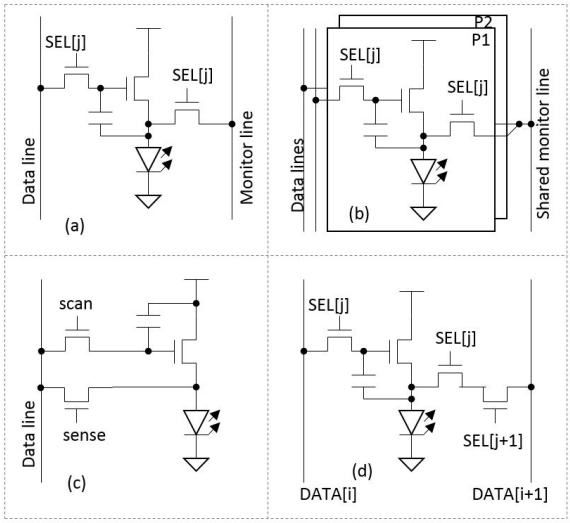

FIGURE 1. State-of-the-art pixel circuits for AMOLED displays with external compensation schemes. (a) A pixel circuit with separate data line and monitor line [1], [2]. (b) A pixel circuit with shared monitor lines [3]. (c) A pixel circuit with shared data and monitor lines [4]. (d) A pixel circuit with shared data and monitor lines. The scan signal is reused for feedback path control [5], [6].

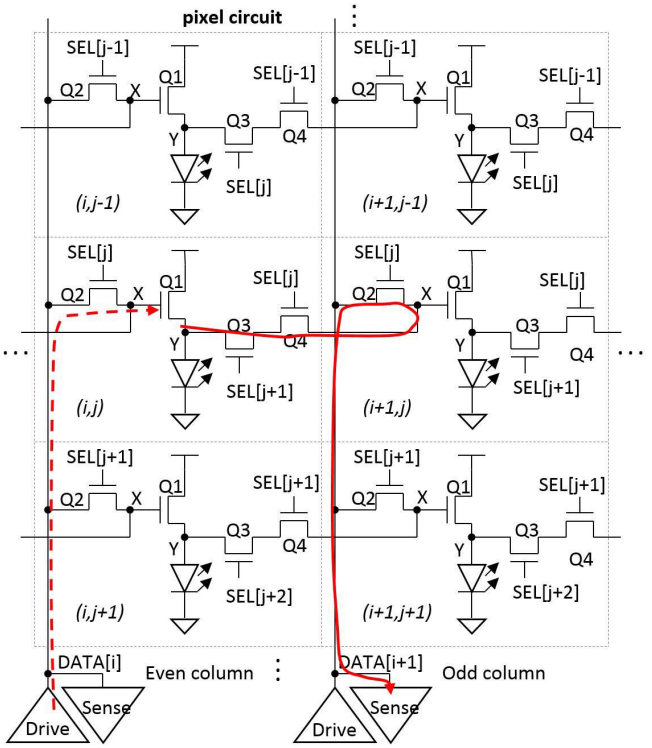

FIGURE 2. A partial array of the proposed pixel circuits for the AMOLED display panel with the data line driver and sense block of each data line.

A pixel circuit equipped with a feedback path is essential for the external compensation scheme of AMOLED displays. The feedback aging information can be in either voltage or current. If the feedback aging information is current, then the sensing block needs to keep the monitor line at a voltage level lower than the threshold voltage of the OLED device in order to keep the OLED off and sink all the current from the driving TFT to the sensing block [8]. During the display period, the display drivers keep charging and discharging the data lines on the display panel. The traditional pixel circuit with dedicated data line and monitor line is shown in Fig. 1a [1], [2]. The capacitive loading on the data line is the lowest with the pixel circuit in Fig. 1a among the existing pixel circuits for AMOLED displays with external compensation schemes since only one TFT of each pixel circuit is attached to the data line. The total number of data and monitor lines is however the largest among the existing pixel circuits. To reduce the number of data and monitor lines for a higher aperture opening ratio, each monitor line is shared by every two columns of pixel circuits in [3] while the data lines are not shared (Fig. 1b). In [4], each data line and monitor line are shared to further reduce the amount of global interconnections (Fig. 1c). Extra scan line is however still required to control the feedback path in [4]. In [5] and [6], the existing scan signal is used as the control signal of the feedback path (Fig. 1d) to further reduce the number of data lines, monitor lines, and scan lines. However, the number of TFTs attached to the shared data and monitor lines is doubled in this scheme, thereby increasing the capacitive loading and seriously impacting the power consumption as well as speed of the display panel.

In this paper, a low power compact pixel circuit is proposed to reduce the number of data, monitor, and scan lines while keeping the capacitive loading on the shared data and monitor lines to the minimum. The number of TFTs attached to each data line is reduced by 50% with the proposed pixel circuit compared to the traditional pixel circuit. The average power consumption of the normal display operation is thereby reduced by 15%.

The paper is organized as follows. The newly proposed pixel circuit is introduced in Section II. Simulation results of the proposed pixel circuit and comparison with the traditional pixel circuits are presented in Section III. The paper is summarized in Section IV.

II. THE PROPOSED PIXEL CIRCUIT

The proposed low power compact pixel circuit is introduced in this section. Qualitative comparison between the proposed pixel circuit and the previously published pixel circuits is also presented.

A. THE PROPOSED PIXEL CIRCUIT

Assuming that the array size of pixel circuits is M×N, M and N are the number of columns and rows, respectively. A partial array (2×3) of the proposed pixel circuits for the AMOLED display panel is shown in Fig. 2. The data line driver and the aging information sensing block for each data line are shown in the figure as well. The data line driver and the sensing block are attached to the data line during the

TABLE 1. Comparison of different pixel circuits.

	Without sharing [1][2]	Shared monitor lines [3]	Shared data and monitor lines [4]	Shared data and monitor lines [5][6]	The proposed design
Monitor and data line #	2×M	1.5×M	M	M+1	M+1
Scan line #	N	N	2×N	N+1	N+1
Data line diff. cap. #	N	N	2×N	2×N	N
Monitor line diff. cap. #	N	2×N	2×N	2×N	N
Re-program line #	1	1	1	2	2
Feedback path TFT #	1	1	1	2	3

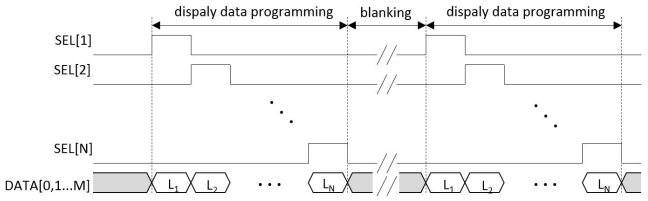

FIGURE 3. The waveform of the display operation with the proposed pixel circuit.

display and feedback operations, respectively. The proposed pixel circuit is embedded in each dotted box in Fig. 2. Q1 is the driving TFT which provides programmable current for the OLED to emit light. Q2 is the switch TFT which is used to select the pixel circuit for display data or calibration data programming. Q3 and Q4 are two TFT switches for constructing the feedback path. To construct a feedback path, Q2 from the adjacent pixel circuit on the right side (see Fig. 2) needs to be turned on as well. To construct the data programming path of the Pixel(i, j), only SEL[j] needs to be asserted. Alternatively, to construct the feedback path, both SEL[j] and SEL[j+1] need to be asserted. In Fig. 2, the dashed line with an arrow shows the data programming path of Pixel(i, j). The solid line with an arrow shows the feedback path of the Pixel(i, j).

The characteristics of different pixel circuits are summarized in Table 1. The pixel circuit in [1] and [2] (see Fig. 1a) has dedicated data lines and monitor lines as well as separated scan lines for pixel circuit selection and feedback path control. Therefore, for M×N array of pixel circuits, the number of TFTs attached to each data line and monitor line is N. The total number of data and monitor lines is 2×M, while the total number of scan lines is N. The feedback path starts from the output of the current source (the source terminal of the driving TFT) and ends at the sensing block. There is only one switch TFT between the output of current source and the monitor line. The number of TFTs on the feedback path is therefore one. At the beginning of the feedback operation, the calibration data need to be programed into the pixel circuits, thereby corrupting the original display data. It is therefore necessary to write back the corrupted display data after completing the feedback operation. The data line and monitor line share the same scan signal. Only one line of display data are corrupted, therefore need to be re-programed after the feedback operation. The pixel circuit in [3] (see Fig. 1b) shares the monitor lines. The total number of monitor and data lines is reduced to 1.5×M. However, the total number of diffusion capacitors attached to each shared monitor line are increased to 2×N. Only one line is corrupted after sending back the aging information of a line of pixel circuit. The pixel circuits in [4] (see Fig. 1c) re-use the data line as the monitor line but apply different control signals, which reduce the total number of monitor and data lines to be M. However, separated signals for display data programming and feedback path control double the number of scan lines to 2×N. Furthermore, the number of capacitors attached to the data line and monitor line is 2×N. The number of TFT between the output of the current source and the monitor line is one. Only one line of display data needs to be re-programed after the feedback operation. The pixel circuit in [5] and [6] (see Fig. 1d) shares the data line of the adjacent/next column as the monitor line. This approach reduces the total number of data and monitor lines to M+1. The number of TFTs attached to each data/monitor line is however increased to 2×N. The pixel circuit in [5] and [6] also re-uses the existing scan lines for controlling the feedback path, thereby reducing the number of scan lines to N+1. The feedback path is controlled by two switching TFTs and their control signals from SEL[j] and SEL[j+1]. There are therefore two TFTs between the output of the current source and the monitor lines. Two lines of display data are corrupted during the feedback operation, and require to be written back after the feedback operation. The proposed pixel circuit combines the advantages of the pixel circuits in [1], [2], [5], and [6]. The total number of data and monitor lines of the proposed pixel circuit is M+1, while the total number of scan lines is N+1, thereby achieving the same aperture opening ratio as the pixel circuit in [5] and [6]. The number of TFTs attached to each data/monitor line is N in the proposed pixel circuit, thereby obtaining similar capacitive loading on the data/monitor lines to the pixel circuit in [1] and [2].

B. THE DISPLAY OPERATION

During the display operation of Row j, the gate driver asserts the scan signal SEL[j] and turns on all Q2's of Row j. The data line drivers release the display data of Row j (L_j) on the data lines DATA[0, 1, ... M] simultaneously. The display data of each data line can be subsequently programmed into the corresponding pixel circuit and stored on the node X. Although all Q3's of Row j-1 are turned on by SEL[j], the previously stored display data are not corrupted since all Q4's of Row j-1 are off.

The waveform of the display operation with the proposed pixel circuit is illustrated in Fig. 3, which is the same as the display driver IC with the traditional pixel circuits [7]. During the display data programming period, the gate driver generates the scan signals (SEL[1], SEL[2], ... SEL[N]) to turn on the pixel circuits row by row. The data line drivers release the corresponding display data (L_x) of the row on

all data lines (DATA[0, 1, . . . M]) simultaneously. After programming the last row of the pixel circuits, there is an inter-frame blanking period.

C. THE FEEDBACK OPERATION

The feedback operation typically occurs during the non-displaying period, thereby posing no influence on the normal display operation. The non-display period can be the inter-frame blanking period, the period before turning on the panel, and the period after turning off the panel.

The aging information of the proposed pixel circuits in the even and odd columns is fed back to the sensing block alternatively. The proposed pixel circuit turns an existing switch TFT to be used on the feedback path, which increases the resistive loading, compared to the traditional pixel circuits [5], [6]. Since the feedback operation occurs during the non-display period, the increased resistive loading does not affect the circuit performance.

The waveform of the feedback operation of the pixel circuits in Row j is illustrated in Fig. 4. The feedback operation is divided into three steps. The aging information of the pixel circuits in the even column and the odd column is fed back to the sensing block in the display driver IC in the first and second steps, respectively. In the third step, the display data of Rows j and j+1 are re-programmed. In the first step, the gate driver asserts both SEL[j] and SEL[j+1] to turn on all the Q2's, Q3's and Q4's in the pixel circuits of Row j. The data line drivers in the even columns drive the even column data lines DATA[0, 2, . . .] with the calibration data (C_{j_even}) of the pixel circuits in the even columns. The aging information (F_{j_even}) of the pixel circuits in the even columns are fed back to the sensing blocks in the odd columns through the odd column data line DATA[1, 3, . . .]. One option of the aging information is the current used for driving TFT Q1. To sink the current for driving TFT Q1 to the sensing block, the voltage of the feedback path needs to be held below the threshold voltage of the OLED [8]. The second step operates in the same way as the first step while the roles of the even and odd data lines are exchanged.

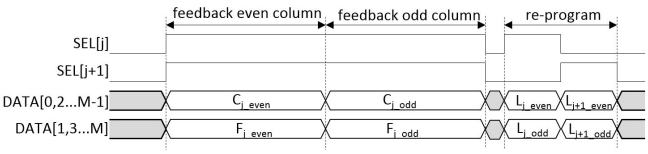

FIGURE 4. The waveform of the feedback operation with the proposed pixel circuit.

External compensation scheme requires to program the calibration data into the pixel circuit, thereby corrupting the originally stored display data. It is therefore necessary to re-program back the original display data after feedback operation. If the feedback operation carries out before turning on or after turning off the panel, there is no impact on the normal display operation. Alternatively, if the feedback operation carries out during the inter-frame blanking period, the panel displays abnormally during the period of the feedback operation. However, the inter-frame blanking period is very short and invisible to human eyes. The abnormal display caused by the feedback operation is therefore negligible.

III. SIMULATION RESULTS

In this paper, we focus on analyzing the power consumption on the data line during the display operation. Two 2×3 pixel arrays illustrated in Fig. 2 are constructed with the proposed and the traditional pixel circuits [5], [6], respectively. The loading of 3 kΩ resistor and 100 pF capacitor is added to the data line, which mimics the loading of a data line of an FHD (1920×1080) AMOLED panel. 1077 and 2154 dummy TFTs are attached to each data line of the 2×3 array with the proposed and the traditional pixel circuits, respectively, to mimic the capacitive loading of the other 1917 pixel circuits attached to the data line. The size (W/L) of the driving TFT and all switching TFTs of both designs is 10 μm / 3.5 μm and 7 μm / 3.5 μm, respectively. SPICE simulation is performed for both circuits with IGZO TFT model and with diode-connected TFT to mimic an OLED device. The SPICE model in [16] is used for the IGZO TFT. The key model parameters are listed in Table 2. The power supply voltage is 20 V.

TABLE 2. Key SPICE model parameters used for the simulation.

Parameter	Unit	Value	Physical Explanation
TOX	m	2.00E-07	Thin-oxide thickness
VTO	V	1.21	Zero-bias threshold voltage
KVT	V/°C	-0.0005	Threshold voltage temperature coefficient
GAMMA	-	0.135	Power law mobility parameter
MUBAND	m^2/Vs	2.34E-03	Conduction band mobility
VAA	V	2 000	Characteristic voltage for field effect mobility
EMU	eV	0.06	Field effect mobility activation energy
CGDO	F/m	2.65E-09	Gate-drain overlap capacitance per meter channel width
CGSO	F/m	2.65E-09	Gate-source overlap capacitance per meter channel width

The display power consumed by the proposed and the traditional designs [5], [6] is compared by charging the gate of the driving TFT from gray level 0 to 128, the corresponding gate voltage of which is 3.878 V to 10.18 V. The simulation results are illustrated in Fig. 5. The display power is calculated by taking average of the integration of the product of the output voltage and current of the data line driver from 140 μs to 155 μs, as shown in Fig. 5. Due to coupling effect, the voltage programmed onto the gate of the pixel circuits is reduced slightly when the scan signal switches from high voltage level to low voltage level. In order to program the target data voltage onto the gate of the pixel circuits, a voltage higher than the target data voltage, such as 10.66 V and 10.39 V, has been outputted by the data line driver for the proposed and the traditional pixel circuit, respectively.

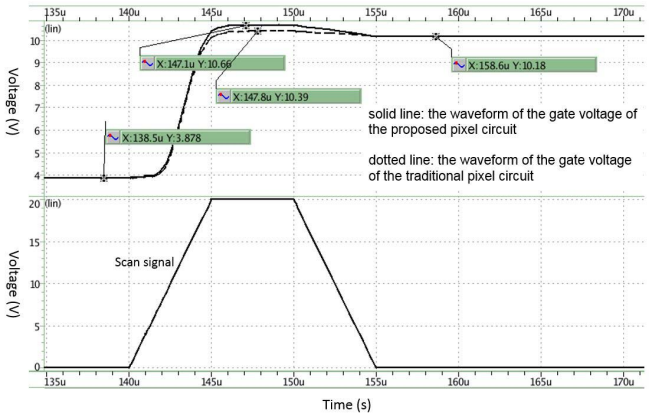

FIGURE 5. The waveform of the scan signal and the gate voltages of the proposed and the traditional pixel circuits during the display operation.

The proposed pixel circuit requires a slightly higher data line voltage because the new pixel circuit has an extra gate-source capacitor of the switching TFT between the scan line and the gate of the driving TFT.

Based on the SPICE simulation, the display power to charge the data line is reduced by 15% with the proposed design compared to the traditional design in [5] and [6]. Although the number of transistors attached to the data line is reduced by the proposed design compared to the traditional design, the number of switching TFTs connected to the gate of the driving TFT of a pixel circuit increases from one to two in the proposed design, which induces higher charge injection and coupling effect during switching off the scan line. The power savings with the proposed design is therefore lower than expectation.

IV. CONCLUSION

A new low power and compact pixel circuit with feedback path for external compensation of AMOLED displays is proposed in this paper. With shared data and monitor lines, the proposed pixel circuit increases the aperture opening ratio of display panel and reduces the number of TFTs attached to each data line by 50% with the proposed pixel circuit compared to the traditional pixel circuit, thereby reducing the average power consumption of the normal display operation by 15%.

In the proposed pixel circuit, the feedback path may have an intersection with data line in the layout. Careful layout is needed to minimize this effect. However, the overlap area of this intersection is not supposed to be large. The capacitor induced by this kind of intersection is interlayer capacitor, which is significantly smaller than intra-layer capacitors. Therefore, the coupling effect caused by this kind of intersection would not be significant. Furthermore, metallic nanowire [17] has a great potential to replace ITO (Indium Tin Oxide) as the interconnect on the display panel. Metallic nanowire has much lower resistance than ITO and can make the data line narrower to reduce the intersection capacitance.

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