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Normally-OFF GaN MIS-HEMT With F^- Doped Gate Insulator Using Standard Ion Implantation

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ABSTRACT A normally-OFF GaN metal-insulator-gate high electron mobility transistors with fluorine doped gate insulator has been fabricated using standard ion implantation technique. Fluorine ions with negative charges were doped lightly into both the gate insulator and the partially recessed barrier layer, resulting in high positive threshold voltage (V_{th}) for the device, meanwhile preserving low ON-resistance. Compared to the fluorine-free and recess-free device, only about 16% increase of ON-resistance was observed for the F^- doped devices. The fabricated F^- doped device exhibits a threshold voltage of +0.68 V at $I_{DS} = 5\ \mu$A/mm, a current density of 620 mA/mm, an OFF-state breakdown voltage of 800 V, and high ON/OFF current ratio of 10^{10}. For thermal stability consideration of fluorine dopant, the V_{th}-thermal stability test and positive bias temperature instability test were also discussed.

INDEX TERMS AlGaN/GaN, MIS-HEMT, enhancement-mode, normally-OFF, Al_2O_3, fluorine ion implantation.

I. INTRODUCTION

GaN based high electron mobility transistors (HEMTs) have demonstrated superior performance for high power applications. However, due to safety-consideration, normally-OFF operation is preferred when the device is used as power switching devices for electrical vehicles. Several approaches have been demonstrated to achieve normally-OFF HEMTs in the past, such as recessed-gate [1], p-type GaN [2], and fluorine implantation [3]. To effectively suppress ON-state gate leakage current and increase gate swing, normally-OFF devices have been fabricated by combining recessed-gate and MIS (metal-insulator-gate) approaches [4], [5]. However, a fully recessed barrier degrades the channel mobility and increases the channel resistance, leading to large ON-resistance and low current density [6], [7]. Partial-gate-recess, which maintains a thin barrier layer, could preserve high channel mobility, but the threshold voltage is not positive enough to achieve normally-OFF operation. Therefore, new approaches are needed. In order to increase the threshold voltage with small current degradation, the partially recessed fluorine-implanted barrier layer using CF_4 plasma etch has demonstrated the E-mode GaN MIS-HEMTs with low ON-resistance with high output current density [8]. However, the CF_4 plasma etch could cause high fluorine concentration in the remaining barrier layer, resulting in trap generation and channel mobility drop [9]. To prevent the high fluorine concentration in the barrier layer, GaN HEMT using multilayer fluorinated gate oxide stack has been demonstrated with high threshold voltage of + 6.5 V [10]. It indicates that fluorine implantation with the negative charge incorporation into the gate oxide stack could effectively make a positive shift of the threshold voltage without much current degradation.

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Many groups have reported the results of fluorine implantation using the RIE, ECR systems [3], [8]–[10]. However, the process conditions of these systems could vary from equipment to equipment [11] and the fluorine concentration in the film was not well controlled. In contrast, ion implanter which has been widely used in CMOS process, and has been proved to be the better choice to control the fluorine doping profile in the film. Several groups have demonstrated the results of E-mode GaN HEMT with ion implantation technology, however, a large current degradation and large ON-resistance were observed [11], [12].

In this letter, we report a fabrication process of normally-OFF GaN MIS-HEMT with fluorine doped gate insulator using the standard fluorine ion implantation. The fluorine ions were doped into both the gate insulator and the partially recessed barrier layer to achieve normally-OFF device with positive V_{th}, but without large ON-resistance increase. The fabricated F^- doped devices exhibit a positive V_{th}, high drain current density, low ON-resistance, high breakdown voltage and small V_{th} hysteresis. The switching behaviors, temperature stability and PBTI characteristics of the device are also investigated in this study.

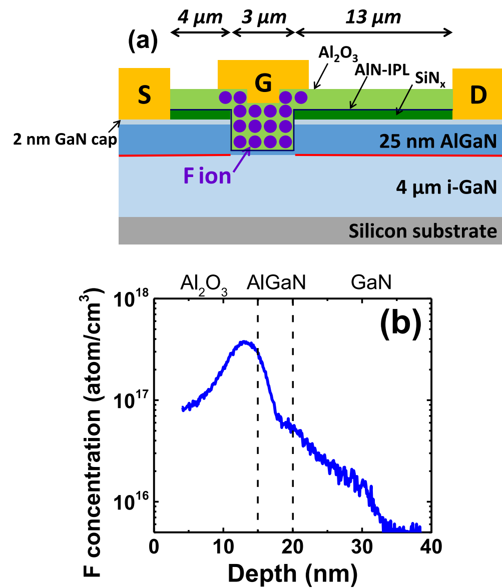

FIGURE 1. (a) The schematic cross section of the F^- doped GaN MIS-HEMTs. (b)Fluorine profiles measured by Secondary-Ion-Mass-Spectrometry (SIMS) in F^- doped-Al_2O_3/AlGaN/GaN structure.

II. DEVICE FABRICATION

The AlGaN/GaN HEMT structure was grown on (111) silicon substrate by metal-organic chemical vapor deposition (MOCVD). The epitaxial structure consisted of a 2-nm GaN cap layer, a 25-nm $Al_{0.23}Ga_{0.77}N$ barrier layer, and a 4.3 µm buffer layer. The electron mobility and sheet resistance were 1500 cm^2/V and 380 ohm/sq, respectively. The device fabrication started with ohmic contact formation of alloyed Ti/Al/Ni/Au metal stack. The planar isolation was performed using nitrogen ion implantation. For device passivation, in-situ nitrogen plasma treatment was performed using plasma-enhanced chemical vapor deposition (PECVD) machine, followed by the deposition of 15-nm SiNx layer as the passivation layer [13]. Nitride etch and gate recess were performed by low power inductively coupled plasma (ICP) system, the remaining barrier thickness was about 5 nm. The gate recess process was performed using Cl_2 gas with the following parameters: flow rate: 40 sccm, chamber pressure: 0.1 Pa, RF power: 200 W of with 5 W of bottom bias. The bottom electrode voltage was about 30 V. For the etch depth control, we use the open-gate structures to monitor current change during the gate recess process [14]. This current change with etching time is strongly related to remaining barrier thickness, which can precisely control the etch depth. In this work, two samples were etched at the same time and the currents after etching were approximately the same. 15 nm AlN/Al_2O_3 was deposited by plasma-enhanced atomic layer deposition (PEALD) system as gate dielectric, where the AlN was deposited as interfacial passivation layer (IPL) to reduce the interface traps at the Al_2O_3/GaN interface [15]. A post–deposition annealing (PDA) at 400 °C was performed in N_2 ambient. After gate window was opened, fluorine ions were directly implanted into the gate region by Varian E500HP ion implanter. The implantation energy and ion dose were 10 keV and 1×10^{12} cm^{-2}, respectively. Ni/Au was deposited by electron beam evaporation as the gate metal, subsequently. Finally, post–metallization annealing (PMA) was carried out at 400 °C for 10 minutes in N_2 ambient to remove the implantation damages and activate the fluorine ions.

III. RESULTS AND DISCUSSION

The schematic cross section of the normally-OFF device is as shown in Fig. 1 (a). The fabricated devices feature a gate length of 3 µm, a gate-drain spacing of 13 µm, gate-source spacing and gate width were 4 µm and 25 µm, respectively. The fluorine distribution in the F^- doped Al_2O_3 /AlGaN/GaN structure was confirmed by SIMS measurement, as shown in Fig. 1 (b). The peak fluorine ion concentration was $\sim 2 \times 10^{17}$ atom/cm^3 and the peak ion concentration located nearly at the Al_2O_3/AlGaN interface, indicating that most fluorine ions were blocked at the gate insulatorand AlGaN layer and only a few fluorine ions were incorporated into the GaN channel layer. The fluorine ion concentration in the GaN channel layer was $\sim 3 \times 10^{16}$. It suggests that 2DEG electrons in the channel might still possess high mobility but with little mobility degradation. Fig. 2(a) and Fig. 2(b) show the I_{DS}-V_{GS} transfer characteristics of the F^- doped devices with various V_{DS} and with constant V_{DS} = 10 V, respectively. The F^- doped device showed a V_{th} of +0.68 V, as determined by drain current criterion (I_{DS} = 5 µA/mm at V_{DS} = 10 V), and the maximum transconductance was 100 mS/mm. The steep subthreshold slope (SS) of 82 mV/decade and the small V_{th} hysteresis (160 mV) were obtained at the up and down

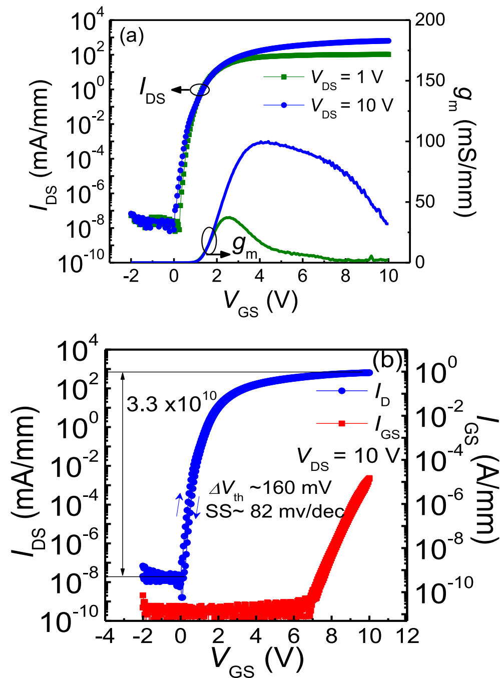

FIGURE 2. Transfer characteristics of the F^- doped devices with various V_{DS} (a) and with constant $V_{DS} = 10$ V (b).

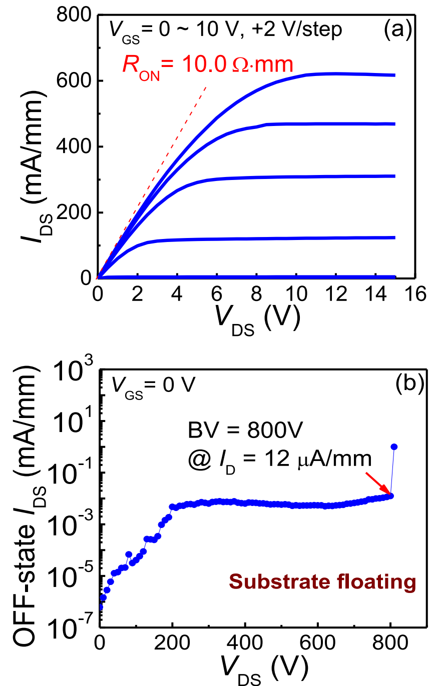

FIGURE 3. (a) I_{DS}–V_{DS} characteristics and (b) OFF-state drain current for the F^- doped normally-OFF GaN MIS-HEMTs.

sweeps between −2 V to +10 V, suggesting a good fluorinated dielectric/AlGaN interface. The off-state drain current (I_{OFF}) was $\sim 10^{-8}$ mA/mm, leading to the high I_{ON}/I_{OFF} current ratio of 3.3×10^{10}. Besides, a very low forward gate leakage of $\sim 10^{-11}$ A/mm was observed, indicating the quality of gate insulator was preserved after fluorine ion implantation and annealing process. The maximum current density was 620 mA/mm as shown in Fig. 3(a) The ON-resistance (R_{ON}) of F^- doped device was 10 Ω·mm. Compared with the fluorine free and recess free device with R_{ON} of 8.6 Ω·mm, only 16% increase of R_{ON} was observed for the F^- doped devices. This slight R_{ON} increase is comparable to the reported results in [5]–[7] and [11]. Thus, the F^- doped devices with high drain current and low R_{ON} indicates that the 5 nm remained AlGaN barrier maintained high electron mobility in the channel and suppressed the channel resistance increase. The OFF-state drain current characteristics of the F^- doped device is shown in Fig. 3(b). The devices exhibit breakdown voltage of 800 V with drain current of 12 μA/mm when $V_{GS} = 0$ V. It also shows that the device with F^- doped oxide exhibited a well pinched off behavior at $V_{GS} = 0$ V.

Fig. 4 (a) compares the I_{DS}-V_{GS} of the recessed-gate device with and without F^- doping. The recess-only device was fabricated with the same process flow but without fluorine ion implantation. The fluorine process resulted in the V_{th} shift of 1.5 V (V_{th} @ $I_{DS} = 5$ μA/mm). This demonstrates that the doped fluorine ions effectively shift the V_{th} to achieve normally-OFF operation. The positive V_{th} shift was due to the implanted fluorine ions at the gate insulator and barrier layer, which provides higher positive potential to increase the V_{th} [10], [16]. However, even F^- doped device could make a large positive shift of V_{th}, several reports indicated that implantation-induced mobility degradation, leading to low current density due to trap generation in the films [9], [11]. Fig. 4 (b) compared the I_{DS}-V_{DS} characteristics of the recessed gate device with and without fluorine implantation at 9 V gate over drive ($V_{GT} = V_{GS} - V_{th} = 9$ V, V_{th} was extracted at $I_{DS} = 5$ μA/mm with $V_{DS} = 10$ V). Only 8 % reduction on maximum drain current density was observed for the F^- doped device compared to the recess-only device. It indicates that 2DEG electrons in the channel still has high mobility with very little mobility degradation. This is attributed to the low fluorine concentration in the GaN channel layer.

Fig. 4 (c) shows the I_{GS}-V_{GS} characteristics of both devices with $V_{DS} = 0$ V. The gate breakdown for recess-only device and for F^- doped device was 11.1 V and 11 V, respectively. The similar gate leakage current characteristics of both devices indicate the quality of the gate insulator was preserved after fluorine ion implantation.

Fig. 4 (d) shows the temperature-dependent V_{th} characteristics of both devices from 30 °C to 200 °C. The V_{th} changing rates for both devices from 30 °C to 200 °C were near the same. The V_{th} shift of F^- doped device at 200 °C was ∼0.6 V. It is much lower than the reported fluorinated oxide results [17], which suggests the F^- doped technology in this work has low bulk oxide trap generation with improved V_{th} temperature stability. Besides, after high temperature measurement, the V_{th} of the devices returned to

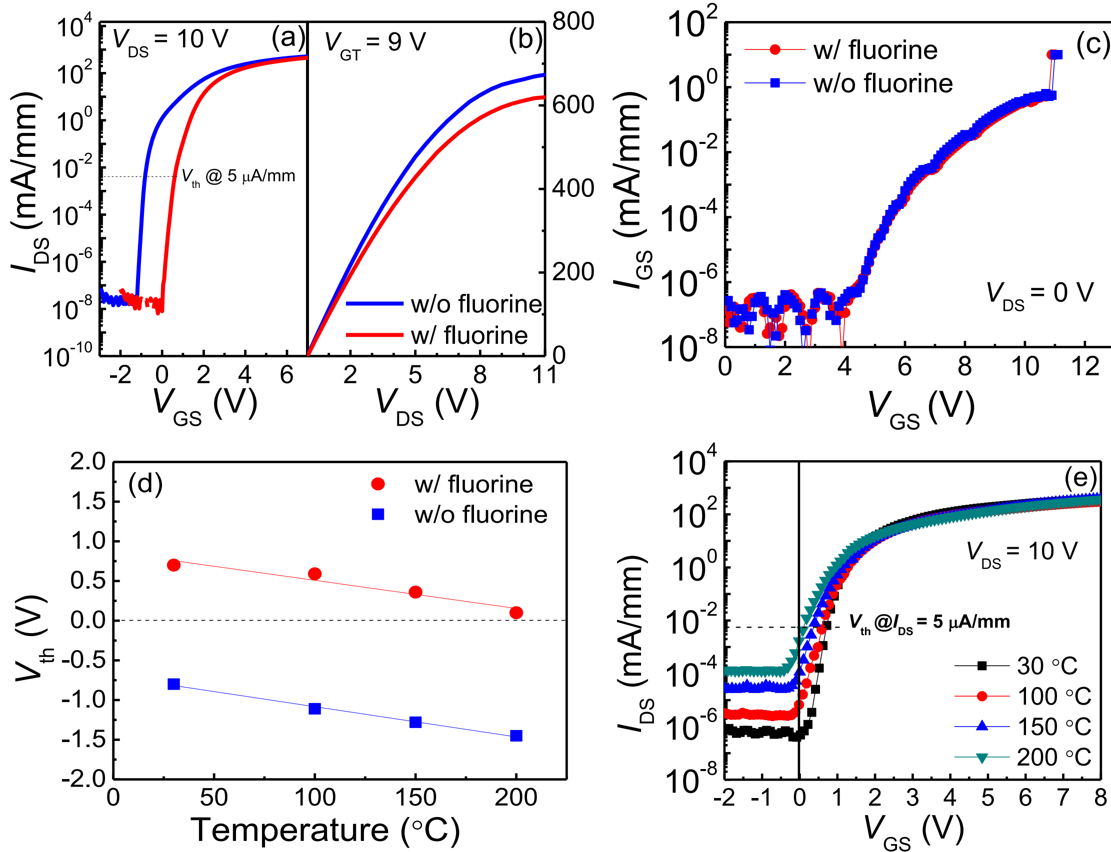

FIGURE 4. (a) I_{DS}–V_{GS} characteristics in the log scale, (b) I_{DS}–V_{DS} characteristics at over drive condition (V_{GT} = 9 V) and (c) I_{GS}-V_{GS} characteristic for device with and without F^- doping. (d) Temperature-dependent V_{th} characteristics of both devices from 30°C to 200°C. (e)Temperature-dependent transfer characteristics of the F^- doped device.

the initial V_{th} value at room temperature. Fig. 4 (e) shows the temperature-dependent transfer characteristics of the F^- doped device. Even at 150° C, the good pinch-off behavior was still observed (I_{DS} = 7.7 × 10^5mA/mm at V_{GS} = 0 V).

Fig. 5 shows the PBTI characteristics of both devices at 30 °C (a) and 150 °C (c). Devices were stressed at a constant positive gate voltage. The stress is periodically interrupted to measure the device DC *I-V* characteristics. The V_{th} was extracted at I_{DS} = 5 μA/mm with V_{DS} = 1 V and R_{ON} was extracted at V_{GS} = 5 V. Similar to PBTI evolution in GaN device and other device technologies [18]–[21], the V_{th} shift (ΔV_{th}) was also observed to follow a power law of the stress time and stress gate overdrive voltage:

$$\Delta V_{th} = A_0 (V_{GS} - V_{th})^{\gamma} t_{stress}^{n} \quad (1)$$

where A is the prefactor and *n* is the time exponent. The time-dependent exponent *n* was estimated by fitting the power law (1) to the ΔVth versus stress time curves at 30 °C [18]. The average *n* value for devices with and without F^- doping were ~0.1 and ~0.11, respectively, which were in the typical range of the reported PBTI results [18], [19]. Both devices have the similar *n* value indicates the quality of the gate insulator was preserved after fluorine ion implantation. Besides, both devices with similar V_{th} shift suggests that F^- doped technology in this work did not generate severe defects and traps in the oxide, which usually attributes to the V_{th} shift during the PBTI measurement, since V_{th} shift in the PBTI is dominated by the pre-existing bulk oxide traps and the interface oxide traps [18], [20]. Small degradation of R_{ON} at same stress condition was also observed in Fig. 5 (b), this is due the low interface trap generation during the PBTI stress [22]–[24].

To investigate high voltage switching performance, the dynamic R_{ON} measurement at high drain bias was conducted using Agilent B1505A with N1267A HVSMU/HCSMU Fast Switch [28]. After high drain voltage stress in OFF-state at V_{GS} = 0 V within 0.5 s, the device was switched to ON-state at V_{GS} = 8 V and V_{DS} = 1 V as shown in Fig. 5 (b). Due to the switching delay at high drain stress voltage, the switching time for OFF-state to ON-state was 60 μs when the drain stress voltage in OFF-state V_{DS} was lower than 200 V and was 150 μs when the drain stress voltage in OFF-state V_{DS} was higher than 200 V. After stressed V_{DS} at 600 V, R_{ON} of the F^- doped device increased only 1.4 times. For short switching time (60 μs) at stress voltage of 200 V, R_{ON} increased only 1.2 times. These results indicate that

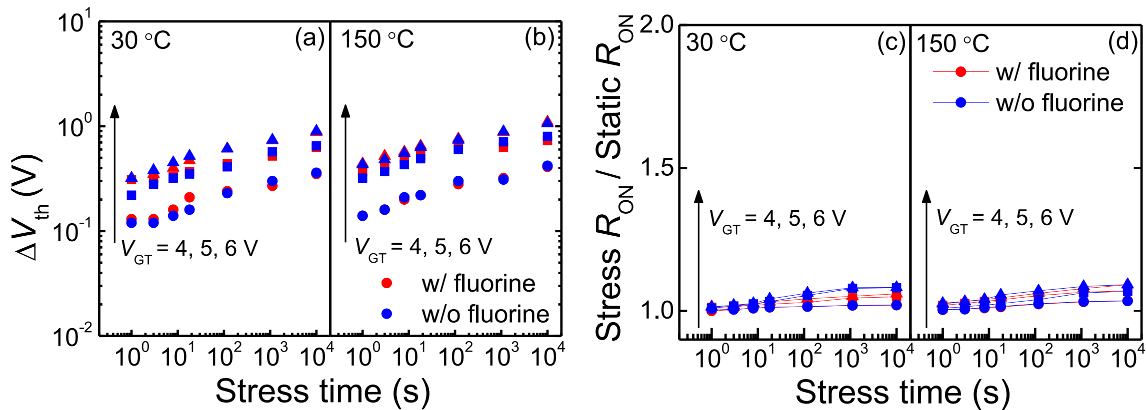

FIGURE 5. Time evolution of V_{th} shift and R_{on} increase under PBTI stress (0–10^4 s) for device with and without F⁻ doping during the gate bias with V_{GT} = 4, 5, 6 V at 30 °C ((a) and (c)) and 150 °C ((b) and (d)).

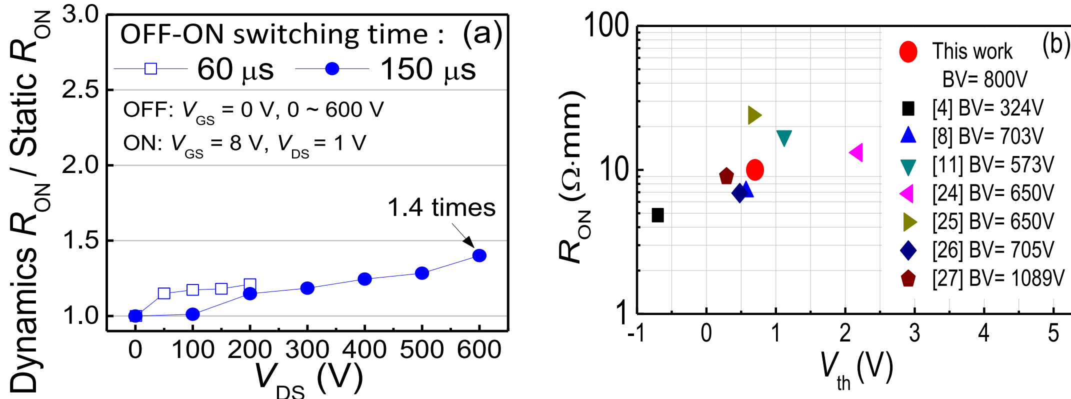

FIGURE 6. (a) Dynamic R_{ON} and static R_{ON} ratio versus drain stress voltage (V_{DS}) for F⁻ doped device. (b) Benchmark of V_{th} and R_{ON} of the fabricated fluorine device with published state-of-the-art normally-off GaN MIS-HEMTs. (V_{th} was determined at I_{DS} = 5 µA/mm.)

low current collapse phenomena exists for the F⁻ doped devices. Besides, it also confirms that the quality of gate insulator was well preserved after fluorine ion implantation and annealing process. The benchmark of V_{th} and R_{ON} with reported normally-OFF GaN MIS-HEMTs is shown in Fig. 6. The fluorine device in this work have higher V_{th} with lower R_{ON} compared to the other reported results.

IV. CONCLUSION

High performance normally-OFF GaN MIS-HEMT was achieved by partial-gate-recess barrier with F⁻ doped gate insulator using standard fluorine ion implantation. Fluorine ions were introduced into both the gate insulator and the recessed barrier layer to increase the positive V_{th} shift with low ion implantation damages. Compared to the fluorine free and recess free device, only about 16% increase of ON-resistance was observed for the F⁻ doped devices. The fabricated F⁻ doped device shows a positive threshold voltage of 0.68 V, a maximum current density of 620 mA/mm, an ON-resistance of 10 Ω·mm, an OFF-state breakdown voltage of 800 V, with low current collapse. The device also shows very low V_{th} shift under thermal stability test and PBTI test. Thus, the proposed normally-OFF GaN MIS-HEMTs architecture in this study is a promising approach for future E-mode GaN power electronics device fabrication.

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