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Multi-V_{th} Strategies of 7-nm node Nanosheet FETs With Limited Nanosheet Spacing

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ABSTRACT In this paper, multi-threshold voltage ($V_{\rm th}$) scheme of 7-nm node nanosheet FETs (NSFETs) with narrow NS spacing were successfully achieved by metal-gate work function (WF) and channel doping ($N_{\rm ch}$) using fully calibrated 3-D TCAD simulations. The limited NS spacing, which allows TiN capping layer only, makes different WF between the edge and the middle part of NS circumference. Unfortunately, this causes non-linear $V_{\rm th}$ shifts and dc performance degradation as a function of WF due to one-side turn-on phenomena between the edge and the middle part. Furthermore, the fixed WF of TiN capping layer limits $V_{\rm th}$ shifts toward ultra-low-power applications. To enable multi-$V_{\rm th}$ of NSFETs, several possible solutions are addressed: changing the $N_{\rm ch}$ and the WF of TiN capping layer. The higher $N_{\rm ch}$ enables lower off-state current while 50-nm-wide three-stacked NS decreases dc performance variations effectively. Changing the WF of TiN capping layer can extend $V_{\rm th}$ margins, but degrade DC performance as a trade-off. Nonetheless, 7-nm node NSFETs adopting these techniques have multi-$V_{\rm th}$ options to satisfy wide ranges from ultra-low-power to high-performance applications.

INDEX TERMS 7-nm node, nanosheet FET (NSFET), nanosheet spacing, work-function metal, multi-V_{th}, TiN capping layer.

I. INTRODUCTION

Silicon fin field-effect transistors (FinFETs) have been successfully scaled down to 10-nm node by increasing fin height/width aspect ratio. Self-aligned diffusion and gate contacts, and dummy gate removal also help to scaling down the devices aggressively [1]. However, the performance improvement while decreasing the short channel effects (SCEs) is highly challenging in the following technology nodes [2], [3].

Meanwhile, the horizontally-stacked nanosheet FETs (NSFETs) have been introduced with great potentials to substitute fin structure by attaining superior electrostatics and greater drive currents with greater effective widths ($W_{\rm eff}$) under the same footprint [4]. In addition, the NS widths of NSFETs can be easily tuned, which allows flexible cell design for power-performance optimization [5]. Threshold voltages (V_{th}) of NSFETs can be modulated by controlling work-function metal (WFM) thickness, but the NS spacing is too thin to fill the WFM in, which brings about non-linear V_{th} sensitivity as a function of WFM thickness [6].

In this work, V_{th} modulations of the 7-nm node NSFETs by different WF of the WFM ($WF_{\rm WFM}$) were analyzed in detail based on TCAD platform calibrated with 10-nm node FinFETs [1] in terms of device structure and performance. Several process techniques that can be adopted to the NSFETs were also addressed for the multi-V_{th} strategy.

II. DEVICE STRUCTURE AND SIMULATION METHODOLOGY

7-nm node three-stacked NSFETs were simulated using Sentaurus TCAD [7]. Drift-diffusion transport equations

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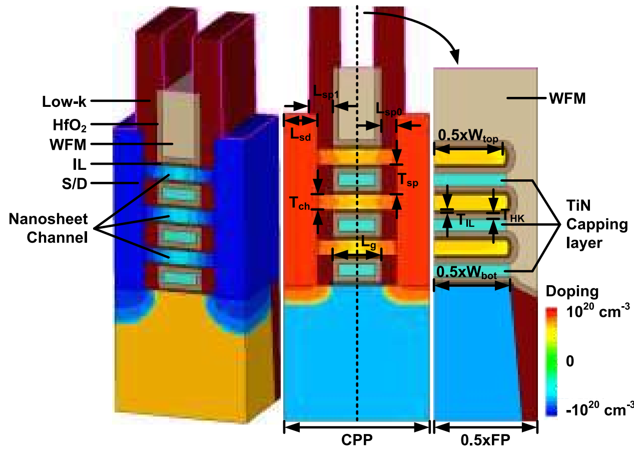

FIGURE 1. Schematic diagram of the NSFETs. Doping profiles for p-type (left), n-type (middle) NSFETs and its cross-section (right) are also specified.

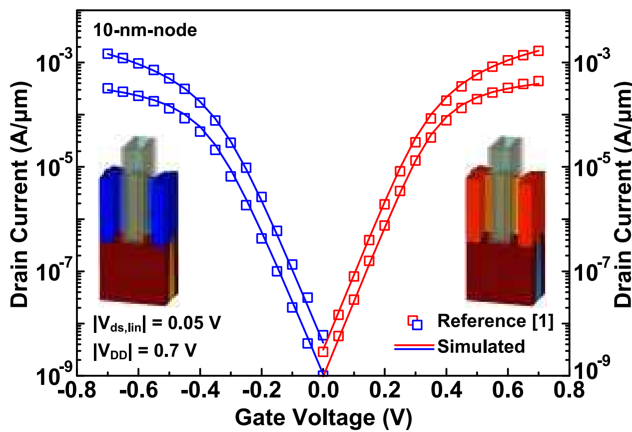

FIGURE 2. TCAD calibration results (lines) with the experimental data (symbols) for the 10-nm node FinFETs [1].

were calculated self-consistently with Poisson, carrier continuity equations, and density-gradient model. Slotboom bandgap narrowing model was considered for all the Si and SiGe regions. Lombardi mobility model was included to calculate the mobility degradation by remote phonon and Coulomb scatterings at the channel/insulator interface. Inversion & accumulation layer and thin-layer mobility models were included to consider impurity, phonon, and surface roughness scatterings. Low-field ballistic mobility model was considered as well. Shockley-Read-Hall, Auger, and Hurkx band-to-band tunneling recombination models were used. Stress-induced changes in band structure, effective masses, effective density-of-states, and carrier mobility were also included.

Fig. 1 shows the schematic diagram of the p-type (left), n-type (middle) of NSFETs and its cross-section (right). The NSFETs were simulated by following the gate-last process flow described in [4]; three-stacked NS structure was formed by depositing Si/$Si_{0.7}Ge_{0.3}$ multi-layer channel epitaxy and etching $Si_{0.7}Ge_{0.3}$ regions selectively. Ge

TABLE 1. Geometrical parameters for 7-nm node NSFETs.

	Geometrical Parameters	Values (nm)
L_g	Gate length	16
T_{ch}	NS thickness	5
T_{sp}	NS spacing	10
L_{sp0}	Spacer length between S/D and MG	5
L_{sp1}	Spacer length between M0 and MG	7
L_{sd}	S/D length	11
T_{IL}	Interfacial layer thickness	1
T_{HK}	High-k thickness	2
FP	Fin pitch	68
CPP	Contacted poly (gate) pitch	48
W_{top}	Top-side NS width	45
W_{bot}	Bottom-side NS width	50

intermixing between Si and $Si_{0.7}Ge_{0.3}$ layers under STI annealing was also performed to consider the changes of energy bandgap and carrier mobility by Ge mole fraction within the NSFETs. Geometrical parameters of the NSFETs are defined in Table 1. Due to the High-k (HK) and interfacial layer (IL) regions, only 4-nm-thick region remains for the NS spacing. TiN capping layer is 2 nm at least [8], and thus, fills the remnant NS spacing. Since WFM is not possible to be deposited within the NS spacing, the WF values between the edge (WFM) and the middle (TiN capping layer) of the NS are different. Although TiN capping layer surrounds the NS in reality, the region of WFM on the TiN capping layer is separated with the region of TiN capping layer only to reflect the change of WF values in this simulation work (right in Fig. 1).

Channel and substrate regions were doped with boron (phosphorus) at 10^{15} and 2×10^{18} cm^{-3}, and source/drain (S/D) regions were doped highly with phosphorus (boron) at 10^{20} (5×10^{20}) cm^{-3} for n-type (p-type) devices, calibrated with 10-nm node FinFETs [1]. For all the FETs, dielectric constants of IL, HK, and low-k regions were 3.9, 22, and 5.0, respectively.

Physical parameters such as minimum low-field mobility, ballistic coefficients, and saturation velocity are finely tuned to calibrate the 10-nm node FinFETs (Fig. 2). Parasitic resistances are fixed constant as 50 $\Omega \cdot \mu m$ for each S/D regions. All the drain currents (I_{ds}) were normalized to the fin pitch, and the operation voltage (V_{DD}) is equal to 0.7 V. Subthreshold swing and drain-induced barrier lowering of n- and p-type FinFETs are fitted by changing S/D doping and junction gradient.

III. RESULTS AND DISCUSSION

Fig. 3 shows the transfer characteristics of the NSFETs having different WF_{WFM} from 4.22 to 4.82 eV but fixed WF of the TiN capping layer ($WF_{TiN,capping}$) to 4.52 eV, which is the average value for TiN [9]. The WF_{WFM} shifts the I_{ds} of both n- and p-type NSFETs, but the I_{ds} do not shift at some WF_{WFM} from 4.52 to 4.82 eV (4.22 to 4.52 eV) for n-type (p-type) NSFETs. It means that there is no more WF_{WFM} modulation once $WF_{TiN,capping}$ is turned on. Furthermore, in case of n-type NSFETs, WF_{WFM} modulation is not able

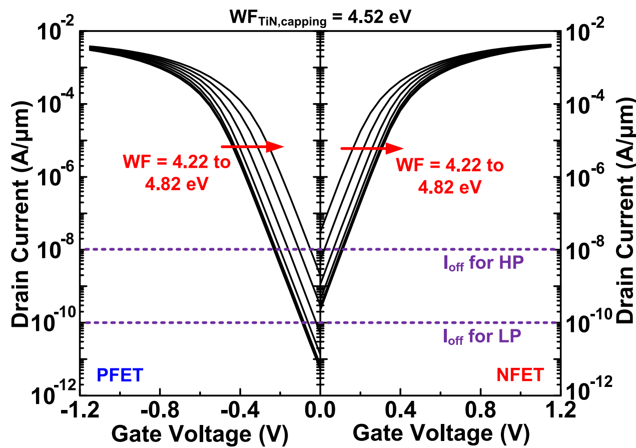

FIGURE 3. Transfer characteristics of the NSFETs having different WF of the WFM (WF_{WFM}) from 4.22 to 4.82 eV in steps of 0.10 eV but the same WF of the TiN capping layer ($WF_{TiN,capping}$) of 4.52 eV.

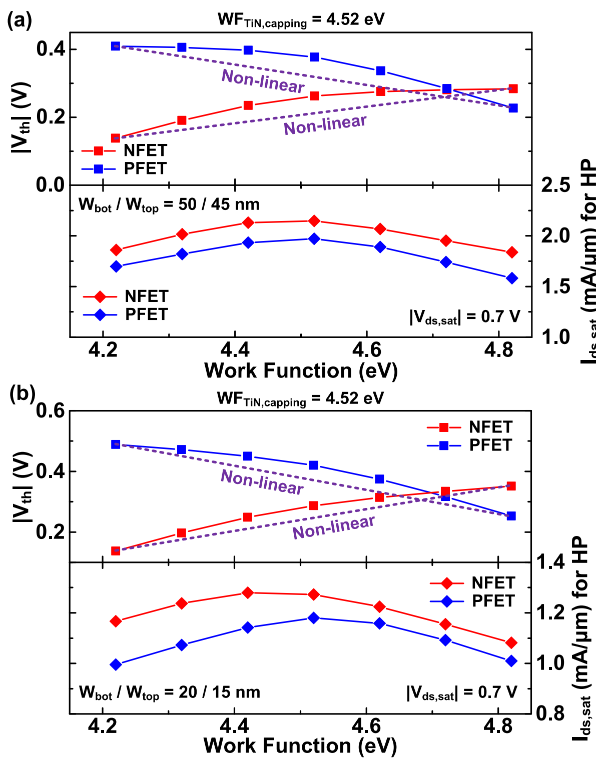

FIGURE 4. Threshold voltages (V_{th}) and I_{ds} at on-state ($I_{ds,sat}$) satisfying high-performance (HP) applications of the NSFETs having W_{bot}/W_{top} of (a) 50/45 and (b) 20/15 nm.

to satisfy the off-state current (I_{off}) for low-power (LP) applications.

V_{th} and saturation I_{ds} ($I_{ds,sat}$) satisfying I_{off} for high-performance (HP) applications at different WF_{WFM} are shown (Fig. 4). V_{th} are extracted using constant current method at $W_{eff}/L_g \times 10^{-7}$, and $I_{ds,sat}$ are extracted from I_{ds} at on-state ($V_{gs} = V_{ds} = V_{DD}$) at the fixed I_{off}. In general, V_{th} is shifted linearly by WF_{WFM}, but non-linear V_{th} shifts with respect to WF_{WFM} are obtained for both n- and p-type NSFETs having W_{bot}/W_{top} of 50/45 and 20/15 nm. In addition, $I_{ds,sat}$ decreases as the WF_{WFM} changes with respect to $WF_{TiN,capping}$ of 4.52 eV.

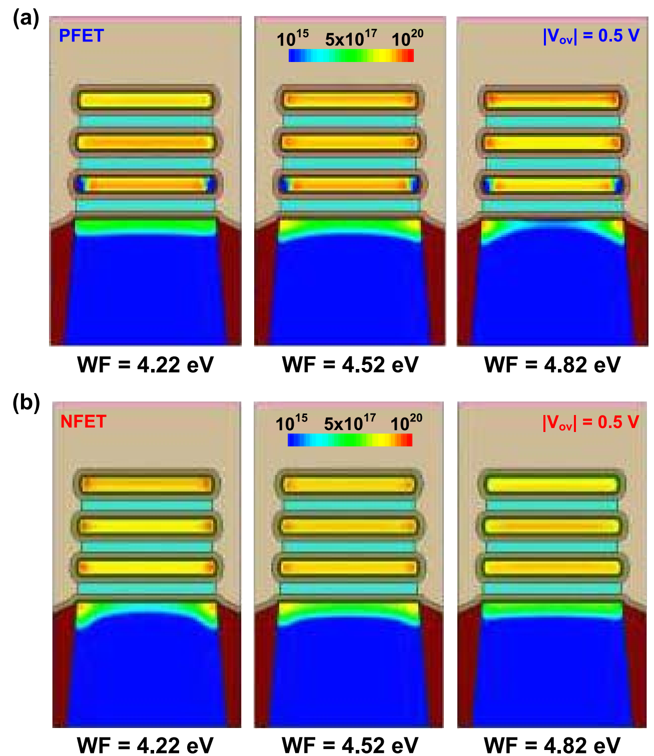

FIGURE 5. Carrier density of the NSFETs having different WF_{WFM} (light brown region, specified in Fig. 1) at the gate overdrive voltage (V_{ov}) of 0.5 V.

These abnormal DC characteristics are explained by the carrier density at the gate overdrive voltage ($V_{ov} = V_{gs} - V_{th}$) of 0.5 V (Fig. 5). At the WF_{WFM} of 4.22 eV, large hole density is formed at the middle of NS adjacent to the TiN capping layer, whereas the top and edge of NS have small amount of hole density. As the WF_{WFM} increases to 4.82 eV, large hole density is formed at the edge of NS adjacent to the WFM, while hole density at the edge of bottom NS channel is almost negligible because phosphorus dopants diffuse to the edge of bottom NS during S/D annealing. The n-type NSFETs, on the other hand, do not have this phenomena because of boron segregation at the $Si_{0.7}Ge_{0.3}$ dummy NS spacing layer [10]. The n-type NSFETs have the changing trend of carrier opposite to p-type NSFETs; large electron density is formed at the edge of NS as the WF_{WFM} becomes smaller toward 4.22 eV.

This can be explained as two transistors having different WF connected in parallel: one transistor having WF_{WFM}, and the other having $WF_{TiN,capping}$. For the W_{bot}/W_{top} of 50/45 nm, TiN capping layer holds 75 % (= $(W_{top}+W_{bot})\times 2.5/W_{eff}$) out of total W_{eff} (= $(W_{top}+W_{bot})\times 3+T_{NS}\times 6$), whereas WFM takes 25 % as for the rest. Because the NS channels adjacent to the TiN capping layer dominantly affect the DC performance and are not

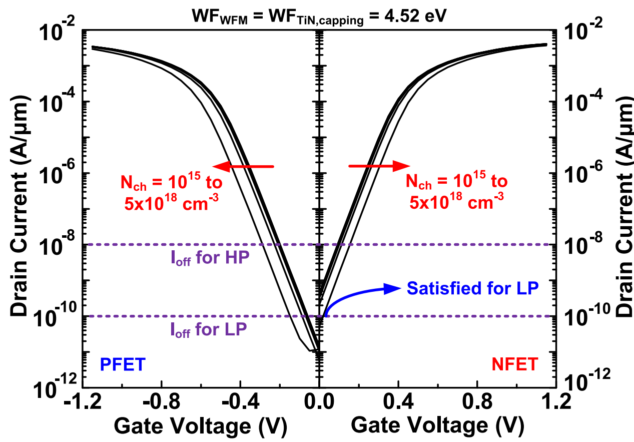

FIGURE 6. Transfer characteristics of the NSFETs having different channel doping (N_{ch}) from 10^{15} to 5×10^{18} cm^{-3} at the same WF of 4.52 eV.

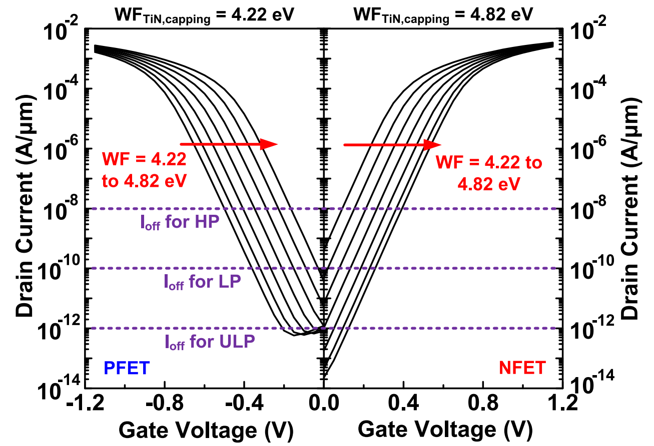

FIGURE 7. Transfer characteristics of the NSFETs having different WF_{WFM} from 4.22 to 4.82 eV, but different $WF_{TiN,capping}$ between p-type (4.22 eV) and n-type (4.82 eV).

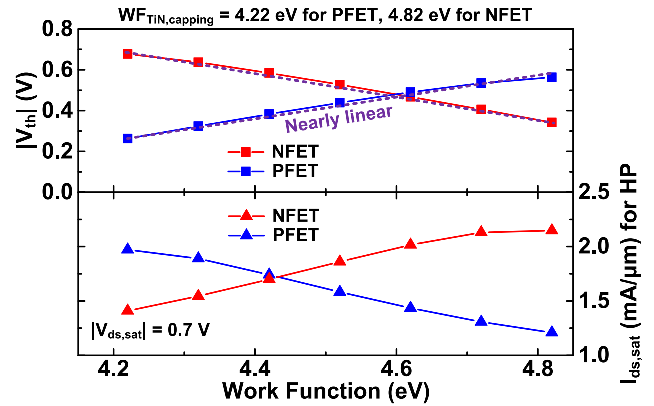

FIGURE 8. V_{th} and $I_{ds,sat}$ for HP applications of the p-type (n-type) NSFETs with the $WF_{TiN,capping}$ of 4.22 (4.82) eV.

controlled by the WFM, I_{off} of the NSFETs do not decrease below the I_{off} which the transistor with $WF_{TiN,capping}$ has. On the other hand, for the W_{bot}/W_{top} of 15/20 nm, TiN capping layer holds 65 %, which alleviates the $I_{ds,sat}$ degradation and non-linearity of V_{th} with respect to WF_{WFM}.

As the WF difference between WFM and TiN capping layer increases, either middle or edge of the NS decreases the carrier density with respect to the same $WF_{TiN,capping}$ at the same V_{ov}, thus degrading $I_{ds,sat}$ (Fig. 4). The one-side turn-on phenomena would likely affect two maximum transconductance ($g_{m,max}$) peaks, but all the NSFETs have the single $g_{m,max}$at the drain voltages (V_{ds}) of 0.05 and 0.7 V (not shown).

On this wise, the fixed $WF_{TiN,capping}$ makes multi-V_{th} via WF_{WFM} difficult. To enable multi-V_{th} scheme, there are three options applicable to the NSFETs. First, increasing channel doping (N_{ch}) can shift the I_{ds} curves further toward lower I_{off} (Fig. 6). This enables n-type NSFETs satisfying LP applications, and the $I_{ds,sat}$ are not degraded much compared to the WF_{WFM} control. $I_{ds,sat}$ for HP applications of the n-type (p-type) devices decrease slightly from 2.15 (1.97) mA/μm for the N_{ch} of 10^{15} cm^{-3} to 2.10 (1.95) mA/μm for the N_{ch} of 5×10^{18} cm^{-3}. However, the V_{th} shift is effective only when the N_{ch} is greater than 10^{18} cm^{-3} because the active channel volume is small.

DC performance variations induced by N_{ch} as well as S/D doping are investigated using impedance field method [11]. The number of samples is 10000 for N_{ch} each. The standard deviations of V_{th} (σV_{th}) are 9.1 mV (10.9 mV) at the N_{ch} of $2 \times 10^{18}cm^{-3}$ for n-type (p-type) NSFETs, slightly larger than undoped nanowire FETs [12] but much smaller than doped FinFETs [13] because the NSFETs have 50-nm-wide and three-stacked NS, decreasing DC performance variations according to Pelgrom's law [14]. These values are not large compared to other variability factors such as line-edge roughness and WF variation of nanoscale devices [15], [16], thus the doped NSFETs until the N_{ch} of $2 \times 10^{18}cm^{-3}$ are feasible without the random dopant fluctuation (RDF) concerns. However, at the N_{ch} of $5 \times 10^{18}cm^{-3}$, σV_{th} increase greatly to 24.5 mV (48.2 mV) for n-type (p-type) NSFETs. In addition, the V_{th} mismatches ($A_{Vth} = \sigma V_{th} \times (W_{eff} \cdot L_g)^{1/2}$ [17]) by RDF are 1.74 (3.43) mV·μm for n-type (p-type) NSFETs, comparable to or larger than the A_{Vth} by total variability concerns of nanowire FETs [17], [18], thus not desirable for V_{th} shift strategy.

Second, changing the $WF_{TiN,capping}$ to other WF values can shift the I_{ds} curves effectively by the WF_{WFM}. This technique makes possible for the NSFETs to satisfy HP, LP, and ultra-LP (ULP) applications (Fig. 7). The high gate-induced drain leakage currents for p-type NSFETs at low $|V_{gs}|$are due to the large junction gradient of boron diffusing into the NS channel [19], [20].

V_{th} and $I_{ds,sat}$ with different $WF_{TiN,capping}$ between n-type and p-type NSFETs are investigated (Fig. 8). Compared to the single $WF_{TiN,capping}$ of 4.52 eV in Fig. 4, having two different $WF_{TiN,capping}$ enables wide and linear V_{th} shifts

with respect to the WF_{WFM} ($\Delta V_{th}/\Delta WF_{WFM} = 0.51$ V/eV and -0.57 V/eV for n- and p-type NSFETs, respectively). However as explained in Fig. 5, the larger difference of WF between WFM and TiN capping layer degrades $I_{ds,sat}$ much as a trade-off for multi-V_{th} options.

Final technique to satisfy both LP and HP applications of the NSFETs is adjusting single-valued $WF_{TiN,capping}$ between 4.56 and 4.62 eV by shifting I_{ds} curves toward right slightly (not shown). This does not degrade the $I_{ds,sat}$ as much as two $WF_{TiN,capping}$ technique as shown in Figs. 7 and 8, and is also immune to RDF.

IV. CONCLUSION

The effects of WFM and N_{ch} in 7-nm node NSFETs were analyzed in detail for multi-V_{th} strategy. Because of 10-nm-thin NS spacing filled by IL, HK, and TiN capping layer, the fixed $WF_{TiN,capping}$ limits the V_{th} shifts to a certain point, unable to satisfy the LP conditions for n-type NSFETs. Using the concept of two transistors having different WF connected in parallel, the limitation of V_{th} shifts and the degradation of $I_{ds,sat}$ are explained. To satisfy multi-V_{th} scheme, several possible techniques are addressed: increasing N_{ch}, separating $WF_{TiN,capping}$ for n- and p-type, and adjusting $WF_{TiN,capping}$ between 4.56 and 4.62 eV. The N_{ch} up to $2 \times 10^{18}\text{cm}^{-3}$ can modulate the V_{th} of the NSFETs without the DC performance degradations as well as its RDF concerns. In spite of certain DC performance variations, WFM is able to shift V_{th} while satisfying both LP and HP applications.

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