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Plasma Charging Effect on the Reliability of Copper BEOL Structures in Advanced FinFET Technologies

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ABSTRACT Plasma induced damage remains a critical concern in VLSI manufacturing process as a result of the introduction of the high-k and low-k dielectric layers and complicated 3D structures in advanced technology nodes. In this paper, the level of plasma induced charging distribution on a wafer is studied comprehensively. A strong correlation between the charging level and the geometry as well as densities ratio of via structures in dual damascene BEOL copper processes is found. In addition, the effect of plasma charging on Cu corrosion is studied in this paper. To investigate the root causes of such failure mode, an in-situ plasma charging recorder is embedded with RC test structures formed by Cu BEOL processes. The recorded charging current has a strong effect on the reliability levels of the via-chain resistors and backend capacitors. Experimental data suggests that plasma charging effect not only leads to gate dielectric stress on transistors but also affects the reliability performances of the copper interconnects.

INDEX TERMS Cu corrosion, VIMIC, plasma induced charging, PID, BEOL, FinFET.

I. INTRODUCTION

For decades, IC advancements have been the main driver for CMOS technologies. As integrated circuits continue to scale aggressively, with the introduction of complicated 3D and high aspect ratio structures, plasma induced damage (PID) can become problematic for circuit fabricated by advanced FinFET process [1], [2]. Over the years, extensive studies on the topic of plasma induced damages have been reported [4]–[6]. Conventionally, test patterns for monitoring plasma induced damage levels generally contain devices with large antenna ratio for analyzing stress effects on gate dielectric layers [7]–[9]. The demand for optimized, complex circuits with increasing functionalities has driven the rapid development of advanced CMOS technologies. It gives rise to the complex stacking of metal lines and via layers in BEOL interconnects [10], [11]. Plasma induced charging levels are expected to be subjected to geometric and density effect in via and metal patterns in dual damascene process [12], [13]. In addition, plasma induced stress may also lead to failures in interconnect structures. Hence, antenna ratio might not be sufficient and suitable for monitoring plasma induced latent damage occurring in back-end structures. An in-situ plasma charging recorder coupled by antennas which has been reported in earlier studies [14], [15] designed with different geometric structures are used instead in this study. Experimental data indicates that not only does antenna ratio plays an important role in plasma induced stress but via structure/density can also significantly affect the plasma charging level on test samples formed by Cu BEOL processes.

As mentioned, the increase in the number of metal and via layers may cause more severe plasma induced damage in integrated circuits with complex interconnects. In recent years, copper (Cu) has been widely incorporated as the interconnecting metal and via in CMOS integrated circuit technologies beyond 0.13mm node [16], [17]. Cu interconnects has enabled further reduction in metal resistivity, essential for circuits with dense metal lines and increased layers of metal stacks [18], [19]. In advanced technology nodes, thinner and narrower lines make copper interconnects more

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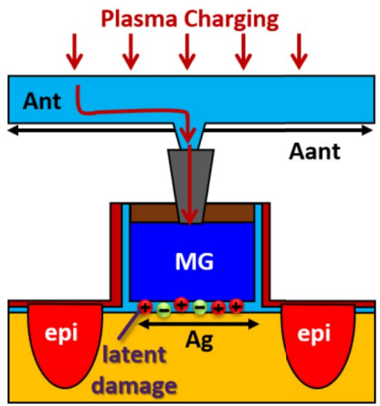


FIGURE 1. **Plasma induced effect in traditional plasma detector. Plasma density stresses oxide and leads to latent oxide damages.**

prone to reliability challenges, thus more likely to result in failures after stress or yield problems [20], [21]. For example, in dual damascene processes, copper voids may occur due to non-uniformly deposited Cu after via/trench etching steps [22], [23]. Copper corrosion (Cu corrosion) is found to be one of the failure modes that affects the stability and yield in the production lines which employ narrow/dense interconnects [24]–[26]. Some studies have suggested that Cu corrosion might be induced by the residual charging effect caused by BEOL plasma treatments [27]. In this work, incorporating the plasma charging recorders developed on FinFET technologies [14], [15], experiments are performed to study the correlations between the plasma charging level and the reliability characteristics of the copper interconnect structures.

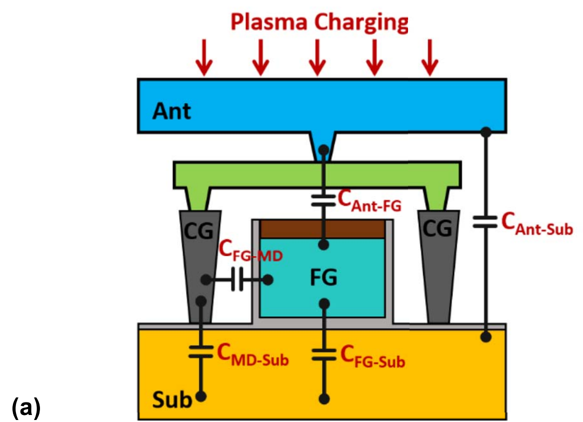
II. DETECTION OF PLASMA INDUCED CHARGING EFFECT

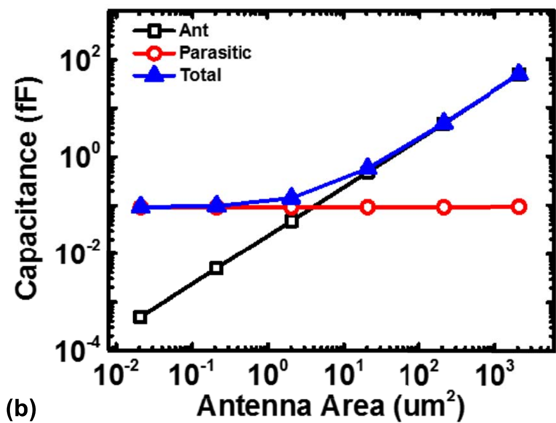
Traditional antenna charging theory indicates that plasma current is proportional to the exposed antenna area. The most critical layers subjecting to plasma charging damage is generally believed to be the gate dielectric layer on transistors. It is expected that the latent oxide damages on the gate oxide, caused by the discharging of plasma induced current, is proportional to the amount of charge collected, hence, can be increased by the antenna ratio of a test pattern [28].

In conventional PID test patterns, see Figure 1, the definition of antenna ratio (AR) is the ratio of the antenna area (A_{ant}) of antenna metal layer to the gate area in the test transistor (A_g), as depicted in the equation which is shown below.

$$AR = \frac{A_{ant}}{A_g}$$

During plasma process, electrons and ions may both be impinged on the exposed antenna structure, defined mostly by one or more metal layers. Plasma charge collected by the antenna is expected to discharge mostly through the gate dielectric layer. Hence, test samples experience high





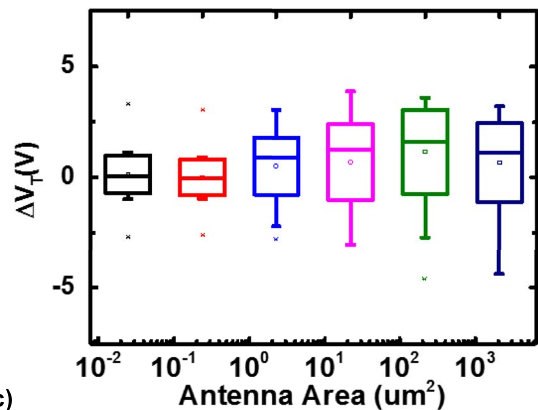


FIGURE 2. **(a) Illustration of capacitance (b) As AR exceed 2um², C_{Ant} becomes the major component of C_{total} and (c) ΔV_T saturates.**

stress current and induced damages on the gate dielectric, see Figure 1. This conventional PID monitor structure can only reflect discharging stress through gate dielectric, which might be insufficient for the study of PID on backend RC structures.

A plasma charging recorder proposed in previous studies [14], [15] can record the charging current level by connecting the antenna structure to the coupling gate. In FinFET technologies, the corresponding structure is illustrated in Figure 2(a), where a floating gate (FG) is coupled

by closely placed slot contacts, as its coupling gate (CG). Its floating gate (FG) is coupled by long contact slots which are connected to an antenna, composed of a large metal structure. During plasma process, the antenna collects charge and the potential on the antenna gate raises. As the high voltage is coupled to the floating gate, it induces charge injection to / ejection from the floating gate during plasma charging. The stored floating gate charges which reflect the charging level can be read out after wafer fab out. As the antenna/coupling gate potential is raised during plasma process, charge will be injected into or ejected out of the FG, recording the charging level. The amount of the charge in FG can then be read out by finding the shift on the threshold voltage (ΔV_T) of the FG transistor. ΔV_T is found to be linearly proportional to the plasma charging current density at the location where the plasma charging recorded in placed on a wafer [14], [15].

To further understand the effect of antenna area designed in this plasma charging recorder, assume the plasma charge current density on a wafer is J_p, the total charging current on a device with antenna area of A_{ant} is I_p, and $I_p = J_p \times A_{ant}$. Defining the total capacitance (C_T) on antenna plus coupling gate structure as followed,

$$C_T = C_{Ant} \parallel C_{parasitic}$$

where $C_T \propto A_{ant}$, then the potential on CG should reach the same level. Figure 2(a) indicates the main compositions of capacitance of the recorder in FinFET technology, which are capacitance between antenna and substrate, where $C_{Ant} \propto A_{ant}$, and the parasitic capacitance ($C_{parasitic}$) contributed mostly by the coupling and connecting structures. Figure 2(b) shows the total capacitance being dominated by Antenna structure as its area exceeds 2 μm^2. Once the total capacitance increases proportionally with antenna area (A_{ant}), the charging rate on CG node remains the same level. Hence, the threshold voltage shift saturates when C_{Ant} dominates the total capacitance, as demonstrated in Figure 2(c). Without a large antenna, the size of this in-situ plasma charging recorder could be reduced while not affecting its ability to detect plasma induced damage in advanced technologies. Therefore, higher spatial resolution for detecting the distribution of local plasma charging effect as well as the study of patterning effect can be achieved.

III. PATERN EFFECT ON PLASMA CHARGING LEVEL

Conventionally, antenna ratio is the main parameter to elevate the level of charging stress in an experiment [29]. As antenna area increases, the total amount of plasma induced charge collected increases proportionally. The collected charges mainly discharge through thin gate dielectric region. Hence, it is well-known that increased antenna ratio raises the stress current density, as suggested in the following expression.

$$J_{stress} = \frac{Q_p}{A_g} = J_p \frac{A_{ant}}{A_g}$$

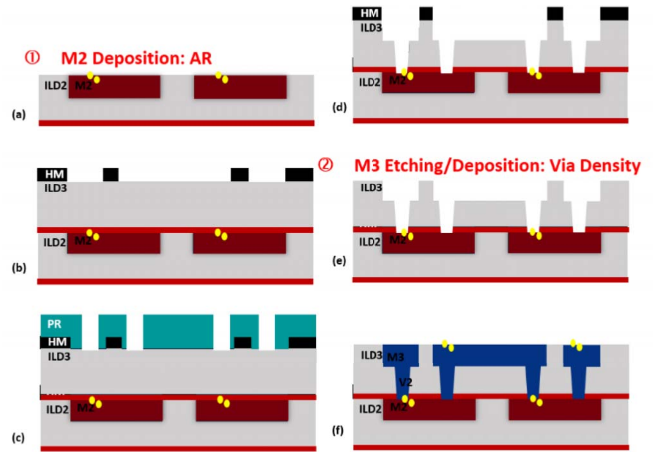


FIGURE 3. Processing steps in dual damascene of BEOL and the illustrations of how plasma induces damages during etching/deposition steps, suggesting two major factors, AR and via densities, both have significant impacts.

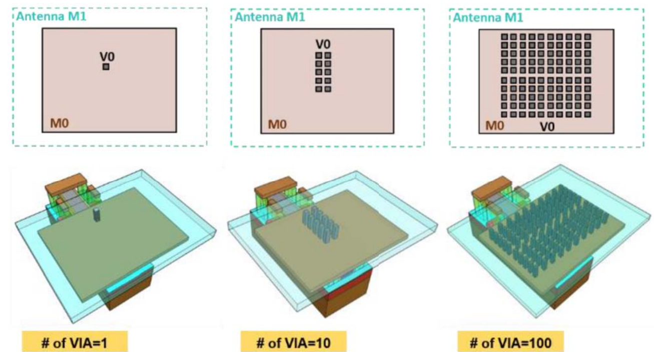


FIGURE 4. The pattern of PID recorder with different via density.

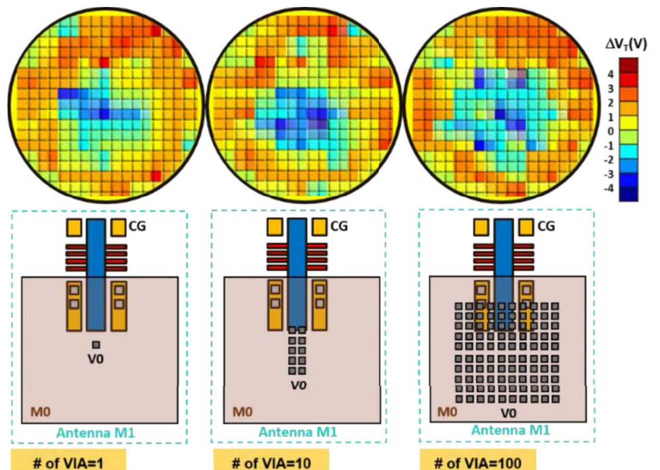


FIGURE 5. Wafer maps exhibit a clear negative shift in charging area on the center of wafer as the number of vias rises.

in which, J_{stress} is the stress current density through oxide, and Q_p is the plasma charge during plasma process.

However, after examining the dual damascene process, it is found that antenna area is not the only factor affecting

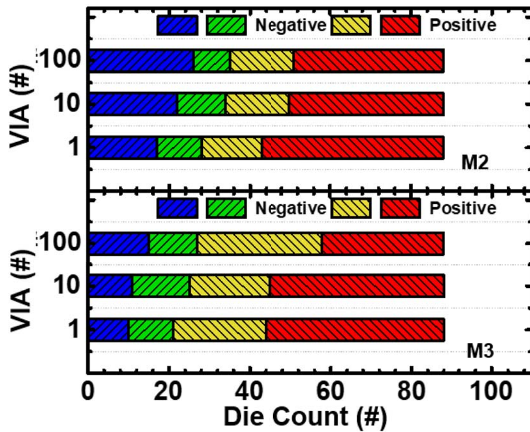


FIGURE 6. Number of dies that are negatively charged increase while number of vias increase in Metal2 and Metal3.

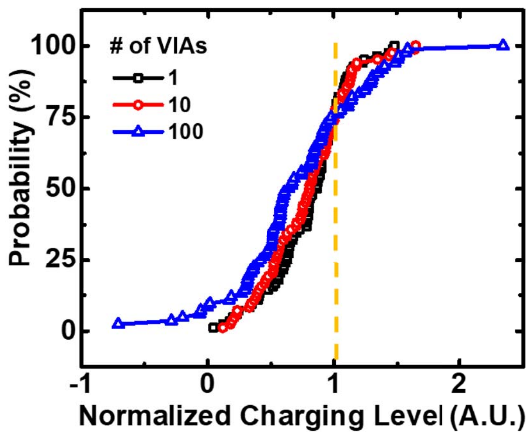


FIGURE 7. The probability distribution shows severe charging level during plasma process as a result of increase in number of vias.

the amount of collected charge. The simplified flow to the dual damascene process for producing Cu interconnects is illustrated in Figure 3. Here, metal 2 to metal 3 connections are used as an example. After the formation of metal2, the etching process of via2 and metal3 patterns was performed. At this process step, via density decides the contact area at the top of metal2, indicating the plasma charging level on metal2. To study the effect of via patterns, different numbers of via is placed above a fixed area of metal0 of PID recorder, creating test devices with different via densities, while the antenna area of metal1 remains the same at 20 μm^2, as illustrated in Fig. 4.

In this work, the charging recorder is designed with different via density to investigate the effect of via patterns on plasma charging level on a sample. Figure 5 presents wafer maps of ΔV_T on PID recorder with different number of vias on a particular test pattern. Measurement results indicate that the higher via density is, the more negative charging level is recorded. PID recorder is also designed with via0-metal1, via1-metal2 and via2-metal3 patterns. As summarized in Figure 6, measurement data reveal that as via density increases, the number of positively charge dies across the wafer also increases. The normalized charging levels of all PID recorders on each dies are compared in the cumulative plot of Figure 7. When more vias are placed on a test sample, the underneath metals are expected to be subjected with higher level of plasma induced charging rate, as the larger number of trenches are being etched, see Figure 3. During fabrication process, the acids would attract the Cu^{2+} ions leaving electrons behind [30], then collected by the antenna. The negatively charged CG will lead to positive FG charge, which in turn results in a negative shift in the threshold voltage readout. The effect of via density can be critical for devices which are connected to large amount of vias, and affect the future design rule modifications.

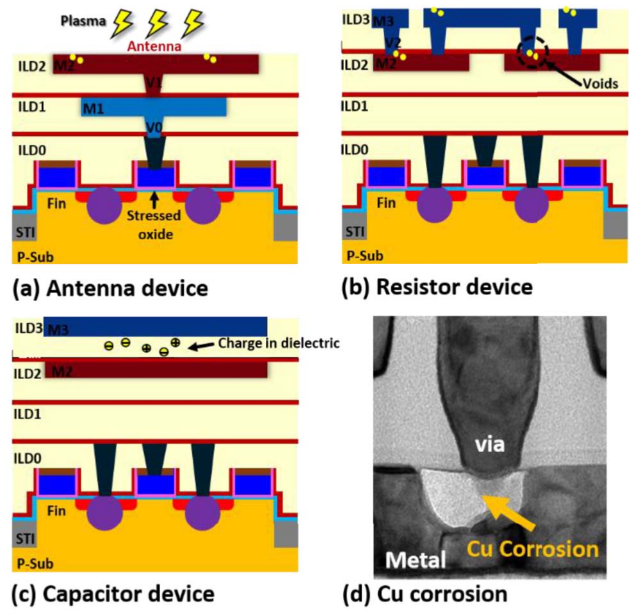


FIGURE 8. Plasma charging effect can lead to (a) gate dielectric layer breakdown (b) void in via-chain resistor and (c) trapped charges in ILD (d) TEM of Cu Corrosion between via and metal resulting in interconnect wiring faults.

IV. PLASMA CHARGING EFFECTS ON COPPER INTERCONNECTION RELIABILITY

In our previous works [14], [15], a new PID recorder is proposed and demonstrated. In this extended study, by using the same PID recorder, strong correlations between plasma charging stress and the damage to BEOL structure, such as, resistor chain and inter-metal capacitance are observed. Figure 8 is composed of four diagrams illustrating the cross-sections of different copper BEOL structures, which are subject to different plasma damage in advanced FinFET technology. Conventionally, the most critical PID is believed to occur in the gate dielectric layer as it experiences high stressed current during plasma processes, as illustrated Figure 8(a). It has been previously reported that the time-to-breakdown characteristics of the gate-dielectric layer are

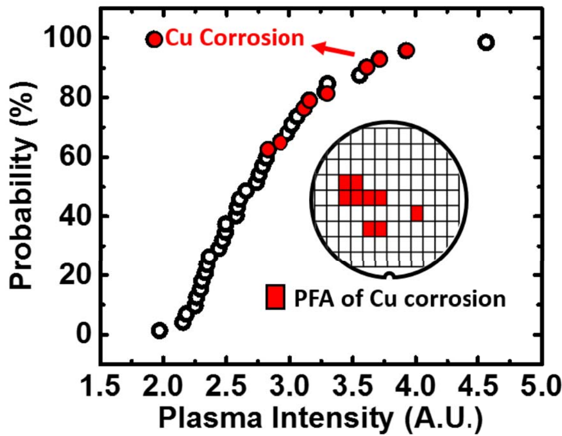


FIGURE 9. Sites where Cu corrosion concurs with dies having experienced high plasma current, as marked red on the wafer.

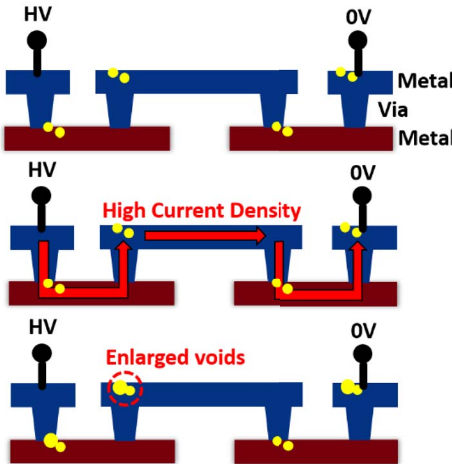


FIGURE 10. Under high voltage stress, latent plasma induced damage (PID) is further exacerbated as a result of electro-migration.

strongly correlated to the stress level of its experience during plasma treatments [15]. In addition, plasma charging effect can also lead to stress and or damage in interconnects and capacitors formed by the backend layers. To monitor the copper BEOL reliability, test structures of via-chain resistor as shown in Figure 8(b), are used for investigating its plasma charging levels. Figure 8(c) demonstrates a finger typed metal-to-metal capacitor for monitoring the plasma damage on ILD layers. Through methods of accelerating test, latent damages in the metal/via connections and on the inter-metal dielectric layers can be revealed. An example of Cu corrosion on sample subjected to high plasma stress is shown in Figure 8(d), where corrosion site is found to occur most likely at metal/via interfaces. This type of interconnect failure is also referred as Via Induced Metal Island Corrosion (VIMIC) [32].

During a dual damascene process, charged metal could be corroded in wet etching steps leading to via landing above a corrosion site [31]. Physical Failure Analysis (PFA)

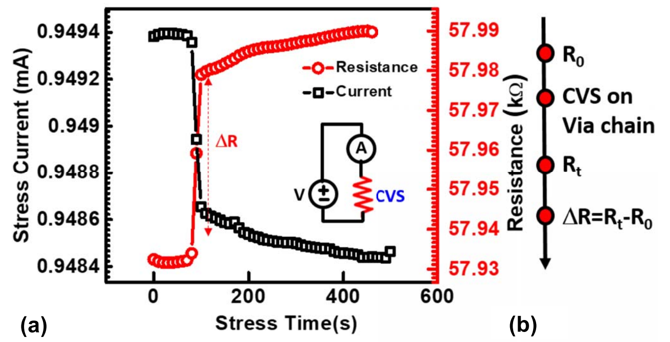


FIGURE 11. (a) Shift in resistance under constant voltage stress of 55V is obtained through the experiment flow illustrated in (b).

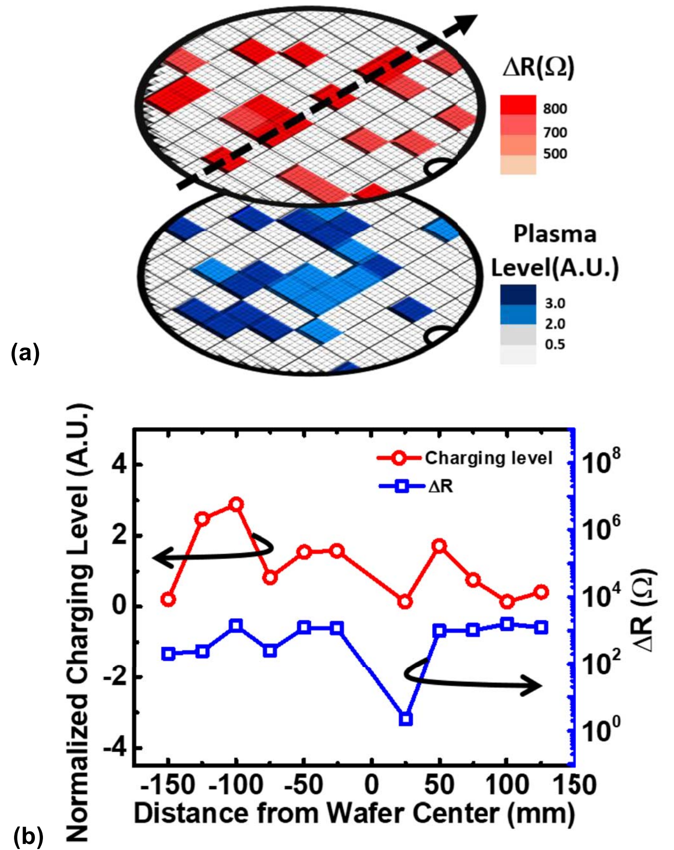


FIGURE 12. (a) Location which recorded a high shift in resistance is marked red on the wafer. Position with high charging level is marked blue. (b) Normalized plasma stress level and shift in resistance across the horizontal cut-line across wafer center correlates with each other.

data suggest the occurrences of Cu corrosion on particular dies coincide with location of higher plasma charging rate, see Figure 9. Cu corrosion occurs in dies that experienced high plasma intensity. The plasma charging level during formation of metal layer can be obtained from the readings of in-situ plasma charging recorder. Such experimental data provide a preliminary indicator of the correlation between induced charging level and Cu corrosion.

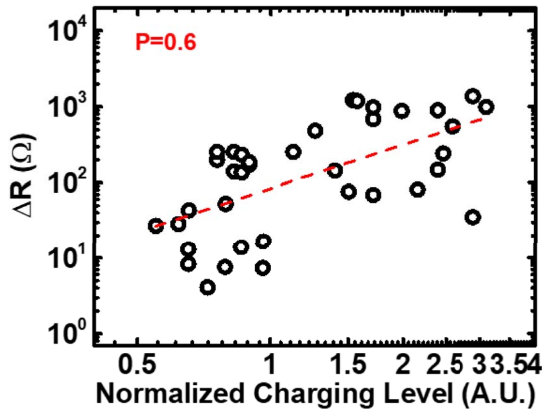
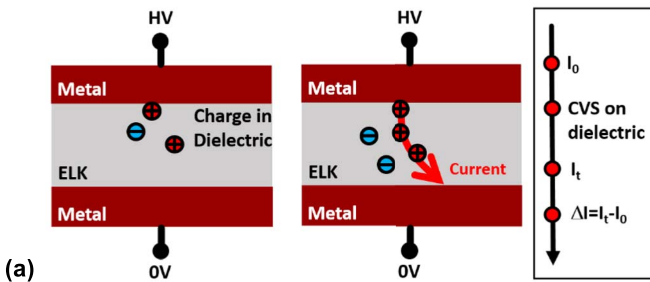


FIGURE 13. High Correlation between shift in resistance of via chain and normalized plasma induced damage level is shown in this plot with correlation coefficient of 0.6.



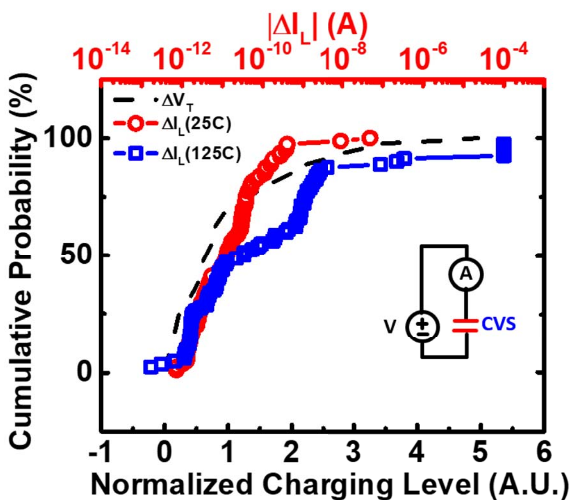


FIGURE 14. (a) The latent damage in ELK was enhanced by constant voltage stress, observed by measuring its leakage current. (b) Cumulative probability plot of normalized charging level and leakage current shift under 25°C and 125°C on plate capacitors after CVS.

V. EXPERIMENTAL RESULTS AND DISCUSSION

Even though Physical Failure Analysis (PFA) can confirm definitively the occurrence of Cu corrosion, it can be costly and time consuming. Through electrical testing of RC patterns after high voltage stress may provide indications of Cu corrosion, which might not be easily observed through PFA, and allows full coverage examination at a faster rate. The following experiments, show the reliability of via-chain resistors

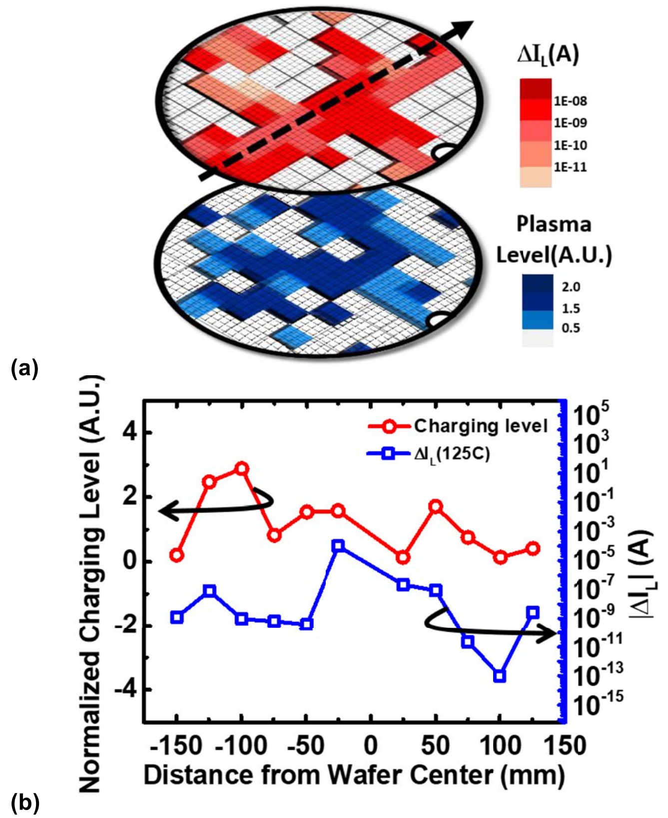


FIGURE 15. (a) Wafer map of leakage current shift under 125°C after constant voltage stress is compared with charging level by PID recorders (b) Comparison of plasma stress level and leakage current change after stress.

and lateral metal-to-metal capacitors, which are investigated to study the correlation between after-stress response and the plasma charging effect.

After constant voltage stress (CVS), small Cu void might be enlarged by electro-migration [33], [34] in via chains. Therefore, resistance levels of sample with small voids are expected to be raised. The effect of electro-migration on resistors with pre-existing voids are illustrated in Figure 10. Plasma charging stress is known to cause small voids during Cu etching and deposition steps [26], [27], as illustrated in Figure 3. When the via-chains structure is subjected to high current stress, these voids serve as seeds for enhanced electro-migration [35]. Hence, the high current stress tests allow us to identify existence of small voids in the via-chain resistors. When high current density flows through the via-chains, the locations where voids exist may experience increased current density. Electro-migration is expected to accelerate the degradation, leading to more pronounced shift in resistance. Figure 11(a) reveals the monitored current under constant voltage stress (CVS).

The flow of obtaining DR is outlined in Figure 11(b). The wafer maps of DR and that on the normalized charging level compared in Figure 12(a) reveal that dies have larger resistance shift also experienced higher plasma induced charging

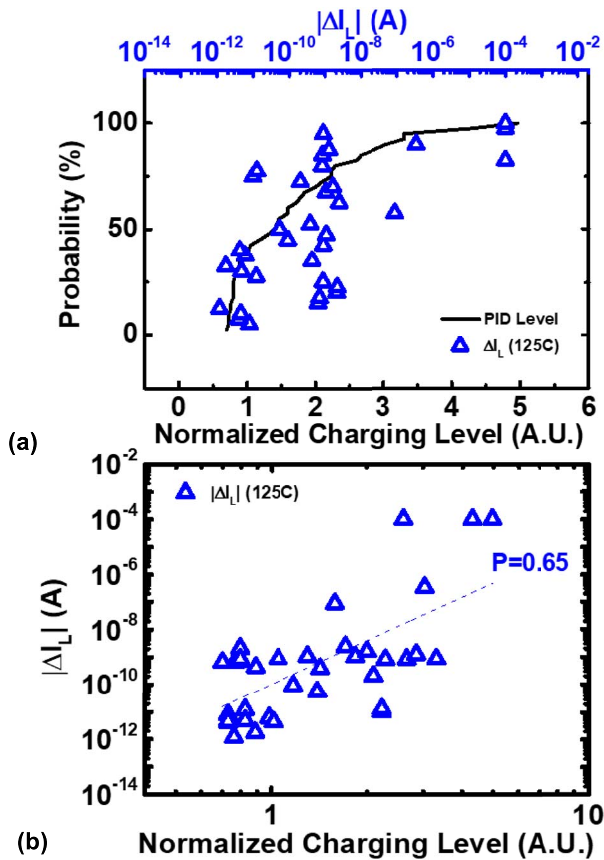


FIGURE 16. (a) Cumulative probability plot of normalized PID level corresponding to leakage current shift under 125°C on plate capacitors after CVS. (b)Interaction between leakage current shift and normalized PID level shows high correlation.

stress. Comparison of normalized plasma stress level and shift in resistance across center cutline of a wafer is compared in Figure 12(b). Strong correlations between DR and normalized charging level are found. The correlation between DR and normalized charging level is further established in Figure 13, revealing a strong Pearson's value.

High plasma charging current may also lead to residue damage in dielectric layers, affecting initial or stress- induced leakage current between two laterally placed metal electrodes. It is generally believed that the latent damages in the dielectric layer can be revealed by constant voltage stress, as illustrated in Figure 14(a). The cumulative distributions of the leakage current shift after a constant voltage stress (CVS) of 20s and normalized plasma charging level recorded on the same die are compared in Figure 14(b). The comparison of shift in leakage current ($|\Delta I_L|$) under 25°C and 125°C after CVS of 20s suggests that over 50% of the dies reveal a more significant shift from the main population. $|DI_L|$ on the capacitor under CVS and normalized charging level from the recorder are compared by wafer maps, as shown in Figure 15(a). The normalized plasma stress level and shift in leakage current on the horizontal cut-line across center of the wafer are arranged in Figure 15(b). The cumulative distributions of normalized charging level and corresponded $|\Delta I_L|$ are further compared in Figure 16(a). After CVS, the conduction path formed as a result of the latent damages inside the dielectric layer is more prominent at high temperature. Strong positive correlation between normalized charging level and $|DI_L|$ under 125°C after CVS are found in Figure 16(b). Accelerated test results on resistors and capacitors show that plasma induced charging stress do have a strong effect on the ILD and interconnection quality in Cu BEOL process. The above results suggest that pattern-dependent plasma charging effect should also be considered in designing complex, multilayer interconnect structures.

VI. CONCLUSION

The in-situ recorder presented is used to investigate plasma charging effect in FinFET processes. The correlation between reliability of copper interconnects and plasma charging stress is established. Experiment results suggest that via density also plays an important role on affecting charge stress level. Experimental data also shows that number of vias on the antenna structure can also affect the type or amount of charging in a test structure. Hence, further optimization of design rules on BEOL structures, is expected to alleviate PID effects on advanced FinFET circuits. Experimental data reveals a strong correlation between plasma charging level and the reliability of BEOL structures. This study provides insights to directions of further optimization for plasma processes while enhancing interconnection reliability and yield in advanced FinFET BEOL processes.

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REFERENCES

[1] K. Eriguchi, Y. Takao, and K. Ono, "A new aspect of plasma-induced physical damage in three-dimensional scaled structures—Sidewall damage by stochastic straggling and sputtering," in *Proc. IEEE Int. Conf. IC Design Technol.*, Austin, TX, USA, 2014, pp. 1–5, doi: 10.1109/ICICDT.2014.6838597.

[2] E. Karl *et al.*, "A 4.6 GHz 162 Mb SRAM design in 22 nm tri-gate CMOS technology with integrated read and write assist circuitry," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 150–158, Jan. 2013, doi: 10.1109/JSSC.2012.2213513.

[3] K. Eriguchi and K. Ono, "Quantitative and comparative characterizations of plasma process-induced damage in advanced metal-oxide-semiconductor devices," *J. Phys. D Appl. Phys.*, vol. 41, Jan. 2008, Art. no. 024002.

[4] M. Akbal, G. Ribes, M. Guillermet, and L. Vallier, "Plasma induced damage investigation in the fully depleted SOI technology," in *Proc. Int. Conf. IC Design Technol. (ICICDT)*, Leuven, Belgium, 2015, pp. 1–4, doi: 10.1109/ICICDT.2015.7165900.

[5] R. Kishida, A. Oshima, and K. Kobayashi, "Negative bias temperature instability caused by plasma induced damage in 65 nm bulk and silicon on thin BOX (SOTB) processes," in *Proc. IEEE Int. Rel. Phys. Symp.*, Monterey, CA, USA, 2015, pp. CA.2.1–CA.2.5, doi: 10.1109/IRPS.2015.7112780.

[6] A. Matsuda, Y. Nakakubo, Y. Takao, K. Eriguchi, and K. Ono, "Atomistic simulations of plasma process-induced Si substrate damage—Effects of substrate bias-power frequency," in *Proc. Int. Conf. IC Design Technol. (ICICDT)*, Pavia, Italy, 2013, pp. 191–194, doi: 10.1109/ICICDT.2013.6563334.

[7] J. Ackaert, E. De Backer, P. Coppens, and M. Creusen, "Prevention of plasma induced damage on thin gate oxide of HDP oxide deposition, metal etch, Ar preclean processing in BEOL sub-half micron CMOS processing," in *Proc. 5th Int. Symp. Plasma Process Induced Damage*, Santa Clara, CA, USA, 2000, pp. 77–80, doi: 10.1109/PPID.2000.870600.

[8] P. Simon, J. M. Luchies, and W. Maly, "Identification of plasma-induced damage conditions in VLSI designs," *IEEE Trans. Semicond. Manuf.*, vol. 13, no. 2, pp. 136–144, May 2000, doi: 10.1109/66.843628.

[9] C. Gill, J. Porter, and P. McEntarfer, "Plasma induced damage on sub-0.5 μm MOSFETs using a CMOS driver as input protection," in *Proc. 3rd Int. Symp. Plasma Process Induced Damage*, Honolulu, HI, USA, 1998, pp. 100–103, doi: 10.1109/PPID.1998.725584.

[10] L. S. Huat *et al.*, "Physical fault isolation of complex BEOL defects in advanced microprocessors using EBAC technique in nano-prober," in *Proc. IEEE 24th Int. Symp. Phys. Failure Anal. Integr. Circuits (IPFA)*, Chengdu, China, 2017, pp. 1–4, doi: 10.1109/IPFA.2017.8060144.

[11] R. D'Esposito *et al.*, "Influence of the BEOL metallization design on the overall performances of SiGe HBTs," in *Proc. 13th IEEE Int. Conf. Solid-State Integr. Circuit Technol. (ICSICT)*, Hangzhou, China, 2016, pp. 358–360, doi: 10.1109/ICSICT.2016.7998920.

[12] L. Kljucar *et al.*, "Impact of via density on the mechanical integrity of advanced back-end-of-line during packaging," in *Proc. IEEE 66th Electron. Compon. Technol. Conf. (ECTC)*, Las Vegas, NV, USA, 2016, pp. 1778–1785, doi: 10.1109/ECTC.2016.100.

[13] B.-Y. Tsui, S.-S. Lin, C.-S. Tsai, and C.-C. Hsia, "Plasma charging damage during contact hole etch in high-density plasma etcher," *Microelectron. Rel.*, vol. 40, no. 12, pp. 2039–2046, 2000.

[14] Y.-P. Tsai, C.-H. Wu, C.-J. Lin, and Y.-C. King, "Wafer-level mapping of plasma-induced charging effect by on-chip in situ recorders in FinFET technologies," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2497–2502, Jun. 2016, doi: 10.1109/TED.2016.2552231.

[15] Y.-P. Tsai, T.-H. Hsieh, C. J. Lin, and Y.-C. King, "Charge splitting in situ recorder (CSIR) for real-time examination of plasma charging effect in FinFET BEOL processes," *Nanoscale Res. Lett.*, vol. 12, no. 1, p. 534, Sep. 2017, doi: 10.1186/s11671-017-2309-0.

[16] D. C. Edelstein, "20 Years of Cu BEOL in manufacturing, and its future prospects," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2017, pp. 14.1.1–14.1.4, doi: 10.1109/IEDM.2017.8268387.

[17] P. C. Andricacos, C. Uzoh, J. O. Dukovic, J. Horkans, and H. Deligianni, "Damascene copper electroplating for chip interconnections," *IBM J. Res. Dev.*, vol. 42, no. 5, pp. 567–574, Sep. 1998, doi: 10.1147/rd.425.0567.

[18] K. Ueno *et al.*, "A high reliability copper dual-damascene interconnection with direct-contact via structure," in *Int. Electron Devices Meeting Tech. Dig. (IEDM)*, San Francisco, CA, USA, 2000, pp. 265–268, doi: 10.1109/IEDM.2000.904307.

[19] I. Qin *et al.*, "Advances in wire bonding technology for 3D die stacking and fan out wafer level package," in *Proc. IEEE 67th Electron. Compon. Technol. Conf. (ECTC)*, Orlando, FL, USA, 2017, pp. 1309–1315, doi: 10.1109/ECTC.2017.134.

[20] A. Basavalingappa and J. R. Lloyd, "Effect of microstructure and anisotropy of copper on reliability in nanoscale interconnects," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 1, pp. 69–79, Mar. 2017, doi: 10.1109/TDMR.2017.2655459.

[21] N. C. Wang *et al.*, "Replacing copper interconnects with graphene at a 7-nm node," in *Proc. IEEE Int. Interconnect Technol. Conf. (IITC)*, Hsinchu, Taiwan, 2017, pp. 1–3, doi: 10.1109/IITC-AMC.2017.7968949.

[22] P. G. Borden, J. P. Li, S. R. Smith, A. C. Diebold, and W. W. Chism, "Line and via voiding measurements in damascene copper lines using metal illumination," *IEEE Trans. Semicond. Manuf.*, vol. 16, no. 3, pp. 409–416, Aug. 2003, doi: 10.1109/TSM.2003.815633.

[23] M. H. Tsai, W. J. Tsai, S. L. Shue, C. H. Yu, and M. S. Liang, "Reliability of dual damascene Cu metallization," in *Proc. IEEE Int. Interconnect Technol. Conf.*, Burlingame, CA, USA, 2000, pp. 214–216, doi: 10.1109/IITC.2000.854329.

[24] G. Aggarwal, D. Henke, S. Takedai, R. Anantatmukala, and B. Huber, "Dual lobe shading of surface copper voids in copper metal lines: YE: Yield enhancement/learning," in *Proc. 28th Annu. SEMI Adv. Semicond. Manuf. Conf. (ASMC)*, Saratoga Springs, NY, USA, 2017, pp. 8–9, doi: 10.1109/ASMC.2017.7969188.

[25] B. Imbert, P. Gondcharton, L. Benaissa, F. Fournel, and M. Verdier, "Wafer level metallic bonding: Voiding mechanisms in copper layers," in *Proc. IEEE Int. Interconnect Technol. Conf. IEEE Mater. Adv. Metallization Conf. (IITC/MAM)*, Grenoble, France, 2015, pp. 201–204, doi: 10.1109/IITC-MAM.2015.7325619.

[26] A. Sakata *et al.*, "Copper line resistance control and reliability improvement by surface nitridation of Ti barrier metal," in *Proc. Int. Interconnect Technol. Conf.*, Burlingame, CA, USA, 2008, pp. 165–167, doi: 10.1109/IITC.2008.4546956.

[27] T.-K. Kang and W.-Y. Chou, "Avoiding Cu hillocks during the plasma process," *J. Electrochem. Soc.*, vol. 151, no. 6, pp. 391–395, 2004, doi: 10.1149/1.1740784.

[28] Z. Wang, "Detection of and protection against plasma charging damage in modern IC technologies," Ph.D. dissertation, Elect. Eng., Math. Comput. Sci., Univ. Twente, Enschede, The Netherlands, 2004.

[29] S.-H. Park *et al.*, "Dependence of plasma process induced damage on the transistor gate area," in *Proc. 6th Int. Symp. Plasma Process Induced Damage*, Monterey, CA, USA, 2001, pp. 124–127, doi: 10.1109/PPID.2001.929994.

[30] T. C. Wang, Y. L. Wang, T. E. Hsieh, S. C. Chang, and Y. L. Cheng, "Copper voids improvement for the copper dual damascene interconnection process," *J. Phys. Chem. Solids*, vol. 69, pp. 566–571, Feb./Mar. 2008.

[31] K.-W. Chen *et al.*, "Tungsten corrosion and recess improvement by feasible slurry and clean chemical in WCMP process," in *Proc. IEEE Int. Interconnect Technol. Conf. (IITC)*, Hsinchu, Taiwan, 2017, pp. 1–3, doi: 10.1109/IITC-AMC.2017.7968980.

[32] C. H. Lee and R. K. Shiue, "Mechanism and improvements of Cu voids under via bottom," *Dept. Mater. Sci. Eng. NTU Taipei ROC Solid State Technol.*, vol. 61, no. 2, pp. 12–17, Mar. 2018.

[33] D. Wang *et al.*, "Early failure model analysis and improvement of the upstream electromigration in 45nm Cu low-k interconnects," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Anaheim, CA, USA, 2013, pp. EM.1.1–EM.1.3, doi: 10.1109/IRPS.2013.6532076.

[34] S. A. Sheikholeslam, C. Grecu, and A. Ivanov, "Using magnetic controlled electromigration for electrod fabrication," in *Proc. 14th IEEE Int. Conf. Nanotechnol.*, Toronto, ON, USA, 2014, pp. 839–842, doi: 10.1109/NANO.2014.6968138.

[35] T. C. Lin *et al.*, "The failure mode of Bi and Ni-doped Sn-Ag-Cu solder joint under electromigration tests," in *Proc. Int. Conf. Electron. Packag. iMAPS Asia Conf. (ICEP-IAAC)*, 2018, pp. 226–229, doi: 10.23919/ICEP.2018.8374708.

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