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InGaAs Capacitor-Less DRAM Cells TCAD Demonstration

CARLOS NAVARRO [1], SANTIAGO NAVARRO [1], CARLOS MARQUEZ [1], LUCA DONETTI [1], CARLOS SAMPEDRO [1], SIEGFRIED KARG [2], H. RIEL [2], AND FRANCISCO GAMIZ [1]

1 Computer Electronics and Technology Department, University of Granada, 18071 Granada, Spain
2 Science and Technology Department, IBM Research – Zurich, 8803 Rüschlikon, Switzerland

CORRESPONDING AUTHOR: CARLOS NAVARRO (e-mail: carlosnm@ugr.es)

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ABSTRACT 2D numerical TCAD simulations are used to infer the behavior of III-V capacitor-less dynamic RAM (DRAM) cells. In particular, indium gallium arsenide on insulator technology is selected to verify the viability of III-V meta-stable-dip RAM cells. The cell performance dependence on several parameters (such as the back-gate voltage, semiconductor thickness, indium/gallium mole fraction or interface traps) and simulation models (like ballisticity or spatial quantum confinement) is analyzed and commented. Functional cells are presented and compared with analogous silicon 1T-DRAM memories to highlight the advantages and drawbacks.

INDEX TERMS 1T-DRAM, III-V, capacitor-less, DRAM, fully depleted, InGaAs, MSDRAM, SOI.

I. INTRODUCTION

Nowadays, the Dynamic RAM (DRAM) industry is approaching fundamental limitations since the DRAM capacitor scaling is becoming extremely complex in 2D architectures. The migration from $6F^2$ to $4F^2$ cells is very challenging and new DRAM concepts or 3D cell stacking are currently being explored [1]. Basic dynamic cell requirements include at least low-cost, low-power and fast operation. Several SOI (Silicon-On-Insulator) capacitor-less cells, getting rid of the capacitor integration, have been proposed in the present and last decades [2]–[4], each of them featuring its own advantages. Among this breed of memory cells, the MSDRAM (Meta-Stable-Dip RAM) [5] stands out due to its simplicity of operation and cheaper manufacturing process where only a standard silicon fully-depleted (FD) SOI transistor is required. Nonetheless, capacitor-less memory cells using III-V materials have not been thoroughly studied yet. Previous works on III-V 1T-DRAM cells have been mainly focused on simulations [6]–[8] or on co-integrating source and drain (S/D) gallium phosphide (GaP) side terminals on silicon body transistors [9] to enhance the floating body effect (FBE) [10], hence the DRAM performance.

In this work, III-V n-type transistors are built using 2D TCAD simulations in Synopsys [11] and their operation as MSDRAM memory cell is demonstrated and compared with analogous silicon cells. In order to test if III-V single-transistor DRAM cells are feasible, indium gallium arsenide (InGaAs) is selected as semiconductor due to the increasing interest of implementing this material with CMOS logic [12], [13]. Concretely, InGaAs features extremely high electron mobility [14] motivating its application for ultra-fast and low-power electronics [15].

II. CAPACITOR-LESS DRAM CELLS PRINCIPLES

The original concept of capacitor-less DRAM cell was first experimentally demonstrated in [16] by using the intrinsic floating body effect [10] of partially-depleted (PD) SOI devices. The charge, defining the logic ‘0’ or ‘1’-state, is stored in the body of the transistor, modulating its conductance and avoiding the need of an external capacitor. Instead of sensing the bitline voltage (increase/drop due to the discharge/charge of the storage capacitor) as in common DRAM memories, the logic state discrimination in 1T-DRAM cells is based on reading the current through the cell: charged bodies typically enhance the current flow by reducing the threshold voltage while discharged bodies do the opposite. These operation principles generally apply to most capacitor-less cells [2], [3] with few exceptions [17]–[19].

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TABLE 1. Default MSDRAM biasing conditions for each memory operation. Normally V_{BG} > 0.0 V and V_S = 0.0 V.

Memory Operation	Drain Voltage (V)	Front-Gate Voltage (V)
Hold (H)	0.0	-1.0
Read (R)	0.2	-1.0
Program '0'-State (W_0)	0.0	1.5
Program '1'-State (W_1)	1.0	-2.0

Regarding the MSDRAM [5], the memory operation is based on inter-gate coupling [20] and non-equilibrium state [21]. The back-gate terminal, acting as ground-plane (GP), is constantly biased to positive values, typically over threshold, $V_{BG} > 0$ V, to obtain a virtual n-type back channel. Likewise, the front-gate voltage is generally (but not always) negative, $V_{FG} < 0$ V, to induce a potential well below the top-gate oxide. This mechanism mimics the inherent FBE of PD-SOI devices in fully depleted cells: subsisting holes within the body are collected and modify the cell inner electrostatics. By modulating the hole density, distinct vertical electric fields are achieved originating a change in the back electron-channel regime via coupling. Different conductance values are thus obtained defining the logic '1'- and '0'-states. The '1'-state programming, W_1, is carried out by injecting holes typically through impact ionization or, more likely to prevent reliability issues [22], by band-to-band tunneling at the drain edge ($V_{FG} < 0$ V and $V_{DS} > 0$ V). On the other hand, the logic '0'-state is stored, W_0, evacuating holes via top-gate capacitive coupling ($V_{FG} \geq 0$ V with $V_D \leq 0$ V and $V_S = 0$ V). The cell reading, R, is achieved by simply sensing the drain current ($V_{DS} > 0$ V): high (low) current values imply a large (low) hole population corresponding to the '1' ('0') state. Finally, on holding, H, the cell current is blocked while available holes are preserved underneath the top gate ($V_{FG} < 0$ V and $V_{DS} = 0$ V) for as long as possible in order to enhance the retention time. The non-steady '0'-state is gradually lost due to thermal generation and carrier leakage: mainly tunneling (either direct gate or band-to-band tunneling) and junction leakage. Typical biasing conditions are summarized in Table 1.

III. SIMULATION FRAMEWORK

A 2D n-type FD-SOI transistor built in Synopsys tool [11] is used as basic MSDRAM memory cell structure. A homogeneously beryllium low p-type doped InGaAs film is employed as active layer. The semiconductor lies on-top of a silicon dioxide buried sheet with a p-type ground plane as back-gate terminal underneath. The simplified gate stack, horizontally isolated with wide Si_3N_4 lateral spacers, is made of a thick high-k dielectric with a metal featuring close to mid-gap metal work-function above. The high-k layer thickness guarantees negligible gate tunneling while providing good electrostatics. The lateral regions are raised and implanted with n-type silicon (where the concentration is limited as in [23]) to induce the S/D side terminals. The resultant structure and its corresponding net doping profile are illustrated in Fig. 1. A very

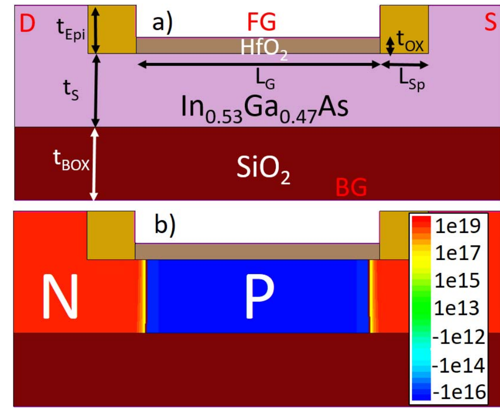


FIGURE 1. a) Default InGaAs-OI MSDRAM cell with its b) net doping profile. L_G = 100 nm and t_S = 30 nm. Other parameters match those found in Table 2. The ground plane is simulated as a metal contact directly below the BOX with a workfunction matching p-type 10^{18} cm^{-3} doped silicon as if it were a ground-plane.

TABLE 2. Memory cell physical parameters.

Parameter	Symbol	InGaAs Cell	Silicon Cell	Unit
HfO_2 Oxide thickness	t_{OX}	7	7	nm
Body thickness	t_S	10-50	30	nm
SiO_2 BOX thickness	t_{BOX}	30	30	nm
Si_3N_4 Gate spacer	L_{Sp}	20	20	nm
S/D Epitaxy thickness	t_{Epi}	20	20	nm
Gate Length	L_G	60-200	100	nm
Width	W	1	1	μm
Body Doping (p)	N_B	10^{16}	10^{16}	cm^{-3}
Source (S) Doping (n)	N_S	10^{19}	10^{21}	cm^{-3}
Drain (D) Doping (n)	N_D	10^{19}	10^{21}	cm^{-3}
Si GP Doping (p)	N_{GP}	10^{18}	10^{18}	cm^{-3}
FG work-function	Φ_{FG}	4.95	4.7	eV

similar silicon cell is used for the aim of comparison. The main difference resides in the doping profile and its species, using boron (p-type) and arsenic (n-type). The essential physical parameters are summarized in Table 2 for both cells.

The employed default semiconductor mole fraction corresponds to $In_{0.53}Ga_{0.47}As$, one of the most commonly studied compounds [12], [13], [15], [23]. Material parameters such as energy band-gap, intrinsic carrier concentration or dielectric constants agree with those found in [24]. Parameters and electrical simulation models include: room temperature (300 K), Fermi statistics, band-to-band tunneling generation and SRH (Shockley-Read-Hall), Auger and radiative recombination processes (only SRH in silicon). Regarding the mobility models, high-field saturation, doping dependence and normal field contributions are considered. The channel length-modulation model to account for ballistic mobility (with Fermi correction) [25], [26] is included when indicated. The ballistic length, L_{ch}, was chosen to match each device gate length, L_G. Density gradient quantization model [11], [27], [28] in the InGaAs film was also considered for thin films ($t_S \leq 20$ nm) to account for spatial confinement. Default double-gate 10/20 nm <100> InGaAs parameter sets were employed.

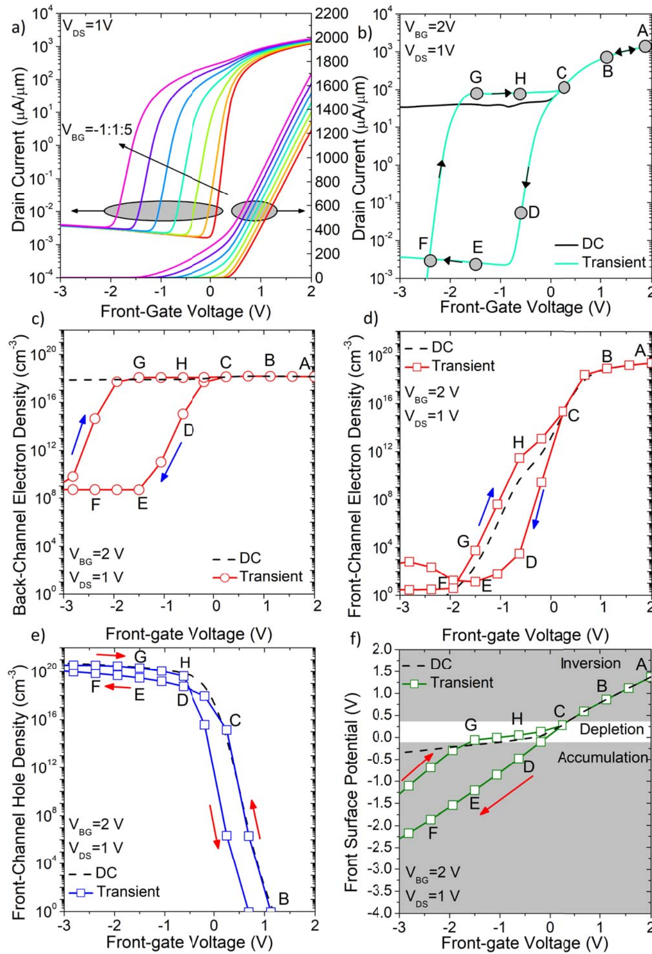


FIGURE 2. a) Reverse anode voltage sweeps as a function of the back-gate bias for the InGaAs cell. b) Detail of the hysteresis cycle (reverse and forward senses) and comparison with the DC curve for $V_{BG} = 2$ V. Corresponding vertical electron c) back and d) front densities. Front e) hole population and f) surface potential. All densities and potentials are extracted at mid channel and 0.1 nm away from the interfaces. Transient sweeps last 1 μs for each sense. $L_G = 100$ nm and $t_S = 30$ nm. $V_{DS} = 1$ V.

IV. III-V MSDRAM CELL

A. HYSTERESIS MEMORY CYCLE

Figure 2a depicts the reverse $I_D(V_{FG})$ sweeps for several back-gate voltages to observe the transistor switching characteristics. The typical threshold voltage coupling dependence according to V_{BG} is found: increasing the back-gate voltage shifts the current onset to lower V_{FG} [20]. A hysteresis cycle, as in [5], is observed at negative V_{FG} enabling the memory operation, Fig. 2b. Notice, by comparing with the DC $I_D(V_{FG})$ sweep, that the hysteresis cycle arises as a consequence of the cell being out of its steady-state. This hysteresis can be explained as follows: at high front-gate voltages, points A and B, the strong electron volume inversion [29] (Fig. 2c and d) impedes the presence of many holes in the body (Fig. 2e). As V_{FG} is reduced towards negative values, the front-channel electron population is reduced and the channel leaves inversion limiting the drain current, point C. Up to this point the cell is in steady-state since the DC and transient curves coincided. From this point, the cell enters in non-equilibrium regime [21] when further reducing V_{FG}. The DC front hole accumulation layer (Fig. 2e) cannot be instantly achieved due to three reasons: i) there is no available reservoir (p^+ region nearby) to supply holes; ii) the p^- body is depleted from free carriers and iii) its volume is limited to rapidly obtain the carriers via thermal generation. This means the required holes to recover the steady-state need to be injected by band-to-band (BtB) tunneling at the drain edge. The reduced hole population in non-equilibrium results in a body potential decrease with respect to DC, Fig. 2f. This electrostatic potential drop gradually cuts, via inter-gate coupling [20], the back-channel inversion reducing even more the current, point D. At a given V_{FG}, the top-gate induced vertical field, not sufficiently screened by the front-hole accumulation channel, completely depletes the back interface from electrons as well, point E, and then the current reaches its minimum. As time passes and V_{FG} goes more negative, holes are gradually introduced in the body (both via thermal generation and band-to-band tunneling) and the front-channel hole density increases toward its equilibrium concentration, point F. Once the hole population is recovered, the body potential increases allowing once again the back channel inversion, i.e. the first current onset before point G. A further increase of the top-gate voltage allows the recovery of a high electron concentration also at the front interface, point H, which finally results in the second current onset corresponding to the front interface inversion, point C. In summary, the lack of holes at the front-interface yields a potential drop that, through coupling, limits the back-channel inversion and the current flow. Once the hole density increases, the back-channel electron population rises and the current is recovered.

B. TRANSIENT OPERATION

A generic W_0-R-W_1-R-W_0-R memory sequence is employed to test the basic DRAM operation for the default cell in Fig. 1. The employed bias pattern is shown in Fig. 3a. The resultant drain current readout, Fig. 3b, successfully demonstrates the valid memory operation: after any W_0 operation, the driven current remains much lower than after W_1. The '1'-state current can be easily enhanced by increasing the drain bias while reading (the '0'-state and current ratio and margin would be degraded though). Figure 3c proves the MSDRAM operation detailed in last section. It represents the InGaAs body electron and hole densities after the first W_1 and last W_0, respectively. After collecting holes generated by band-to-band tunneling at the front interface during W_1, the electron back-channel population is reinforced enabling a larger current readout when sensing afterward. On the other hand, following a W_0, the hole density is limited underneath the top dielectric. The resultant body is deeply out of equilibrium and allows a strong vertical field to deplete the back-channel from electrons. The low electron density yields a drastic drop in the conductance and thus in the drain current.

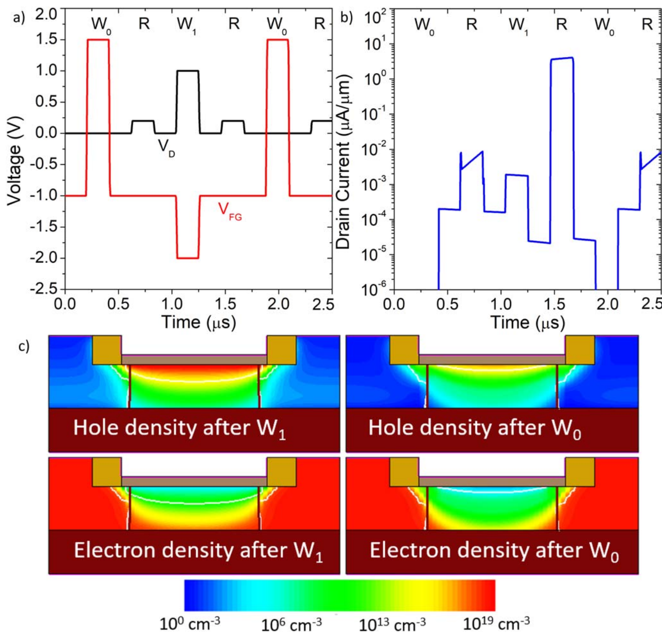


FIGURE 3. a) Transient bias pattern composed of a W_0-R-W_1-R-W_0-R sequence and b) resultant current readout demonstrating the memory operation. c) Hole and electron densities after programming operations, W_1 and W_0 at $t = 1.26$ μs and $t = 2.10$ μs, respectively. Pulses feature 200 ns width and 10 ns rising/falling times. $V_{BG} = 3$ V and $V_S = 0$ V. Same structure as Fig. 1.

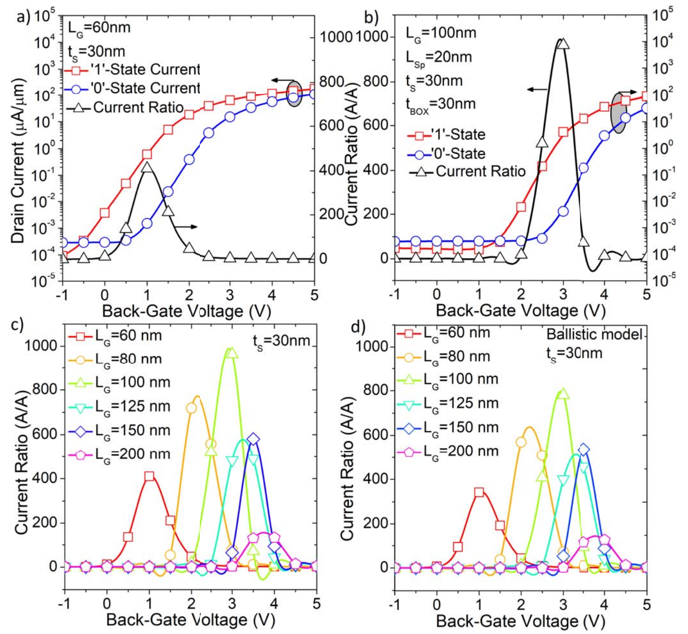


FIGURE 4. Logic current levels ('1' and '0' obtained at $t = 1.6$ μs and $t = 2.4$ μs, respectively) and current ratio as a function of the back-gate voltage for a) $L_G = 60$ nm and b) $L_G = 100$ nm. Current ratios as a function of the back-gate voltage for distinct channel length ranging from 60 nm to 200 nm c) without or d) with the ballistic model included.

In the following subsections, the cell is analyzed as a function of different parameters.

B.1. BACK-GATE VOLTAGE AND GATE LENGTH

These two metrics are closely related to each other. The optimum back-gate voltage to enhance the memory performance, i.e., current ratio between logic levels, strongly depends on the length due to the short-channel effects (SCE). Figures 4a,b show the logic current levels and their ratio for different back-gate voltages at distinct gate lengths. Observe that the current ratio peaks at different V_{BG} according to the length: it moves to higher V_{BG} when increasing the S/D distance. As the gate length is downscaled, SCE gradually facilitates the back-interface inversion reducing the need of a high ground-plane bias. For example, at $L_G = 100$ nm the back-interface remains depleted up to 1.5 V when the back-channel arises. However, for $L_G = 60$ nm the channel appears even for a grounded ground plane. The current ratio comparison, accounting for all analyzed gate lengths and further demonstrating the peak shift, is illustrated in Fig. 4c. Notice that the peak displacement to larger ground plane biases for longer gate channels is gradually reduced denoting the mitigation of SCE. A similar scenario including the ballistic mobility model [26] is represented in Fig. 4d. A degradation that ranges between 5-20% is observed when including the ballistic mobility due to the limited time to accelerate electrons from the source to the drain. As a result the effective mobility drops and the current during the '1'-state becomes smaller (the '0'-state is barely affected when the current is very small) which yields the reduction in the current ratio. Nevertheless, the memory operation is still possible.

Although state-of-the-art buried oxides can sustain very large voltages [30], in order to prevent any reliability concern the back-gate voltage is limited to +5 V where usual operating voltages are even lower.

B.2. SEMICONDUCTOR FILM THICKNESS

Another important tradeoff is observed with the semiconductor channel thickness. Reducing the InGaAs film enhances the inter-gate coupling and benefits the memory effect. Figure 5 shows that the current ratio increases for thinner films. However, this mechanism cannot be sustained in ultra-thin films where the supercoupling effect takes place, as observed in other semiconductors such as silicon [31], [32]. This effect impedes the presence of an electron inversion film facing a hole accumulation layer when the semiconductor is too thin, preventing the FBE single transistor DRAM operation. For InGaAs, the critical thickness seems to be, as in silicon, around 10 nm. Due to SCE, the supercoupling phenomenon arises earlier for shorter cells [33], as can be inferred from the comparison between $L_G = 60$ nm and $L_G = 100$ nm in Fig. 5a,b where all the peaks are again displaced to lower V_{BG}.

Insets in Fig. 5a,b illustrate the current ratio when accounting for quantum mechanics corrections in the charge density distribution (exclusively for $t_S = 10$ nm and $t_S = 20$ nm). Fig. 5c,d shows the vertical charge profiles at mid-channel for electrons and holes after W_0 and W_1. Notice that, when

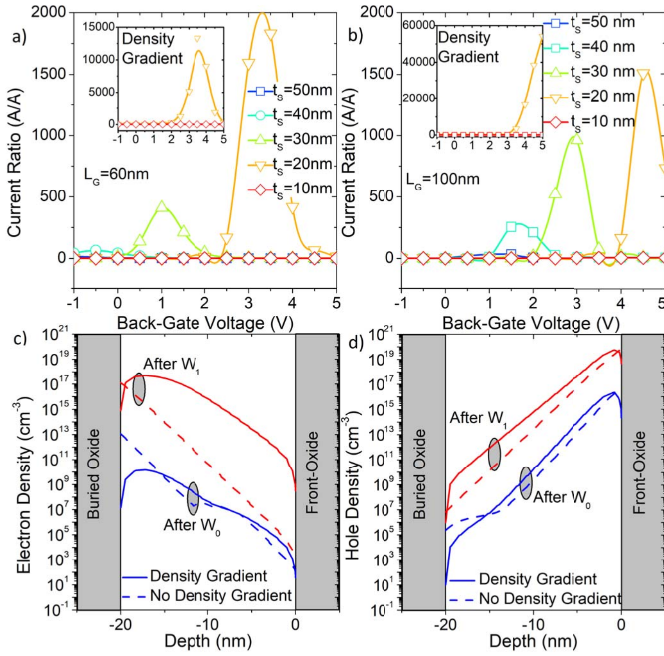


FIGURE 5. Current ratio as a function of the ground-plane bias for several channel thicknesses at a) $L_G = 60$ nm and b) $L_G = 100$ nm. Insets show the results for $t_S = 10$ nm and $t_S = 20$ nm when accounting for density gradient models (default parameters for InGaAs in double gate configuration for the corresponding body thickness). Vertical c) electron and d) hole density profiles at mid-channel after programming both logic states with and without quantum confinement ($L_G = 100$ nm, $t_S = 20$ nm and $V_{BG} = 4.5$ V).

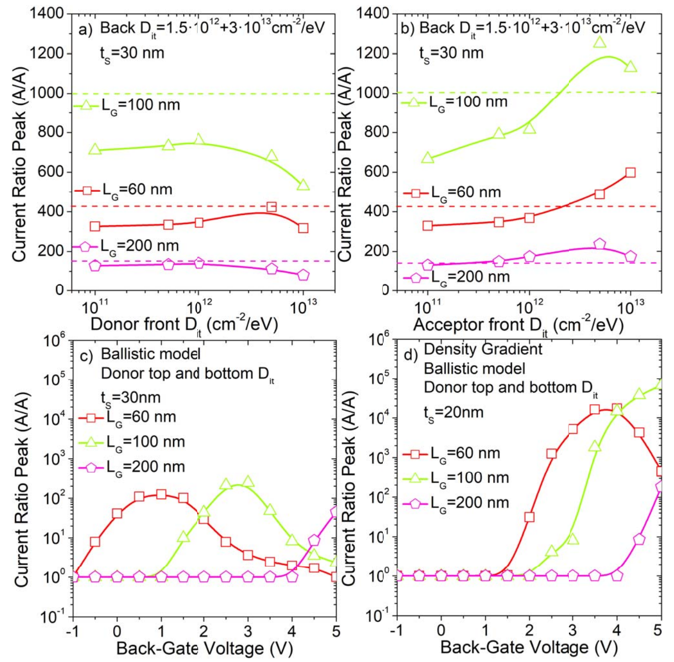


FIGURE 6. Current ratio peak (between $V_{BG} = -1$ V and $V_{BG} = +5$ V) for different a) donor and b) acceptor uniform front D_{it} concentrations. Dashed lines represent the current ratio peak without any D_{it}. Current ratio against V_{BG} with several models activated simultaneously for c) $t_S = 30$ nm and d) $t_S = 20$ nm. The back donor D_{it} as in [34] is always present.

spatial confinement is active, the charge profile peaks appear separated from the interface as if the semiconductor film was thinner. This effective thinning of the film induces a slight shift of the current ratio peak to higher V_{BG} (approximately 0.5 V) as occurs without quantum mechanics. Moreover, the current ratio peaks become much larger due to several reasons: i) coupling increase between interfaces; ii) reduced surface scattering and, especially, iii) notably larger electron density after the '1'-state programming (the '0'-state remains essentially the same). All these contributions enhance the '1'-state current by one order of magnitude leading to the current ratio increase. Finally, it is worth mentioning that the default InGaAs quantization parameters, available exclusively for double-gate and bulk device configurations with 10 or 20 nm film thickness, might not be convenient in this structure (neither bulk or symmetric double gate) yielding an overestimation of the memory performance.

B.3. INTERFACE DENSITY OF STATES

Interface density of states have been considered both at the top (InGaAs/front oxide) and bottom (InGaAs/BOX) semiconductor surfaces to analyze the impact on the memory operation affected by the electrostatic change. The assumed back-interface density of states is similar to that found for Al_2O_3 [34]. It comprises a donor uniform distribution of 1.5×10^{12} cm^{-2}/eV and a donor Gaussian distribution close to the valence band of 3×10^{13} cm^{-2}/eV. At the top interface an uniformly distributed density of states along the energy bandgap, with variable concentration, is considered. No trap-assisted tunneling or any other generation/recombination mechanism, such as surface recombination, is enabled. Figure 6 shows the current ratio for several a) donor and b) acceptor D_{it} concentrations. Besides the influence on the subthreshold swing characteristics [10] (not shown), D_{it} does not seem to extremely degrade the memory characteristics. Depending on the traps nature, the current ratio can be even improved reflecting a beneficial effect in the electrostatic control. Acceptor distributions (negatively charged when occupied) at the front interface contribute to storing holes underneath the gate dielectric, therefore enhancing the memory effect. On the other hand, donor densities (positively charged when fully occupied) counterbalance the negative V_{FG} degrading the FBE. It is worth noting that even for a reduced front D_{it}, the current ratio drops with respect to the default scenario (dashed lines in Fig. 6a,b) because of the donor back-interface density, which is constantly present and reduces the vertical back-gate-induced electric field. As a final remark, since trap distributions are stochastic, the main challenge D_{it} introduces, even for the best acceptor scenario, is the variability from device to device.

Figures 6c,d illustrate the current ratio when accounting for several models simultaneously. Spatial quantization has not been considered for $t_S = 30$ nm since no default InGaAs parameters are available for such thickness. The current ratio strongly depends on quantum mechanics as previously

TABLE 3. III-V cell current ratio peak summary, I_1/I_0 [A/A].

t_S (nm)	L_G (nm)	Default models	Ballistic model	Quantum Mechanics	Donor D_{it}	All Combined
20	60	1830	1784	13500	1943	17078
	100	1504	1343	54000	1110	65876
	200	62	58	1103	41	45
30	60	410	342	Not applied	414	124
	100	964	781		678	245
	200	133	128		112	55

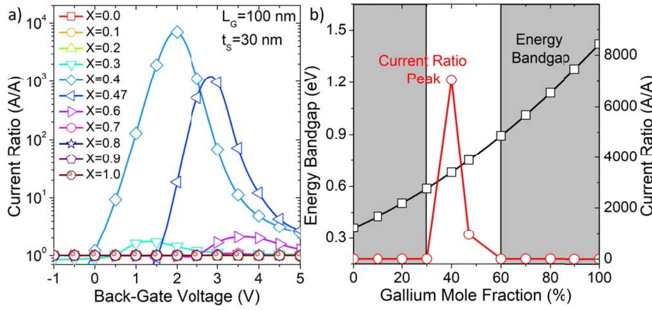


FIGURE 7. a) Current ratio as a function of the back-gate voltage for different $In_{1-x}Ga_xAs$ gallium mole fractions. b) InGaAs energy bandgap [24] and peak current ratio (for any V_{BG}) as a function of the gallium mole fraction.

observed in Fig. 5a,b and confirmed in Table 3. This table summarizes the current ratio peak dependence on the different models considered for several cell geometries (length and semiconductor thickness). The peak ratio is extracted from the range $-1 \leq V_{BG} \leq 5$ V. In all cases, the D_{it} presence accounts for the default back-interface state density as in [34] whereas the front-interface features an uniform donor (worst case) 5×10^{12} cm^{-2}/eV distribution. Ballistic and D_{it} distributions slightly degrade the performance whereas density gradient strongly benefits the ratio.

B.4. MOLE FRACTION IMPACT

Different mole fractions are tested attending to the $In_{1-x}Ga_xAs$ relation. From InAs ($x = 0$ %) to GaAs ($x = 100$ %), the MSDRAM operation for distinct indium/gallium ratios, following parameters in [24], is verified. The default structure mimics the one in Fig. 1a. Figure 7 shows the current ratio as a function of V_{BG}. Notice that only few mole fractions enable the memory operation where a value close to $x = 40$ % seems to be the optimum approach (for the considered parameters and cell architecture). The current ratio peak (for any back-gate bias) and the energy band-gap are depicted in Fig. 7b. It is worth observing that memory capabilities disappear for very low/high bandgaps. If E_G is reduced, parasitic injection of holes via BtB tunneling occurs while storing the logic '0'. As a result, the current after any programming operation is high (as for the '1'-state) and the current ratio drops. Likewise, if the bandgap is too large, the BtB tunneling becomes inefficient and the current during the '1'-state resembles a logic '0' and thus the current ratio tends to 1 as well. Other biasing conditions and/or architectures (different channel thickness, doping profiles or spacers for example) might exhibit functional memory operations.

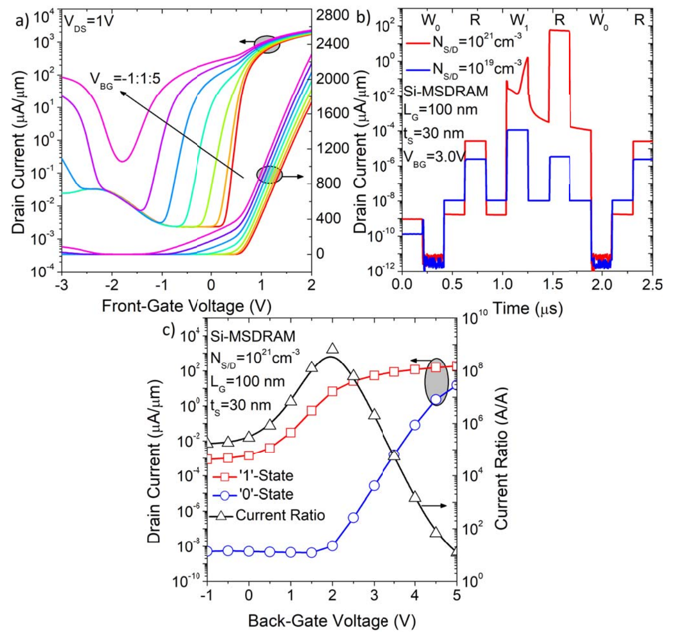


FIGURE 8. a) Reverse anode voltage sweeps as a function of the back-gate bias for the Si cell. The transient ramping (falling or rising) times are fixed to 1 μs. b) Transient current readout to test the memory operation with a W_0-R-W_1-R-W_0-R sequence (identical bias pattern as in Fig. 3a) and c) logic levels and current ratio for several GP biases.

The optimum InGaAs cell found, featuring the largest current ratio, corresponds to $In_{0.6}Ga_{0.4}As$ with $L_G = 100$ nm and $t_S = 30$ nm (other lengths and thicknesses have not been tested) at $V_{BG} = 2$ V, Fig. 7.

V. SILICON MSDRAM COMPARISON

For the aim of benchmarking, a similar FD-SOI silicon transistor is build in Synopsys. The corresponding architecture is totally analogous and features the parameters in Table 2 unless explicitly stated.

A. SILICON MSDRAM CELL

$I_D(V_{FG})$ switching and transient characteristics are depicted in Fig. 8 for analogous silicon cells. They replicate the same biasing conditions as for the InGaAs cell previously presented in Fig. 2 (switching curves) and 3 (transient operation). Fig. 8a shows the transient reverse drain current sweeps as a function of the front-gate voltage. A significant difference, at very low front-gate voltages, is observed with respect to Fig. 2a for InGaAs. The drain current rises earlier in silicon due to the enhanced BtB hole generation as will be discussed later. Figure 8b,c represent the Si cell memory operation (same biasing as in Fig. 3a) and the current levels and ratios as a function of V_{BG}. Results demonstrate that the silicon MSDRAM outperforms the InGaAs cell in terms of current ratio: at same biasing, $V_{BG} = 3$ V, the silicon cell current ratio ($\simeq 2 \times 10^6$ A/A) exceeds the InGaAs ($\simeq 10^3$ A/A) in about 3 orders of magnitude.

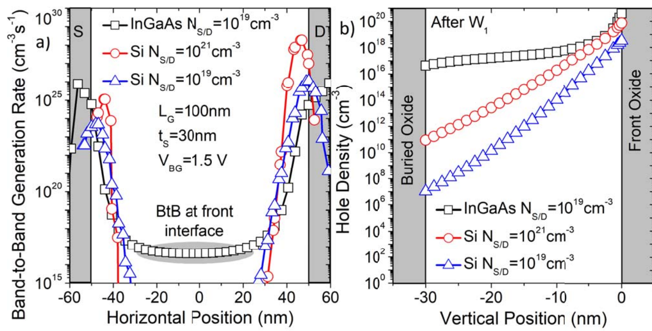


FIGURE 9. a) Front-interface band-to-band tunneling generation rate per second for the different MSDRAM cells during W_1 (at $t = 1.20$ μs for the pattern in Fig. 3a) and corresponding b) vertical hole density at mid channel after W_1 (at $t = 1.26$ μs).

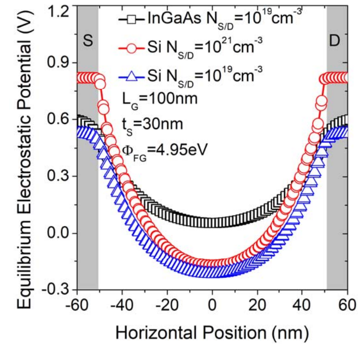


FIGURE 10. Electrostatic potential well at equilibrium (all device terminals are short-circuited) for the InGaAs and silicon cells at mid channel (y=$t_S/2$). For a fair comparison, all devices feature the same front-gate workfunction, $\Phi_{FG} = 4.95$ eV. $L_{Sp} = 20$ nm and $t_{BOX} = 30$ nm.

B. BAND-TO-BAND TUNNELING GENERATION

The main MSDRAM hole injection mechanism is based on gate-induced drain leakage (GIDL). It enables holes to tunnel from the conduction band to the valence band and gather in the body thanks to the strong electric field at the drain edge ($V_{FG} < 0$ V and $V_D > 0$ V). Due to the lower InGaAs energy bandgap compared to Si, approximately 0.74 eV against 1.12 eV (room temperature), the band-to-band tunneling generation rate is expected to be more effective (at equivalent conditions). This fact could be employed to reduce the programming voltage and thus the power consumption. Figure 9a shows the band-to-band generation rate along the front-interface (0.1 nm away from the top insulator) during W_1 for the InGaAs and Si memory cells. It is worth noticing that, in order to be fair, a silicon cell featuring lower S/D doping, 10^{19} cm^{-3}, as in the InGaAs cell has been also considered. It can be observed that the generation rate is larger in InGaAs than in silicon when the cells feature the same source/drain doping concentration. Specifically, by integrating the BtB generation throughout the whole 2D structure at $t = 1.2$ μs (middle of the W_1 operation pulse), it turns out that InGaAs is more than 27 times the BtB generation in silicon (at same doping, $N_{S/D} = 10^{19}$ cm^{-3}) and about 22% for the silicon default doping $N_{S/D} = 10^{21}$ cm^{-3}. This extreme difference implies that the Si cell with lower doping is not able to adequately repopulate the body with holes after W_1, Fig. 9b, and the memory operation fails, Fig. 8b. As a negative point, the InGaAs BtB generation slightly occurs not only at the drain edge but along the front-interface as well and, more importantly, also during the hold operation (not shown). This means that the logic '0'-state retention time would be degraded faster than in silicon.

Another important difference with respect to silicon is the direct bandgap (regardless the considered mole fraction): the generation of electron-hole pairs is more effective. This fact is expected to negatively impact on the cell retention time. The '0'-state would be compromised earlier limiting the performance.

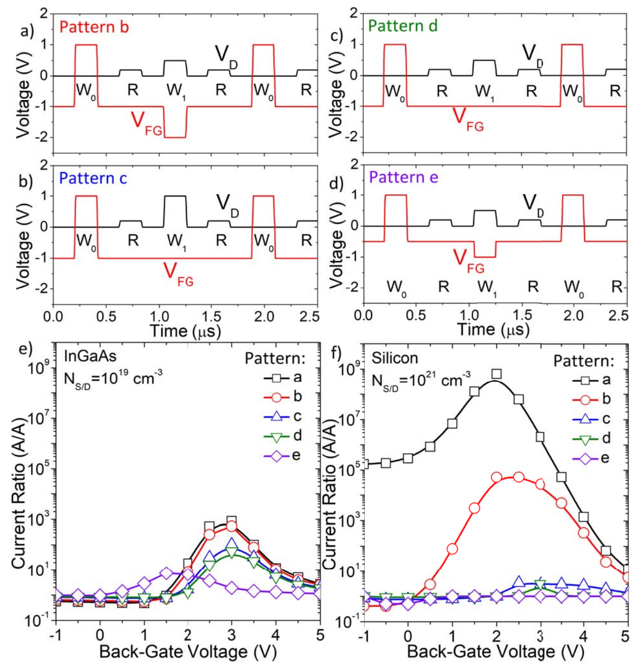


FIGURE 11. a-d) Different bias patterns to test the low voltage MSDRAM memory operation in Si and InGaAs cells (pattern a corresponds to Fig. 3a). Current ratio results for e) InGaAs and f) Si cells with default S/D doping concentrations. At low voltages, InGaAs cells present larger memory performance. $L_G = 100$ nm and $t_S = 30$ nm, other parameters match those from table 2.

C. FRONT-GATE INDUCED POTENTIAL WELL

The front-interface horizontal electrostatic potential cut at equilibrium, with all terminals short-circuited, is depicted in Fig. 10 for similar InGaAs and Si memory cells. It can be observed that, when the S/D regions are less doped, the potential profiles are smoother due to the extended space charge region. The lower S/D doping and, especially, the larger III-V intrinsic carrier density, $n_{i,In_{0.53}Ga_{0.47}As} \simeq 6.3 \times 10^{11}$ cm^{-3} at room temperature [24], combine and yield reduced potential wells for the InGaAs cells with respect to silicon. This means the floating body effect is less intense in InGaAs cells: they are less effective storing holes which

hardens the memory operation with respect to traditional silicon memories. This result partly motivates the lower InGaAs performance as capacitor-less DRAM.

D. LOW-VOLTAGE OPERATION

Several patterns, Fig. 3a (pattern a) and Fig. 11a-d (patterns b-e), were tested on both cells to study the memory performance at low front-gate and drain voltages. Results are summarized in Fig. 11e-f. Notice that the silicon cell is much more affected by the bias lowering than the InGaAs one (even with larger S/D doping concentrations). It turns out that the InGaAs cell is almost insensitive to the W_1 drain or anode voltage reduction by a 50% (compare patterns a with b and c) while the silicon cell is severely affected. Even when reducing all biases (including the holding gate voltage, pattern e), the InGaAs cell still operates as memory, although the performance is degraded. A reduction in the energy consumption for the InGaAs cell can be expected when matching the cells performance at low voltage operation.

VI. CONCLUSION

2D TCAD results suggest the feasibility of implementing capacitor-less memories on III-V materials, particularly MSDRAM cells on $In_{0.53}Ga_{0.47}As$ and close mole fraction compounds. Distinct logic states are demonstrated according to the previous biasing conditions (programmed state). Similar operation with respect to silicon cells is observed. Nonetheless, the larger intrinsic carrier density with respect to silicon, yields lower body potential wells, hence lower hole populations limiting the DRAM capabilities. In spite of the inferior InGaAs DRAM performance, this work fully motivates a further investigation and optimization through advanced calibrated TCAD simulations based on III-V experimental results. Moreover, InGaAs cells may potentially address, thanks to the customizable energy band-gap, low-power consumption cells for the Internet of Things. Additionally, other III-V materials and cell architectures can be targeted as well. For instance, III-V hetero-structure memories optimizing the S/D materials to enhance the hole storage can be considered.

REFERENCES

[1] "International roadmap for devices and systems," Hyderabad, India, IRDS, More Moore White Paper, 2016. [Online]. Available: https://irds.ieee.org/

[2] H.-J. Wann and C. Hu, "A capacitorless DRAM cell on SOI substrate," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Washington, DC, USA, 1993, pp. 635–638, doi: 10.1109/IEDM.1993.347280.

[3] N. Rodriguez *et al.*, "Experimental demonstration of capacitorless A2RAM cells on silicon-on-insulator," *IEEE Electron Device Lett.*, vol. 33, no. 12, pp. 1717–1719, Dec. 2012, doi: 10.1109/LED.2012.2221074.

[4] J. Wan, C. LeRoyer, A. Zaslavsky, and S. Cristoloveanu, "A compact capacitor-less high-speed DRAM using field effect-controlled charge regeneration," *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 179–181, Feb. 2012, doi: 10.1109/LED.2011.2176908.

[5] M. Bawedin, S. Cristoloveanu, and D. Flandre, "A capacitorless 1T-DRAM on SOI based on dynamic coupling and double-gate operation," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 795–798, Jul. 2008, doi: 10.1109/LED.2008.2000601.

[6] Y. J. Yoon *et al.*, "Capacitorless one-transistor dynamic random access memory based on double-gate GaAs junctionless transistor," *Jpn. J. Appl. Phys.*, vol. 56, Apr. 2017, Art. no. 06GF01, doi: 10.7567/JJAP.56.06GF01.

[7] Y. J. Yoon, J. H. Seo, and I. M. Kang, "Capacitorless one-transistor dynamic random access memory based on asymmetric double-gate Ge/GaAs-heterojunction tunneling field-effect transistor with n-doped boosting layer and drain underlap structure," *Jpn. J. Appl. Phys.*, vol. 57, Feb. 2018, Art. no. 04FG03, doi: 10.7567/JJAP.57.04FG03.

[8] C. Navarro *et al.*, "Towards InGaAs MS-DRAM memory cells," *ECS Trans.*, vol. 85, no. 8, pp. 195–200, 2018, doi: 10.1149/08508.0195ecst.

[9] A. Pal *et al.*, "GaP source-drain vertical transistor on bulk silicon for 1-transistor DRAM application," in *Proc. 5th IEEE Int. Memory Workshop*, Monterey, CA, USA, 2013, pp. 192–195, doi: 10.1109/IMW.2013.6582132.

[10] J.-P. Colinge, *Silicon-on-Insulator Technology: Materials of VLSI*. New York, NY, USA: Springer, 2004, doi: 10.1007/978-1-4419-9106-5.

[11] *Sentaurus Device User Guide (Version J-2014.09)*, Synopsys Inc., Mountain View, CA, USA, 2014.

[12] L. Czornomaz *et al.*, "Confined epitaxial lateral overgrowth (CELO): A novel concept for scalable integration of CMOS-compatible InGaAs-on-insulator MOSFETs on large-area Si substrates," in *Proc. Symp. VLSI Technol. (VLSI Technol.)*, Kyoto, Japan, 2015, pp. T172–T173, doi: 10.1109/VLSIT.2015.7223666.

[13] V. Deshpande *et al.*, "First demonstration of 3D SRAM through 3D monolithic integration of InGaAs n-FinFETs on FDSOI Si CMOS with inter-layer contacts," in *Proc. Symp. VLSI Technol. (VLSI Technol.)*, Kyoto, Japan, 2017, pp. T74–T75, doi: 10.23919/VLSIT.2017.7998205.

[14] T. P. Pearsall and J. P. Hirtz, "The carrier mobilities in $Ga_{0.47}In_{0.53}as$ grown by organo-mettalic CVD and liquid-phase epitaxy," *J. Cryst. Growth*, vol. 54, no. 1, pp. 127–131, 1981, doi: 10.1016/0022-0248(81)90258-X.

[15] C. B. Zota, L. E. Wernersson, and E. Lind, "High-performance lateral nanowire InGaAs MOSFETs with improved on-current," *IEEE Electron Device Lett.*, vol. 37, no. 10, pp. 1264–1267, Oct. 2016, doi: 10.1109/LED.2016.2602841.

[16] S. Okhonin, M. Nagoga, J. M. Sallese, and P. Fazan, "A SOI capacitor-less 1T-DRAM concept," in *Proc. IEEE Int. SOI Conf.*, Durango, CO, USA, 2001, pp. 153–154, doi: 10.1109/SOIC.2001.958032.

[17] C. Navarro *et al.*, "Extended analysis of the Z^2-FET: Operation as capacitorless eDRAM," *IEEE Trans. Electron Devices*, vol. 64, no. 11, pp. 4486–4491, Nov. 2017, doi: 10.1109/TED.2017.2751141.

[18] S. Cristoloveanu *et al.*, "A review of the Z^2-FET 1T-DRAM memory: Operation mechanisms and key parameters," *Solid State Electron.*, vol. 38, pp. 10–19, May 2018, doi: 10.1016/j.sse.2017.11.012.

[19] S. Navarro *et al.*, "Experimental demonstration of operational Z^2-FET memory matrix," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 660–663, Mar. 2018, doi: 10.1109/LED.2018.2819801.

[20] H.-K. Lim and J. G. Fossum, "Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFET's," *IEEE Trans. Electron Devices*, vol. 30, no. 10, pp. 1244–1251, Oct. 1983, doi: 10.1109/T-ED.1983.21282.

[21] M. Bawedin, S. Cristoloveanu, D. Flandre, and F. Udrea, "Dynamic body potential variation in FD SOI MOSFETs operated in deep non-equilibrium regime: Model and applications," *Solid-State Electron.*, vol. 54, no. 2, pp. 104–114, Feb. 2010, doi: 10.1016/j.sse.2009.12.004.

[22] A. Marshall and S. Natarajan, *SOI Design: Analog, Memory and Digital Techniques*. New York, NY, USA: Springer, 2002, doi: 10.1007/b100866.

[23] A. G. Lind, H. L. Aldridge, Jr., C. Hatem, M. E. Law, and K. S. Jones, "Review: Dopant selection considerations and equilibrium thermal processing limits for n^+ $In_{0.53}Ga_{0.47}As$," *ECS J. Solid State Sci. Technol.*, vol. 5, no. 5, pp. Q125–Q131, 2016, doi: 10.1149/2.0201605jss.

[24] M. E. Levinshtein, S. L. Rumyantsev, and M. Shur, *Handbook Series on Semiconductor Parameters. Volume 2: Ternary and Quaternary III-V Compounds*. Singapore: World Sci., 1999.

[25] *Sentaurus Device User Guide (Version N-2017.09)*, Synopsys Inc., Mountain View, CA, USA, 2017.

[26] M. S. Shur, "Low ballistic mobility in submicron HEMTs," *IEEE Electron Device Lett.*, vol. 23, no. 9, pp. 511–513, 2002, doi: 10.1109/LED.2002.802679.

[27] M. G. Ancona and H. F. Tiersten, "Macroscopic physics of the silicon inversion layer," *Phys. Rev. B, Condens. Matter*, vol. 35, no. 15, pp. 7959–7965, 1987, doi: 10.1103/PhysRevB.35.7959.

[28] M. G. Ancona and G. J. Iafrate, "Quantum correction to the equation of state of an electron gas in a semiconductor," *Phys. Rev. B, Condens. Matter*, vol. 39, no. 13, pp. 9536–9540, 1989, doi: 10.1103/PhysRevB.39.9536.

[29] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, "Volume inversion in SOI MOSFETs with double gate control: A new transistor operation with greatly enhanced performance," in *Proc. 17th Eur. Solid State Device Res. Conf. (ESSDERC)*, Bologna, Italy, 1987, pp. 399–402.

[30] W. Schwarzenbach, C. Malaquin, F. Allibert, G. Besnard, and B.-Y. Nguyen, "Systematic evaluation of SOI buried oxide reliability for partially depleted and fully depleted applications," in *Proc. IEEE SOI 3D Subthreshold Microelectron. Technol. Unified Conf. (S3S)*, Rohnert Park, CA, USA, 2015, pp. 1–3, doi: 10.1109/S3S.2015.7333496.

[31] S. Eminente, S. Cristoloveanu, R. Clerc, A. Ohata, and G. Ghibaudo, "Ultra-thin fully-depleted SOI MOSFETs: Special charge properties and coupling effects," *Solid State Electron.*, vol. 51, no. 2, pp. 239–244, Feb. 2007, doi: 10.1016/j.sse.2007.01.016.

[32] S. Cristoloveanu, S. Athanasiou, M. Bawedin, and P. Galy, "Evidence of supercoupling effect in ultrathin silicon layers using a four-gate MOSFET," *IEEE Electron Device Lett.*, vol. 38, no. 2, pp. 157–159, Feb. 2017, doi: 10.1109/LED.2016.2637563.

[33] C. Navarro *et al.*, "Supercoupling effect in short-channel ultrathin fully depleted silicon-on-insulator transistors," *J. Appl. Phys.*, vol. 118, Oct. 2015, Art. no. 184504, doi: 10.1063/1.4935453.

[34] G. Brammertz *et al.*, "On the interface state density at In0.53Ga0.47As/oxide interfaces," *Appl. Phys. Lett.*, vol. 95, no. 20, Nov. 2009, Art. no. 202109, doi: 10.1063/1.3267104.

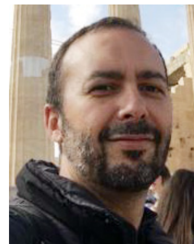
CARLOS NAVARRO received the Ph.D. degrees in electrical engineering from the University of Granada, Granada, Spain, in 2014, and the Institute of Microelectronics, Electromagnetism and Photonics, Grenoble, France, in 2015. He is currently a Post-Doctoral Researcher with the University of Granada. He has authored or co-authored over 60 journal articles or conference abstracts. His current research interests include SOI devices and capacitor-less memory cells.

SANTIAGO NAVARRO was born in Granada, Spain, in 1984. He received the B.Sc. degree from the University of Granada in 2011 and the M.Sc. degree from the University of Seville in 2013. He is currently pursuing the Ph.D. degree in electronics engineering with the University of Granada. His research interest is on SOI devices and 1T-DRAM cells.

CARLOS MARQUEZ received the M.Sc. degree in telecommunication engineering, the M.S. degree in electrical engineering, and the Ph.D. degree in electronics from the University of Granada, Granada, Spain, in 2012, 2014, and 2017, respectively. He has authored or co-authored 11 peer-reviewed international journal articles, two book chapters, and 12 conference proceedings. His research interests include the electrical characterization of semiconductor devices, MOSFET front-end-of the line reliability, one-transistor dynamic-random-access-memory cells, and 2-D materials.

LUCA DONETTI received the M.Sc. degree in physics from the University of Parma, Parma, Italy, in 1998 and the Ph.D. degree in physics from the Università degli Studi di Milano, Milan, Italy, in 2002.

Since 2005, he has been with the Department of Electronics, Faculty of Sciences, University of Granada, Granada, Spain. His current research interests include the simulation of electron and hole transport properties in nanoscale electronic devices, including SOI and multigate devices, focussing on carrier band-structure effects including simple nonparabolicity models, k·p Hamiltonians up to *ab-initio* calculations, and on quantum effects.



CARLOS SAMPEDRO received the Ph.D. degree from the University of Granada, Granada, Spain, in 2006.

Since 2011, he has been an Associate Professor with the Nanoelectronics Research Group, University of Granada. His current research interest includes advanced numerical simulation and modeling of ultimate scaled multi-gate, advanced silicon-on-insulator, and nonconventional devices.

SIEGFRIED KARG received the Ph.D. degree in physics from University of Bayreuth, Germany, in 1995. He has been a Research Staff Member with IBM Research—Zurich since 2000. He was a Post-Doctoral Fellow with IBM Research—Almaden from 1995 to 1996 and an Research Assistant with the Darmstadt University of Technology from 1997 to 1999. He worked on the physics and materials science of organic and polymer devices (OLEDs, OFETs, and electrochemical cells) and memory applications (resistive oxide RAM). He has authored about 90 publications and holds over 30 patents. His current research fields are 1-D electronic properties of nanostructures, applications of III-V semiconductor devices and brain-inspired computing.

H. RIEL photograph and biography not available at the time of publication.

FRANCISCO GAMIZ received the B.S. degree (Hons.) in physics and the Ph.D. degree (Hons.) from the University of Granada, in 1991 and 1994, respectively. Since 2005, he has been a Full Professor of electronics and since 2008, the Head of the Nanoelectronics and Graphene Research Labs. He was a recipient of Best Student Award from the University of Granada.

He has co-authored over 350 refereed papers in major journal and international conference proceedings and several book chapters. He is a co-holder of several international patents related to multibody 1T-DRAM.