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Physical Insights on Quantum Confinement and Carrier Mobility in Si, $Si_{0.45}Ge_{0.55}$, Ge Gate-All-Around NSFET for 5 nm Technology Node

JIAXIN YAO[1,2], JUN LI[3], KUN LUO[1], JIAHAN YU[1], QINGZHU ZHANG[1], ZHAOZHAO HOU[1,2], JIE GU[1,2], WEN YANG[4], ZHENHUA WU[1], HUAXIANG YIN[1,2], AND WENWU WANG[1]

1 Key Laboratory of Microelectronics Devices and Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China
2 University of Chinese Academy of Sciences, Beijing 100049, China
3 Semiconductor Photonics Research Center, Xiamen University, Xiamen 361005, China
4 Simulation of Physical Systems Division, Beijing Computational Science Research Center, Beijing 100094, China

CORRESPONDING AUTHORS: Z. WU AND H. YIN (e-mail: wuzhenhua@ime.ac.cn; yinhuaxiang@ime.ac.cn)

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ABSTRACT We present a comprehensive theoretical investigation of the quantum confinement limited mobility in the $Si_{1-x}Ge_x$-channel gate-all-around nanosheet field effect transistor for 5-nm node. The study encompasses physics-based quantum mechanical models both for P and NMOS with specified channel/wafer orientations and channel thicknesses: 1) k.p model with Poisson solver for band structures, bandgap variations, and confined charge distributions; 2) Kubo-greenwood model for low field mobility with considering surface roughness and stress; 3) multisub-band Boltzmann transport equation based on a state-of-the-art phase space approach is employed to evaluate device IV characteristics; and 4) the threshold voltage (V_T) variations with different channel/wafer orientations are also evaluated. Our simulation study shows that {110} wafer Ge channel can be an attractive option for 5-nm node pMOS, and Si is still promising for nMOS due to strong quantum confinement in Ge channel.

INDEX TERMS Quantum confinement, mobility, GAA NSFET.

I. INTRODUCTION

For devices beyond the 10/7nm technology node, it is important to investigate performance boosters such as superior gate-all-around (GAA) architectures [1]–[6] and/or high mobility channels [7]–[12]. Recently a new stacked GAA nanosheet field effect transistor (NSFET) has been demonstrated experimentally as a promising candidate for 5nm technology node MOSFET, which offers good co-optimization of superior gate control and high on-state currents per footprint [13]. It is urgently desired to physically estimate the performance of such a NSFET with high mobility channels, like SiGe or Ge. Although the carrier mobility of bulk Ge is much higher than that of bulk Si, especially for holes. The significance of mobility degradation mainly due to the quantum effect in extremely thin channels as well as some other conventional problems like surface passivation and integration with Si raises the doubt about the implementation of Ge or SiGe channel in future CMOS of 5nm technology node and beyond. The accurate modeling of the electron/hole mobility with considering the quantum confinement and its impact on various carrier scattering sources in device has become an important issue to predict the performance of future SiGe based NSFETs. We need accurately calculate the band structure and carrier mobility both for P and NMOS with various channel/wafer orientations in the presence of the strong quantum confinement in the ultra-thin scaled nanosheet.

In this paper, we present a systematic assessment of both electron and hole mobility in ultra-thin SiGe NSFETs as shown in Fig. 1, accounting for the impacts of quantum confinement, $Si_{1-x}Ge_x$ channel, channel/wafer orientation, as well as applied strain. Then the device characteristics

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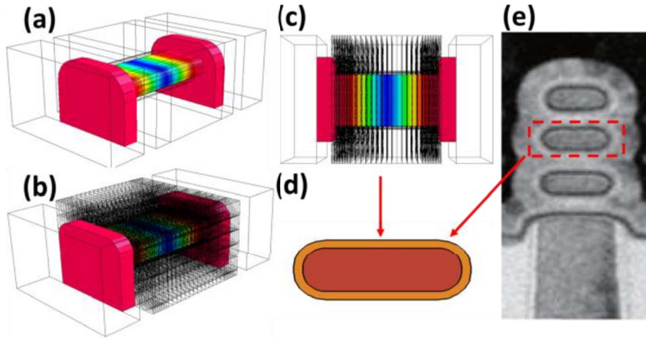

FIGURE 1. (a) 3D simulation domain of a single NSFET structure. (b) Schematic of slicing scheme for solving coupled k.p and multi-subband Boltzmann equation. (c) The same as panel (b) but in top view. (d) 2D simulation domain of a cross section in the channel region. (e) TEM image of a stacked triple nanosheet FET reported in ref. [13].

are evaluated by using multi-subband Boltzmann transport equation based on the physical mobility in contrast to the conventional semi classical drift-diffusion approach employing the empirical mobility parameters. Our simulation framework implements the physics-based quantum mechanical models for both mobility and transport calculations as briefly explained in the next section. The benefits of allowing for virtually fit-parameter-free simulations make the current framework pretty suitable for evaluating upcoming 5nm node transistors.

II. SIMULATION MODEL

To obtain the electrostatic properties with quantum confinement, the device is divided into several slices. In each slice, two-dimensional quantum confinement inside the channel is calculated by solving the 2D Schrödinger equation with k.p Hamiltonian, validated by ab-initio calculations, instead of the effective mass approximation [14]–[16]. It therefore gives accurate full subband structure rather than the band edge information. The geometry, channel orientation effects are naturally adopted in the calculations. The strain effect is captured by deformation potentials for k.p method. Phonon (acoustic, optical and intervalley models), surface roughness, ionized impurity and alloy scattering mechanisms are considered to calculate the low-field mobility by using Kubo-Greenwood formula (KGF) with k.p Hamiltonian [17] in the channel cross section. For the indirect bandgap semiconductors (Si, Ge), the conduction band edge and valence band edge are far from each other, and thus be solved separately. We use a 2-band k.p Hamiltonian for electrons and a 6-band k.p Hamiltonian for holes. Therefore, the problem of spurious solutions from k.p method [18] can be avoided in our calculations.

The calculation of carrier scattering is based on Fermi Golden Rule by evaluating the square matrix element and finding the transition rate $S_{n,n'}(k,\ k')$. With the full subband structure, all the square matrix elements can be calculated accounting for ionized impurity, phonon, surface roughness, and alloy scattering mechanisms, with specific expressions respectively [19]. Especially, for surface roughness scattering (SRS) in the quasi 1-dimensional (1D) GAA nanosheet FET, the transport is related to 1D momentum (k, k'). However, arising from the finite (non-zero) diameter, the surface roughness at the 2D surface is described by the actual fluctuation of the interface position, $\Delta(\boldsymbol{r})$. And it is characterized by its autocorrelation function $C(\mathbf{r}) \equiv \langle\Delta(\boldsymbol{r'})\Delta(\boldsymbol{r'}+\boldsymbol{r})\rangle$, depending on a 2D $\mathbf{r}$ vector and its 2D Fourier transform $C(\boldsymbol{q})$, depending on a 2D $\boldsymbol{q}$ vector. Note that the roughness power spectrum is isotropic, giving rise to $C(\boldsymbol{q}) = C(q)$ [20]. Then the matrix element of the scattering potential between states (n, k) and (n′, k′) is given by,

$$\left\langle\left|H_{n,n';\,k,k'}\right|^2\right\rangle = \frac{1}{2\pi L}\int_{\mathbb{R}}\left|F_{n,n';\,k,k'}\left(q_\perp\right)\right|^2 C\left(q\right)dq_\perp, \quad (1)$$

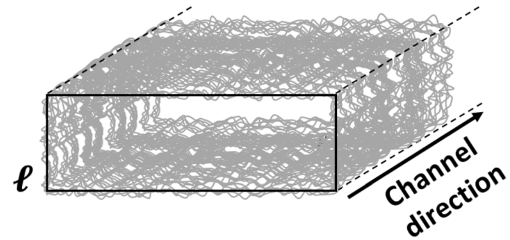

FIGURE 2. Sketch of GAA channel's roughness surface. Solid line: slice circumference ℓ.

where $q = \sqrt{q_\parallel{}^2 + q_\perp{}^2}$ is the roughness wave vector and separated into an axial component $q_\parallel \equiv k - k'$ (in the channel direction) and component $q_\perp$ (along the slice circumference ℓ) as illustrated in Fig. 2. $F_{n,n';\,k,k'}(q_\perp)$ is called a spectral form-function. The alloy scattering in SiGe channel is treated by the following scattering matrix [21],

$$\left\langle\left|H_{n,n';\,k,k'}\right|^2\right\rangle = \frac{\Delta E_{edge}^2 V_{cell}}{L^2}\int x\left(1-x\right)\left|\psi_{n,k}\left(r\right)\right|^2\left|\psi_{n',k'}\left(r\right)\right|^2 dr, \quad (2)$$

where ΔE_{edge} is the band edge offset between the two alloyed materials, x is the alloy fraction, L is the normalization length. Regarding to the screening model in the ionized impurity scattering, the linear approximation (around k-k$' = 0$) in the Poisson equation is used. Thus, screenings of surface roughness and alloy scattering are also considered implicitly in our treatment [22]. EOT is fixed at 1nm, and the widths of NSFET (W) are set to 15nm for all NSFETs in this work. The overall simulation methodology is summarized in Fig. 3. Connected with the physical mobility, device transport properties are simulated by both a conventional drift-diffusion framework for subthreshold region and a deterministic solver for the phase-space subband Boltzmann transport equation for saturation region based on the same scattering rate. BTE is discretized by cutting slices along the channel direction. The number of slices has been proved to be large enough to give converged results.

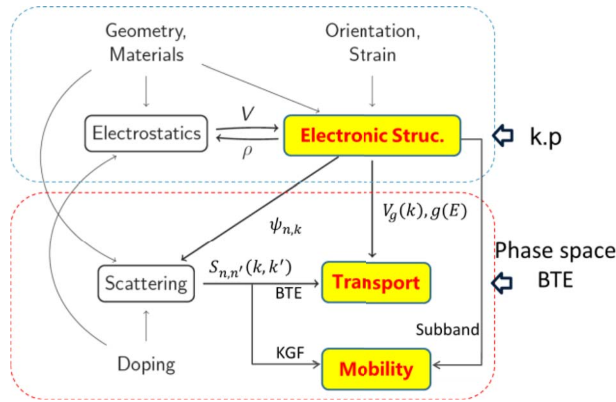

FIGURE 3. Schematic of the simulation methodology employed in this work. Two major advantages than conventional simulation models are 1) k.p model for accurate band structure and quantum confinement. 2) Physical mobility with state-of-the-art phase space BTE for charge transport.

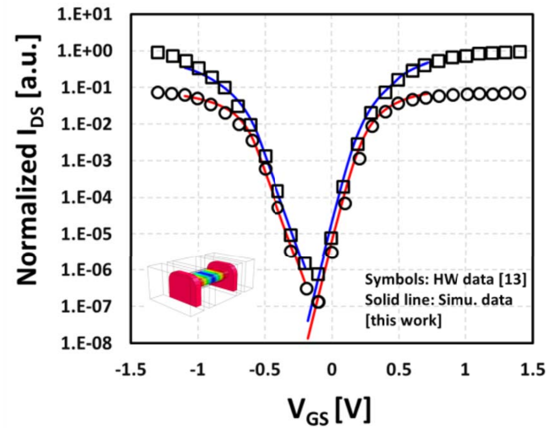

FIGURE 4. Model validation by comparing with published hardware data from [13], for W=15nm, $T_{CH} = 5$ nm, $L_G = 12$nm, $T_{SPC} = 5$nm (inner spacer thickness), Gate Pitch=44nm. The key parameters of 2-band k.p Hamiltonian for conduction band and 2-band k.p Hamiltonian for valence band are $m_l = 0.916m_0$, $m_t = 0.196m_0$, $\gamma_1 = 4.27$, $\gamma_2 = 0.315$, $\gamma_3 = 1.387$, respectively. The key parameters for SRS are correlation length (L_c)= 1 nm, RMS=0.5 nm. Note that only one normalized factor for both NMOS and PMOS is used, accounting for the single-channel NSFET in calculation.

III. RESULTS AND DISCUSSIONS

The target devices are ultra-scaled in order to meet 5nm technology design rules and performance expectations, and thus very limited experimental data for these dimensions are available in the literatures, most of which are only of silicon channel. Here, the physics-based quantum mechanical models in this study are verified with comparing to the recent experimental progress in Si-channel GAA NSFET [13]. Note that to get higher simulation efficiency without losing physical importance, we focus on a single channel NSFET rather than a triple NSFET. Fig. 1. (a)-(d) sketched the original 3D and sliced 2D simulation domain in this work referring to the experimentally demonstrated device as shown in Fig. 1. (e). The calculated physical mobility is incorporated into the Drift-Diffusion framework to get the I_{DS}-V_{GS} transfer characteristics in the subthreshold region. Alternatively, the I_{DS}-V_{GS} transfer characteristics in the saturation region are obtained from the solution of the full BTE to capture the ballistic transport features. So, the full I-V curves are calculated based on both the solutions of the KGF for low-field mobility and the BTE for high-field ballisticity at different bias respectively according to the V_T. Therefore, based on the physical mobility and phase space BTE solver, both the subthreshold and the saturation region current-voltage transfer characteristics can be nicely matched from subthreshold to strong inversion region as shown in Fig. 4. At the crossing between subbands, of which branches are determined by the continuity of the flow, e.g., the continuity of electron group velocity [23].

To evaluate the possible performance boosters of channel materials, orientations, and geometry, we have investigated their impacts on the electrostatic and transport properties with the verified physical models. The quantum confinement effects in ultrathin channel are firstly evaluated by calculating the band structures and charge distributions. Fig. 5 shows the simulated effective bandgap as a function of channel dimension, evolution from a wide nanowire to a thin nanosheet.

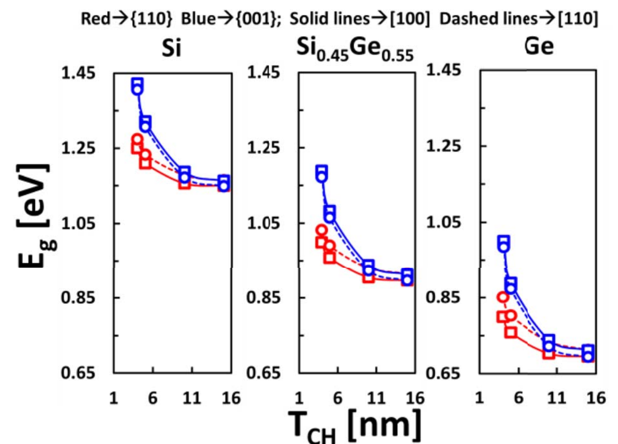

FIGURE 5. Bandgap variation with nanosheet thicknesses for Si, $Si_{0.45}Ge_{0.55}$, and Ge channel. The simulated effective bandgap as a function of channel thickness dimension from a wide nanowire to a thin nanosheet with [100]/{110}/{110}/{001}, and [110]/{001} channel/wafer orientations. The widths of all these NSFETs are fixed to 15nm.

The effective bandgap has a strong anisotropy in these three channel (Si, $Si_{0.45}Ge_{0.55}$, Ge) with different channel/wafer orientations. The band structures and corresponding quantum confinement of SiGe NSFET channels are obtained with the ab-initio-calculation validated k.p method as shown in Fig. 6 (a)-8 (a) for different Ge compositions. We find distinct subbands of light or heavy charge carriers in conduction band. Electrons can be distributed in two sets of steep bands and shallow bands that indicate light and heavy effective mass respectively. It is a quasi 1D counterpart of the bulk electron populating in primed and unprimed ladder of subbands. In valence band we also find two sets of subbands that are simple splitting of the light hole and heavy hole branches in the strongly confined channel. The

composition of the two sets of light and heavy carrier subbands is crucial to the upper limit of the electron and hole mobility in the NSFET. Strong anisotropy is observed in the band structures. Much more light electron and hole subbands appear with [100]/{110} and [110]/{001} channel/wafer orientations than that in [100]/{001} and [110]/{110} channel/wafer orientations, indicating higher carrier mobility in the formal cases. Beside the well-known thickness impacts on the bandgap, we also find its modulation of the light-/heavy-hole subbands composition in the channel with the specified {110} surface confinement. This feature leads to non-intuitive mobility behavior as we will discuss later. Additionally, electron and hole carrier density profiles in the 2D cross section of 15nm × 5nm GAA NSFETs at on-state V_G and zero V_D for Si, $Si_{0.45}Ge_{0.55}$, and Ge GAA nanosheet with different channel/wafer orientations is shown in Fig. 6 (b)-8 (b). Electron and hole density is extremely high at the on-state in 2D cross section region due to the strong quantum confinement in Si and Ge channel, respectively. Strong anisotropy is also observed in four different channel/wafer orientations for both electron and hole density profiles.

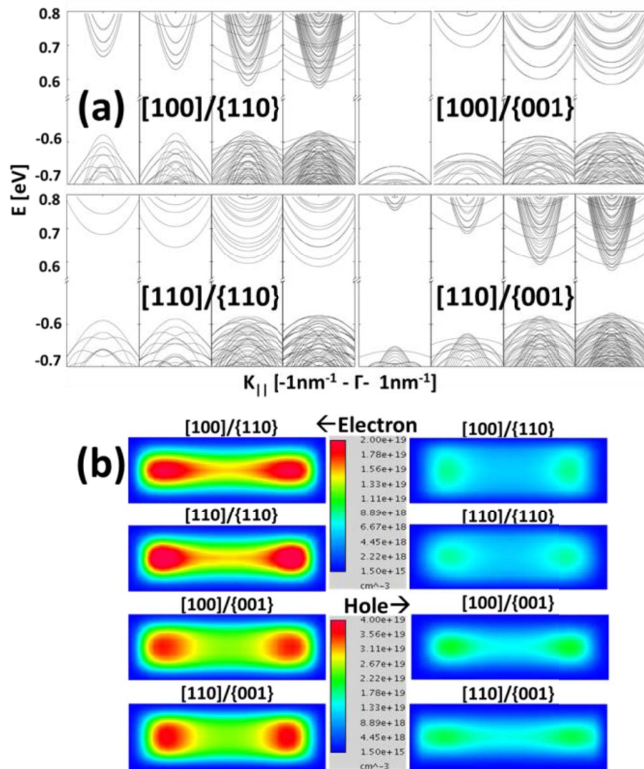

FIGURE 6. (a)Full subband structures of 15nm × 4nm, 15nm × 5nm, 15nm × 10nm, and 15nm × 15nm (from left to right) Si channel GAA nanosheet with four different channel/wafer orientations; (b) electron and hole density profiles in the 2D cross sections of 15nm × 5nm GAA NSFET at on-state V_G and zero V_D for Si GAA nanosheet with four different channel/wafer orientations.

To confirm this theoretical analysis of the intrinsic channel properties, we plot the electron and hole mobility in the un-doped channel at zero gate bias for varied geometries and Ge compositions in Fig. 9. Beside the intrinsic impacts from the channel geometry and material, the impacts of the surface roughness are obtained by using a Gaussian spectrum with RMS=1.0nm and correlation length L_C = 1.0nm. As expected, the [100]/{110} and [110]/{001} channel/wafer orientations give rise to higher mobility for both electrons and holes. In particular for the [100]/{110} channel/wafer orientation, hole mobility increases dramatically in the ultrathin nanosheet rather than the trivial degradation trend. This behavior well explains the measurement data [24], [25] and originates from the confinement induced band structure variations that decrease the hole effective mass and the scattering rates as mentioned in previous discussion about Fig. 6(a). Unlike the situation in the bulk Ge, the ultrathin Ge channel possesses no benefit for electron mobility and that in $Si_{0.45}Ge_{0.55}$ channel is even worse due to the alloy scattering. The hole mobility can be effectively boosted by replacing Si with Ge or SiGe. Therefore, at 5nm technology node, one should consider Ge channel for PMOS whereas Si channel is still preferred for NMOS.

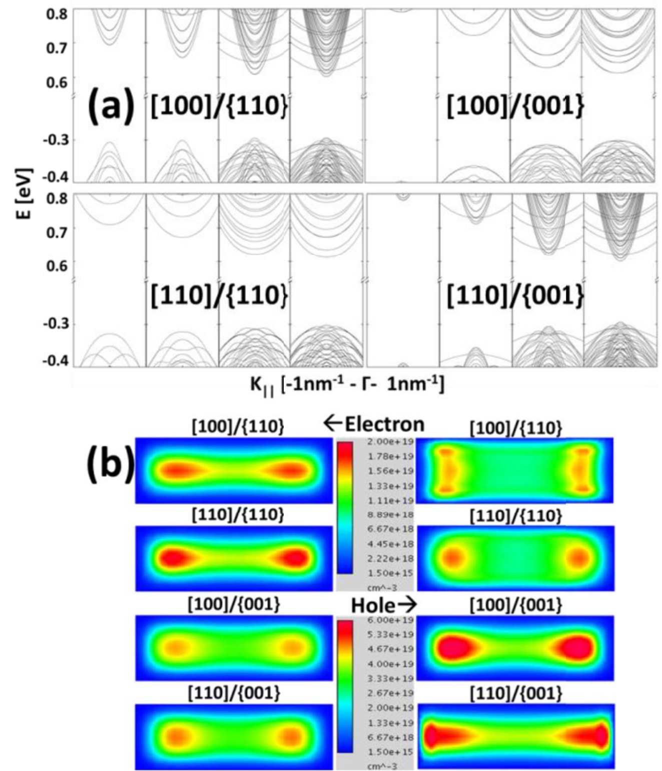

FIGURE 7. (a)The same as Fig. 6, but with $Si_{0.45}Ge_{0.55}$ channel; (b) electron and hole density profiles in the 2D cross sections of 15nm × 5nm GAA NSFET at on-state V_G and zero V_D for $Si_{0.45}Ge_{0.55}$ GAA nanosheet with four different channel/wafer orientations.

Next we examine the SRS limited mobility of the preferred [100]/{110} channel/wafer orientation with Si, $Si_{0.45}Ge_{0.55}$, Ge in Fig. 10. The device cross-section geometry is 15nm (width) × 5nm (thickness). It shows that the SRS becomes most critical at high gate bias in real device

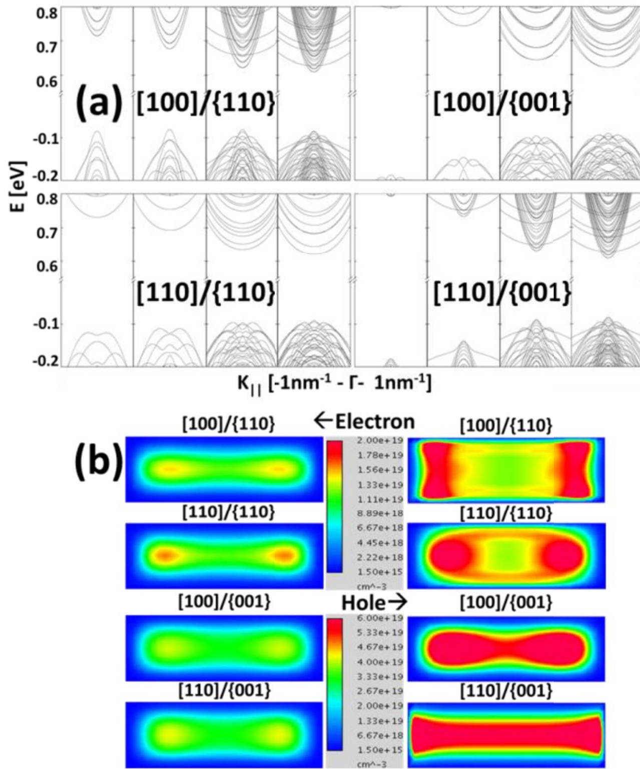

FIGURE 8. (a) The same as Fig. 6, but with Ge channel; (b) electron and hole density profiles in the 2D cross sections of 15nm × 5nm GAA NSFET at on-state V_G and zero V_D for $Si_{0.45}Ge_{0.55}$ GAA nanosheet with four different channel/wafer orientations.

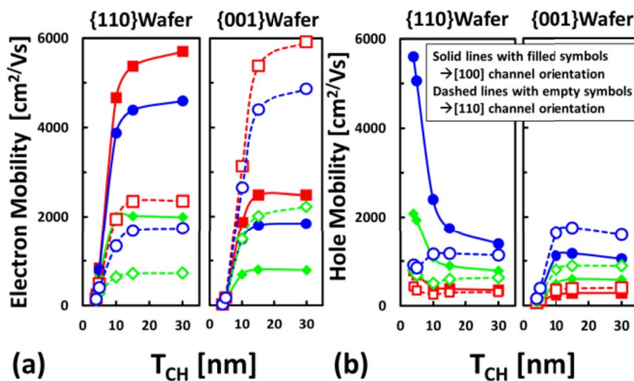

FIGURE 9. (a) Electron mobility accounting for phonon, surface roughness and alloy scatterings of 15nm × 5nm (width × thickness) GAA nanosheets for different channel/wafer orientations and $Si_{1-x}Ge_x$ compositions (red: x=0; green: x=0.55; blue: x=1); (b) hole mobility respectively.

where ideal surface quality cannot be achieved. In Si channel, the maximum local inversion densities of hole in PMOS and electron in NMOS are 1.52×10^{19} and 1.32×10^{19} cm^{-3}, respectively. While the average inversion linear densities of hole in PMOS and electron in NMOS are 6.58×10^{6} and 3.17×10^{6} cm^{-1}, respectively. In $Si_{0.45}Ge_{0.55}$ channel, the maximum local inversion densities of hole in PMOS and electron in NMOS are 5.22×10^{19} and 1.03×10^{19} cm^{-3}, respectively. While the average inversion linear densities

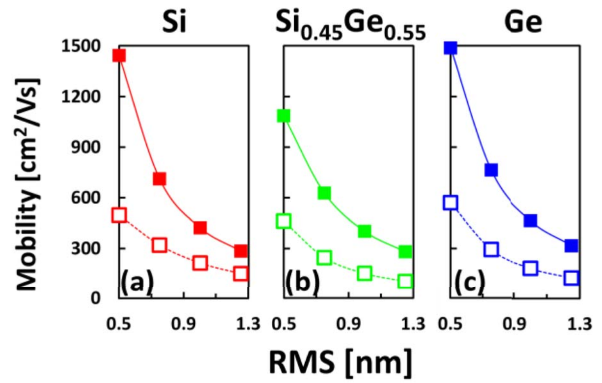

FIGURE 10. Electron (solid line) and hole mobility (dashed line) as a function of RMS with the preferred [100]/{110} channel/wafer orientation for on-state (a) Si , (b) $Si_{0.45}Ge_{0.55}$, and (c) Ge channel.

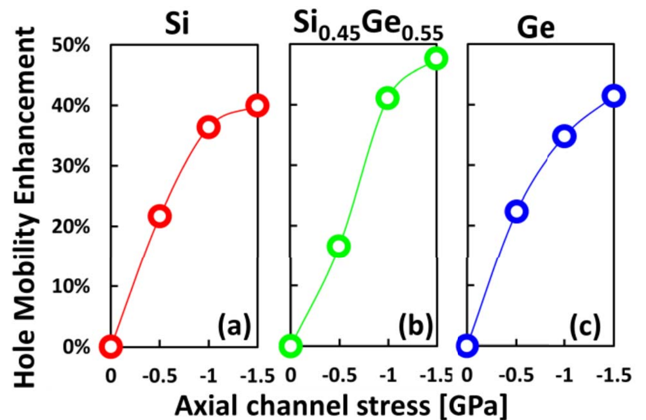

FIGURE 11. Hole mobility enhancement with compressive axial channel stress with the preferred [100]/{110} channel/wafer orientation for on-state (a) Si, (b) $Si_{0.45}Ge_{0.55}$, and (c) Ge channel. 40% mobility gain is expected under 1.5GPa compressive stress.

of hole in PMOS and electron in NMOS are 2.03×10^{7} and 2.45×10^{6} cm^{-1}, respectively. In Ge channel, maximum local inversion densities of hole in PMOS and electron in NMOS are 8.02×10^{19} and 7.80×10^{19} cm^{-3}, respectively. While the average inversion linear densities of hole in PMOS and electron in NMOS are 3.18×10^{7} and 1.87×10^{6} cm^{-1}, respectively. To obtain the desired performance, the Root Mean Square (RMS) roughness should be bellow 1nm, which brings severe challenges in process development.

Note that the full band k.p calculation used in this work can exclude the mobility underestimation in calculation based on effective mass method even with non-parabolic band corrections. Stress is an important performance knob for PMOS. We evaluate the stress effects on PMOS in the preferred [100]/{110} channel/wafer orientation with Si, $Si_{0.45}Ge_{0.55}$, and Ge. Importantly, about 40% mobility gain is expected under 1.5GPa axial compressive stress for PMOS channel with W=15nm and T_{CH} = 5nm as shown in Fig. 11. In detail, for Si-channel PMOS, the maximum local inversion densities of hole are 1.58×10^{19}, 1.78×10^{19}, and 1.97×10^{19} cm^{-3} under 0.5, 1.0, and 1.5 GPa compressive stress. While the average inversion linear densities of

hole are 6.95×10^6, 7.41×10^6, and 7.95×10^6 cm^{-1} under 0.5, 1.0, and 1.5 GPa compressive stress. For $Si_{0.45}Ge_{0.55}$-channel PMOS, the maximum local inversion densities of hole are 5.53×10^{19}, 5.81×10^{19}, and 6.07×10^{19} cm^{-3} under 0.5, 1.0, and 1.5 GPa compressive stress. While the average inversion linear densities of hole are 2.08×10^7, 2.13×10^7, and 2.20×10^7 cm^{-1} under 0.5, 1.0, and 1.5 GPa compressive stress. For Ge-channel PMOS, the maximum local inversion densities of hole are 8.22×10^{19}, 8.41×10^{19}, and 8.59×10^{19} cm^{-3} under 0.5, 1.0, and 1.5 GPa compressive stress. While the average inversion linear densities of hole are 3.27×10^7, 3.29×10^7, and 3.35×10^7 cm^{-1} under 0.5, 1.0, and 1.5 GPa compressive stress. The surface roughness parameters considered in Fig. 11 are not changed in the hole mobility enhancement by compressive stress [26]. Hence, advanced surface passivation process [27] and effective stressor [28], [29] are strongly desired in the GAA NSFETs for 5nm technology node and beyond.

Apart fro the trade of between the good gate control and mobility degradation, variation on the device characteristics is another challenge of very narrow channel. We evaluate the threshold voltage (V_T) variation as a function of the channel thickness with the preferred Ge content and channel/wafer orientations for both NMOS and PMOS as discussed before. Accounting for strong quantum effects, the V_T is defined as [30]:

$$\frac{\partial Q_{inv}}{\partial V_G}\bigg|_{V_T} = \frac{\partial Q_{depl}}{\partial V_G}\bigg|_{V_T}, \quad (3)$$

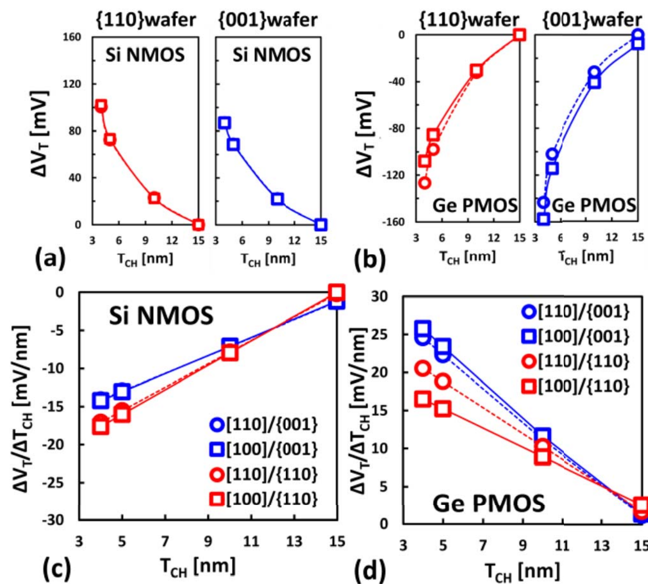

FIGURE 12. (a) V_T shift of Si NMOS Si NMOS with {110} and {001} wafer orientations respectively; (b) Ge PMOS with {110} and {001} wafer orientations respectively. Solid lines are of [100] channel orientation, dashed lines are of [110] channel orientation; (c) The V_T sensitivity to channel thickness of Si NMOS, (d) the same as (c) but for Ge PMOS.

in which Q_{inv} is the total inversion charge, Q_{depl} is the depletion charge. Fig. 12 (a) and (b) show the calculated threshold voltage (V_T) shift with reference to the V_T values of 15-nm-thick [100]/{110} channels. For Si NMOS, if the channel thickness is reduced to 5nm, the V_T shifts approach 72mV (or 68mV) in {110} (or {001}) wafer as results of the quantum effect on the band structure as we discussed before. The V_T shifts of the orthogonal [100] and [110] channel orientations are almost identical in each wafer. For Ge PMOS, the V_T shifts exhibit notable anisotropic feature along the orthogonal [100] and [110] channel directions in both {110} and {001} wafers, i.e., Ge PMOS of [100] channel shows a smaller (or larger) V_T shift as compared to [110] channel in {110} (or {001}) wafer with ultrathin channel thickness. Fig. 12 (c) and (d) show the extracted V_T sensitivity to channel thickness. For Si NMOS with 5nm-thick channel, the absolute values of V_T variation are around 16mV/nm (13mV/nm) in {110} (or {001}) wafer. The V_T variations in Ge PMOS with all the considered channel/wafer orientations range from 23mV/nm to 15mV/nm.

The V_T variation is more serious than that in NMOS due to stronger quantum confinement in Ge with lighter effective mass.

Consequently, the nanosheet FET of [100]/{110} channel/wafer orientation possesses both high mobility and overall good V_T stability accounting for both NMOS and PMOS nanosheet FET. In addition, we evaluated the performance booster of axial channel compressive strain for Ge PMOS, with the preferred [100]/{110} channel/wafer orientation as we just proposed. The on-state drive currents with difference stress are compared by aligning the off-state current to be the same. As shown in Fig. 13, obvious on-state current enhancement is acquired with 1.5 GPa compressive stress. As much as 13% additional on-state current gain is predicted in the presence of 1.5 GPa compressive stress in the Ge [100]/{110} channel.

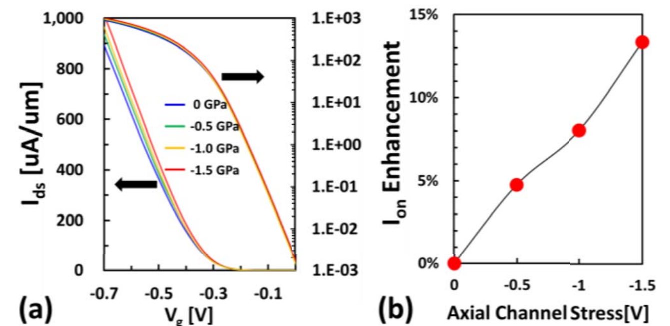

FIGURE 13. (a) IV curve for Ge PMOS with 0, −0.5, −1.0, and −1.5 GPa axial compressive channel stress with the preferred [100]/{110} channel/wafer orientation; (b) summary of I_{on} enhancement by axial channel compressive strain stress of −0.5, −1.0, −1.5 GPa.

IV. CONCLUSION

We present a comprehensive simulation study of the state-of-the-art GAA NSFET with $Si_{1-x}Ge_x$ channel. According to the calculated physical mobility with accurately incorporating the quantum confinement and complete scattering

mechanisms, [100]/{110} Ge-channel can be an attractive option for 5nm node PMOS, while Si still remains competitive capability for NMOS as Ge channel may not provide expected high mobility and V_T stability due to strong quantum confinement in the target dimension.

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JIAXIN YAO received the B.S. degree in electronic science and technology from Hunan University, Changsha, China, in 2015. He is currently pursuing the Ph.D. degree with the Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China. He is also with the University of Chinese Academy of Sciences. His current research interests include HKMG multi-VT modulation and TCAD model.

JUN LI received the Ph.D. degree from the Institute of Semiconductors, Chinese Academy of Sciences in 2010. He joined the Department of Physics, Xiamen University, as an Assistant Professor in 2010. His current research interests include physics of low-dimensional semiconductors and semiconductor spintronics.

KUN LUO received the B.S. degree in physics from Shandong University, Jinan, China, in 2015 and the M.S. degree in physics from the University of Durham, Durham, U.K. In 2017, he became a Research Intern with the Institute of Microelectronics, Chinese Academy of Sciences. His current research interest includes first principle and TCAD model.

JIAHAN YU received the M.S. degree in integrated circuit from the North China University of Technology, Beijing, China, in 2013. She was an Engineer with the Chinese Academy of Science, Beijing. Her current research focuses on advanced device characterization technology.

QINGZHU ZHANG received the B.S. degree from Guizhou University, Beijing, China, in 2014. He is currently pursuing the Ph.D. degree. In 2014, he joined the Institute of Microelectronic, Chinese Academy of Science, Beijing. His current research interests include advanced GAA NW CMOS FET and silicon NW sensors.

ZHAOZHAO HOU received the B.S. degree in electronic packaging from the Huazhong University of Science and Technology, Wuhan, China, in 2014. He is currently pursuing the Ph.D. degree with the Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China. He is also with the University of Chinese Academy of Sciences. His current research interests include flash memory devices, especially 3-D NAND.

JIE GU received the B.S. degree in applied physics from Zhejiang Sci-Tech University, Zhejiang, China, in 2016. He is currently pursuing the M.S. degree in integrated circuit process with the Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China. His current research interests include structure of FinFET and single-electron spin qubits.

WEN YANG received the Ph.D. degree in condensed matter physics from the Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China, in 2007. He has been with the Beijing Computational Science Research Center since 2011. His research interests include electronic and optical properties of semiconductor nanostructures and novel materials.

ZHENHUA WU received the Ph.D. degree in condensed matter physics from the Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China, in 2011. He joined Semiconductor Research and Development Center, Samsung Electronics, Suwon, South Korea, in 2011. In 2016, he became a Full Professor with the Chinese Academy of Science, Beijing. His current research interests include device physics and simulation of nanoscale transistors.

HUAXIANG YIN received the B.S. degree in semiconductor physics and devices from Tianjin University, Tianjin, China, in 1996 and the M.S. and Ph.D. degrees in microelectronics and solid-state electronics from the Chinese Academy of Sciences (CAS), Beijing, China, in 1999 and 2003, respectively. From 2003 to 2010, he was with the Samsung Advanced Institute of Technology, South Korea, as a Research Staff Member. In 2010, he joined the Institute of Microelectronics, CAS, where he is currently a Professor with the Integrated Circuit Advanced Process Center and the Key Laboratory of Microelectronics Devices and Integrated Technology. He holds 42 U.S. and 89 China awarded patents. He has authored or co-authored 54 SCI technical papers. His research interests include nano-scale CMOS device, VLSI manufacture technology, 2-D materials and devices, and Si X-ray detector

WENWU WANG received the Ph.D. degree from Tokyo University, Tokyo, Japan, in 2006. He has been with the Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China, since 2008. His current research interests cover Si/Ge-based processing and device technology, and novel 3-D CMOS devices.