Received 8 May 2018; revised 25 June 2018; accepted 9 July 2018. Date of publication 18 July 2018; date of current version 7 August 2018.
The review of this paper was arranged by Editor A. G. U. Perera.

Digital Object Identifier 10.1109/JEDS.2018.2856892

Enhancing Driving Performance of a-Si:H Thin-Film Transistors With Capacitive Coupling Method for Display Applications

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This work was supported in part by the Advanced Optoelectronic Technology Center, National Cheng Kung University, Tainan, Taiwan, and in part by the Ministry of Science and Technology of Taiwan under Project MOST 104-2221-E-006-189-MY3 and Project MOST 106-2218-E-006-024.

ABSTRACT A new capacitive coupling method to enhance the driving performance of hydrogenated amorphous silicon thin-film transistors (a-Si:H TFTs) in high-resolution applications is presented. The gate voltage can be enlarged by the entirely transmitted high voltage of a global direct current power source line (V_{DD}). Established models that are based on the measured electrical characteristics of fabricated a-Si:H TFTs with different aspect ratios are used to evaluate the feasibility of this proposed method in the gate driver. The maximum voltage of the gate voltage can be increased from 37.3 V to 47.6 V when V_{DD} is set to 20 V, improving the driving capability of the gate driver by more than 17%, based on the specifications of a 5.99 inch HD + (720 × 1440) panel at a frame rate of 120 Hz.

INDEX TERMS Capacitive coupling method, direct current (DC) power source, gate driver, high-resolution, hydrogenated amorphous silicon thin-film transistor (a-Si:H TFT).

I. INTRODUCTION

High-resolution active-matrix liquid-crystal displays (AMLCDs) have been widely used in consumer electronics because they provide an impressive visual experience to users [1]–[4]. As the resolution of displays grows, the scan time of each row line is decreased and the increase in the number of pixels clearly increases the loadings of the row lines [3]–[5], resulting in severely distorting scan pulses. Generally, the switching thin-film transistor (TFT) in a pixel must be operated in time to input the correct data voltage to yield the desired gray level [3]–[5]. Therefore, the generation by the gate driver of a scan pulse with a short rising time and a short falling time is important.

Recently, gate drivers have been increasingly integrated on glass substrates with TFTs eliminating the need for external driver ICs and related processes, providing low cost, compactness, and mechanical reliability [6]–[16]. Unlike low-temperature polycrystalline silicon (LTPS), hydrogenated amorphous silicon (a-Si:H) TFTs can be manufactured by a simple and mature process, which provides good uniformity and high yield [9]–[12]. However, the low carrier mobility of a-Si:H TFTs causes the difficulty in rapidly charging and discharging the row lines [1], [8], [9], [11], disfavoring the use of gate drivers in high-resolution applications.

Fig. 1 depicts the conventional driving structure of a gate driver [7], [9], [11]–[13] which is composed of an input TFT, a reset TFT, a storage capacitor, and a driving TFT. The driving TFT is used to generate the scan pulse that is transmitted to the row line and it is the largest in the gate driver. The most straightforward means to accelerate the charging and discharging of the output node is to widen the channel of the driving TFT. However, the amelioration thus achieved is insufficient to increase the resolution of a display because the width of scan pulses and the loadings of row lines become shorter and greater.

Therefore, Chiang and Li [3] presented a driving method that uses the clock signals with two low voltages to reduce the falling time of a-Si:H gate drivers. Nevertheless, such clock signals can increase the cost and complexity of the

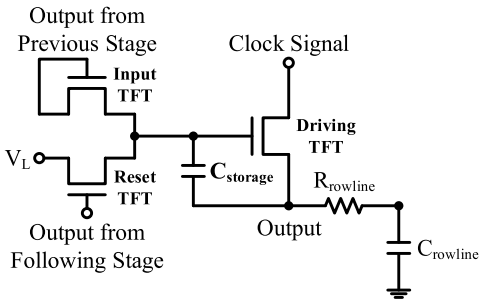

FIGURE 1. **Conventional driving structure of gate drivers.**

implementation of ICs. Kim *et al.* [14] developed a gate driver with pre-bootstrapping method to overcome the low mobility of p-type organic TFTs. However, as this method is applied to the n-type a-Si:H TFTs, the gate node of the driving TFT is reset as the output node is discharged, limiting the improvement of the falling time. Our previous work [4] proposed a two-step-bootstrapping structure to enhance the driving ability of the driving TFT without increasing of the channel width to reduce both rising and falling times. However, the reduction of the rising time is related to the threshold voltage of the TFT in the structure because the first bootstrapping of the gate voltage involves the charging of the TFT that is operated in the saturation region. Moreover, before the output node is discharged, the gate voltage is further bootstrapped by two capacitors in series. The equivalent capacitance is so small that the reduction of the falling time is restricted by the parasitic capacitance of the driving TFT.

This work proposes a new capacitive coupling method for gate drivers in which the gate voltage of the driving TFT is bootstrapped by the entirely transmitted high voltage before the voltage transient of the output waveform is generated. Moreover, the rising and falling times of the output waveforms can be further improved by modulating the voltage of a global direct current (DC) power source line (V_{DD}). Based on the measurements of fabricated a-Si:H TFTs with different aspect ratios and the specifications of a 5.99 inch HD + (720×1440) panel, the driving performance of the proposed method is evaluated using the established TFT models of an HSPICE simulator. The rising and falling times of the output waveforms are improved by 34% and 29%, respectively, by using a 20V V_{DD} when the RC loadings of the gate line are doubled and the pulse width of the clock signals is only 5 μs. Accordingly, the proposed capacitive coupling method is highly appropriate for gate drivers that are used in high-resolution panels.

II. CIRCUIT SCHEMATIC AND OPERATION

Fig. 2(a) presents the gate driver based on the proposed capacitive coupling method which is composed of 11 TFTs and three capacitors. Fig. 2(b) presents the corresponding timing diagram, and CK1-CK4, four overlapping clock signals, are used to drive the proposed gate driver. Notably, V_{DD} is a global DC power line that can be set at a voltage

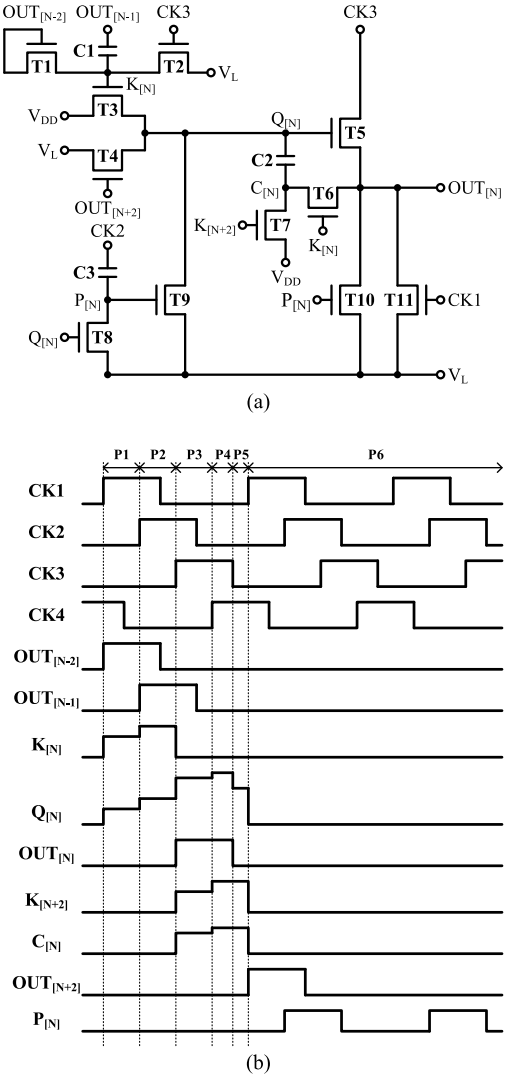

FIGURE 2. **Gate driver based on proposed capacitive coupling method. (a) Schematic. (b) Timing diagram.**

higher than the high voltage of clock signals, depending on the specifications of the panels.

$OUT_{[N-2]}$, $OUT_{[N-1]}$, $OUT_{[N]}$, and $OUT_{[N+2]}$ are respectively the output signals from the [N-2]th, [N-1]th, [N]th, and [N+2]th stages of the gate driver. $Q_{[N]}$ is the gate node of the driving TFT (T5), and the voltage of the $Q_{[N]}$ node is highly related to the charging and discharging rates of the $OUT_{[N]}$ node. $K_{[N]}$ is generated by the $OUT_{[N-2]}$ and $OUT_{[N-1]}$ signals through T1 and C1 to enhance the charging ability of the input TFT (T3), and $K_{[N+2]}$ is generated by the $OUT_{[N]}$ and $OUT_{[N+1]}$ signals. $C_{[N]}$ is utilized to bootstrap the voltage of $Q_{[N]}$, which is maintained at a high voltage during the discharging of the $OUT_{[N]}$ node. $P_{[N]}$ enables T9 and T10 to hold the $Q_{[N]}$ and $OUT_{[N]}$ nodes at a low voltage after the $OUT_{[N]}$ node is discharged.

The operation of the proposed gate driver is divided into the following six periods.

First period: The $OUT_{[N-2]}$ node changes from V_L to V_H, and the $K_{[N]}$ node is charged to V_H-V_{TH} through T1, turning on T3 and T6. The $Q_{[N]}$ node starts to be charged to V_{DD} and the $C_{[N]}$ and $OUT_{[N]}$ nodes are maintained at V_L through T5 and T6.

Second period: The voltages of CK2 and the $OUT_{[N-1]}$ node become V_H from V_L, the voltage of the $K_{[N]}$ node is increased to V_H - $V_{TH} + \Delta V_1$ owing to the capacitive coupling effect of C1, so V_{DD} can be fully transferred to the $Q_{[N]}$ node. Also, the $P_{[N]}$ node is maintained at V_L, turning off T9 and T10.

Third period: CK3 goes V_H from V_L, and T2 is turned on to reset the $K_{[N]}$ node, turning off T3 and T6. Meanwhile, the $OUT_{[N]}$ node starts to be charged to V_H with high speed through T5 because the $Q_{[N]}$ node has been already at V_{DD}. T7 is enabled by the $K_{[N+2]}$ node, and the voltage of the $C_{[N]}$ node is increased. Finally, the $Q_{[N]}$ node is bootstrapped to $V_{DD} + \Delta V_2$ because of C2 and the parasitic capacitance of T5, fully transmitting V_H to the $OUT_{[N]}$ node.

Fourth period: The $OUT_{[N+1]}$ node goes to V_H, and the $K_{[N+2]}$ node is coupled to V_H-$V_{TH} + \Delta V_1$. The $C_{[N]}$ node can thus be charged to V_{DD}, and the voltage of the $Q_{[N]}$ node is further raised to $V_{DD} + \Delta V_2 + \Delta V_3$ to enable the subsequent discharging of the $OUT_{[N]}$ node.

Fifth period: CK3 returns to V_L, and the $OUT_{[N]}$ node is discharged through T5, which has the greatest driving ability, since the $Q_{[N]}$ node was at the highest voltage in the previous period. Thus, the discharging of the $OUT_{[N]}$ node can be accelerated. Simultaneously, the voltage of the $Q_{[N]}$ node is decreased owing to the parasitic capacitance of T5.

Sixth period: The $OUT_{[N+2]}$ node is at V_H, so the $Q_{[N]}$ node is reset to V_L through T4. Meanwhile, CK1 changes to V_H, and the $K_{[N+2]}$ node is reset by CK1, turning off T7. Thus, the $C_{[N]}$ node becomes a floating point and can be pulled down with the $Q_{[N]}$ node. Afterward, as CK2 switches from V_L to V_H, the $P_{[N]}$ node is periodically coupled to V_P, turning on T9 and T10 stabilizing the $Q_{[N]}$ and $OUT_{[N]}$ nodes at V_L.

According to the above operation, the rising time of the output waveform is ameliorated by increasing the voltage of the $Q_{[N]}$ node to V_{DD} before the $OUT_{[N]}$ node is charged. Furthermore, before the $OUT_{[N]}$ node is discharged, the voltage of the $C_{[N]}$ node can also be raised to V_{DD} so that the voltage of the $Q_{[N]}$ node is maximized, reducing the falling time of the output waveform. Consequently, the driving ability of T5 is ameliorated without increasing the size of the TFT, and the proposed gate driver is suitable for high-resolution displays.

III. RESULTS AND DISCUSSION

The electrical characteristics of the fabricated a-Si:H TFTs with different aspect ratios (μm/μm) are obtained using a Keithley 2612A source meter. Fig. 3 plots the transfer curves and established TFT models of an HSPICE simulator (Rensselaer Polytechnic Institute a-Si TFT model, level = 61) with a gate-to-source voltage of −15 V to 25 V and the drain-to-source voltages of 1 V and 10 V. The threshold voltage is 3 V and the mobility is 0.2 $cm^2/V{\cdot}s$.

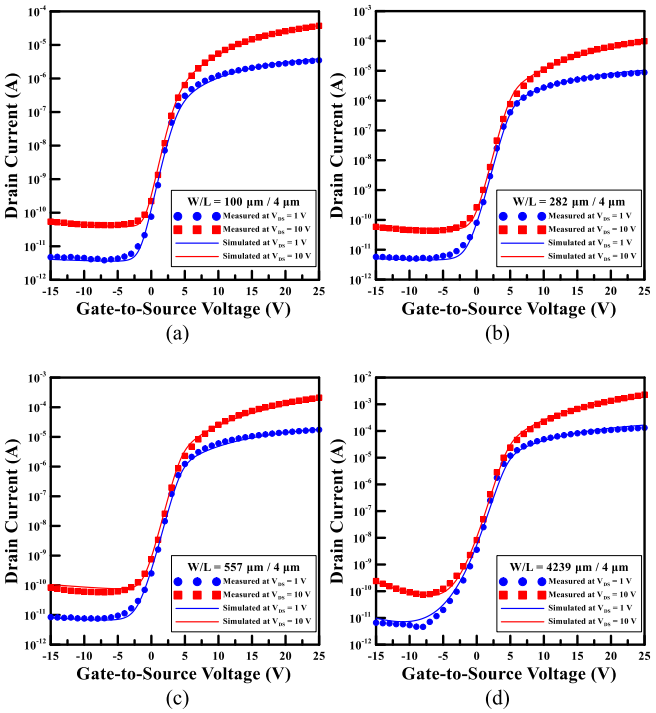

FIGURE 3. Measured and simulated transfer curves of a-Si:H TFTs with different aspect ratios. (a) 100 μm / 4 μm. (b) 282 μm / 4 μm. (c) 557 μm / 4 μm. (d) 4239 μm / 4 μm.

TABLE 1. Designed parameters of proposed gate driver.

Parameter	Value
V_{DD}	20 V
V_L	-12 V
CK1~CK4	-12 V ~ 15 V
$(W/L)_{T1 \cdot T2 \cdot T6 \cdot T8 \cdot T9}$	100 μm/ 4 μm
$(W/L)_{T3 \cdot T4}$	557 μm/ 4 μm
$(W/L)_{T5}$	4239 μm/ 4 μm
$(W/L)_{T7 \cdot T10 \cdot T11}$	282 μm/ 4 μm
C1	0.2 pF
C2	2.7 pF
C3	1.2 pF

To evaluate the performance of the proposed gate driver based on the specification of a 5.99 inch HD + (720 × 1440) panel, the RC loadings of the gate line and the clock signals are respectively set to 2.1 kΩ and 80 pF. The pulse width of the clock signals is set to 20 μs and the duty cycle is 45.5% when the pre-charging method is applied to the 120Hz frame-rate panel [4]. Table 1 lists the design parameters, which include the voltage of V_{DD}, the voltage swings of CK1-CK4, capacitance, and the aspect ratios of the TFTs. Fig. 4 plots the simulated waveforms of the clock signals, and nodes in the proposed gate driver, which includes the output nodes from [N-2]th-[N+2]th stages, as well as $K_{[N]}$, $Q_{[N]}$, $K_{[N+2]}$, $C_{[N]}$, and $P_{[N]}$ nodes. When the voltage

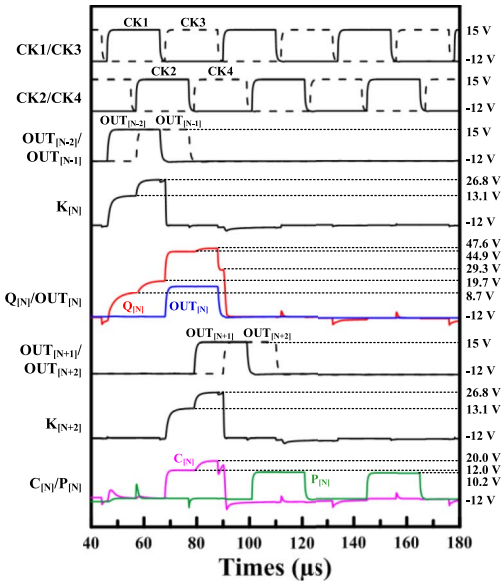

FIGURE 4. Simulated waveforms of clock signals, output nodes from [N-2]th-[N+2]th stages, as well as $K_{[N]}$, $Q_{[N]}$, $K_{[N+2]}$, $C_{[N]}$, and $P_{[N]}$ nodes.

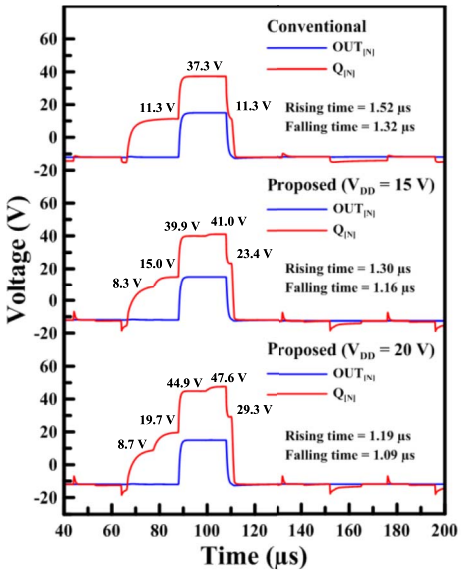

FIGURE 5. Comparison of waveforms of $Q_{[N]}$ and $OUT_{[N]}$ nodes between conventional structure and proposed structure with different voltage levels of V_{DD}.

of the $OUT_{[N-2]}$ node changes from −12 V to 15 V, the $K_{[N]}$ node is charged to 13.1 V, and the $Q_{[N]}$ node is charged to 8.7 V. Next, the $OUT_{[N-1]}$ node goes to 15 V, and the voltage of the $K_{[N]}$ node is increased to 26.8 V by the bootstrapping effect of C1 so the voltage of the $Q_{[N]}$ node can be increased to 19.7 V before the $OUT_{[N]}$ node is charged. Thus, the $OUT_{[N]}$ node can be charged to 15 V at high speed, and the $Q_{[N]}$ node is bootstrapped to 44.9 V by C2 and the parasitic capacitance of T5. Before the $OUT_{[N]}$ node is discharged, the voltage of the $C_{[N]}$ node increases from 12.0 V to 20.0 V so that of the $Q_{[N]}$ node is further increased to 47.6 V. As CK3 returns to −12 V, the $OUT_{[N]}$ node can be rapidly discharged to −12 V through T5 with the maximum driving ability because the $Q_{[N]}$ node is at its highest voltage. Afterward, the voltage of the $P_{[N]}$ node is periodically raised to 10.2 V through C3 as CK2 switches from −12 to 15 V, with the voltages of the $Q_{[N]}$ and $OUT_{[N]}$ nodes held at −12 V.

Fig. 5 compares the waveforms of the $Q_{[N]}$ and $OUT_{[N]}$ nodes between the conventional structure and the proposed structure with different voltages of V_{DD}. Before the $OUT_{[N]}$ node starts to be charged, the voltage of the $Q_{[N]}$ node in the conventional structure is only at 11.3 V. However, in the proposed structure, the $Q_{[N]}$ node is charged to 15.0 V and 19.7 V when V_{DD} is set to 15 V and 20 V, respectively. Therefore, the rising time of the output waveform can be reduced from 1.52 μs to 1.30 μs and 1.19 μs, respectively. However, during the discharging of the $OUT_{[N]}$ node, the voltage of the $Q_{[N]}$ node in the conventional structure is decreased from 37.3 V to 11.3 V, whereas, in the proposed structure, the $OUT_{[N]}$ node starts to be discharged with the $Q_{[N]}$ node at 41.0 V, and the discharging ends with the $Q_{[N]}$ node at 23.4 V when V_{DD} is 15 V. With V_{DD} at 20V, the voltage of the $Q_{[N]}$ node is reduced from 47.6 V to 29.3 V so the falling time of the output waveform can be reduced from 1.32 μs to 1.09 μs. Owing to the multiple bootstrapping steps, the gate voltage during the generation of the gate pulse is increased from 37.3 V to 44.9 V and 47.6 V when V_{DD} is set to 20 V in the proposed structure. The reliability of the driving TFT is verified by the accelerated life time test at 70 °C with the driving signals generated from the external circuit. Figs. 6(a) and 6(b) show the measurement setup of the reliability test, the driving signals for the drain and gate nodes of the driving TFT, and the measured waveform of the source node. Notably, driving signals for the drain and gate nodes are designed to make the gate-source or gate-drain voltages of the driving TFT be larger or equal to the voltage according to the simulated results. Fig. 6(c) plots the measured waveforms of the output node during the reliability test for 240 hours, remaining almost identical throughout the test and confirming the reliability of the driving TFT with high gate voltages. To demonstrate the efficiency of the proposed structure, Fig. 7 shows the changes of rising and falling times as the channel of the driving TFT in the conventional structure is widened. The channel widths of the driving TFT need be increased from 4239 μm to 5935 μm and 5723 μm, respectively, to approach the charging and discharging speeds in the proposed structure with 15V V_{DD}. Furthermore, when 20V V_{DD} is used in the proposed structure, the channel widths of the driving TFT in the conventional structure need be further increased to 7630 μm and 6782 μm, respectively.

Figs. 8(a) and 8(b) plot the improvements of the rising and falling times with different pulse widths of the clock signals, verifying the feasibility of the proposed gate driver for use in higher frame-rate applications. As shown in Fig. 8, when

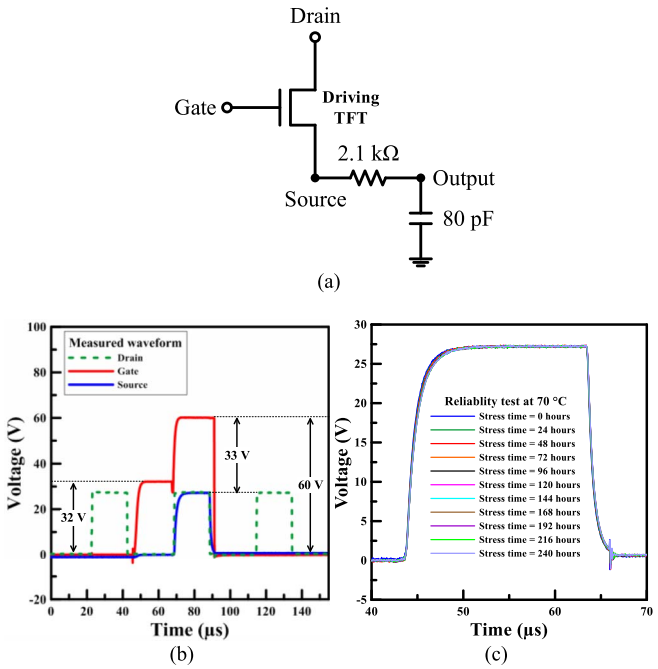

FIGURE 6. (a) Measurement setup of reliability test. (b) Driving signals for drain and gate nodes of driving transistor and measured waveform of source node. (c) Measured waveforms of output node during reliability test for 240 hours.

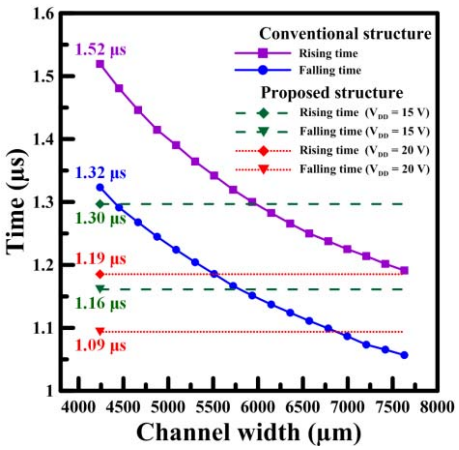

FIGURE 7. Comparison of rising and falling times of gate drivers with conventional and proposed structures.

V_{DD} of the proposed gate driver is set to only 15 V, and the pulse width of the clock signals is set to 40 μs, 20 μs, 10 μs, and 5 μs, the rising time of the output waveforms is improved by 13%, 15%, 17%, and 22%, respectively. Moreover, when V_{DD} is modulated from 15 V to 20 V, the rising time can be further improved to 21%, 22%, 23%, and 27%. Notably, the improvement increases as the pulse width is shortened from 40 μs to 5 μs. Similarly, modulating the voltage of V_{DD} improves the falling time by more than 16% as the pulse width falls from 40 μs to 10 μs and by 21% when the pulse width is shortened further to 5 μs.

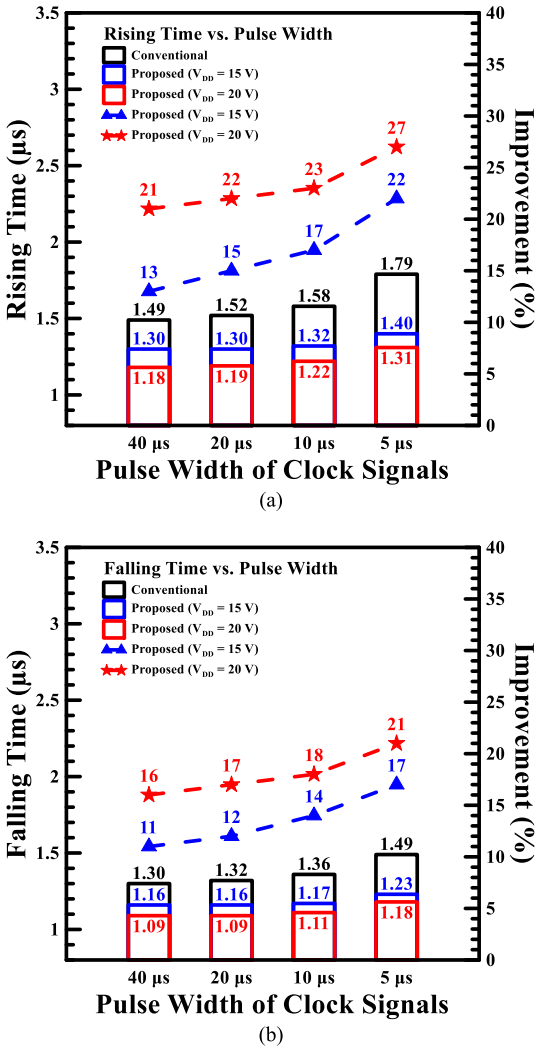

FIGURE 8. Improvements with different pulse width of clock signals as RC loadings are 2.1 kΩ and 80 pF. (a) Rising time. (b) Falling time.

With respect to the high-resolution panels, Figs. 9(a) and 9(b) plot the improvements of the rising and falling times as the RC loadings of the gate line and clock signals are increased from 2.1 kΩ and 80 pF to 2.1 kΩ and 160 pF. As shown in Fig. 9, when the pulse width of clock signals is larger than 10 μs and V_{DD} is set to 15 V, the rising and falling times are still improved by more than 10% and 11%, respectively. When V_{DD} is modulated to 20 V, the rising and falling times can be further improved by more than 18% and 16%, respectively. When the pulse width of clock signals is shortened from 10 μs to 5 μs, the rising and falling times of the conventional structure are dramatically increased from 3.07 μs to 4.37 μs and from 2.68 μs to 3.41 μs, respectively, because the pulse width is short and the loadings are large. However, by using a V_{DD} of 20 V, the proposed method reduces the rising and falling times to 2.88 μs and 2.43 μs, respectively, presenting improvements of 34% and 29%. These analytical results establish the feasibility of the generation of a much smaller

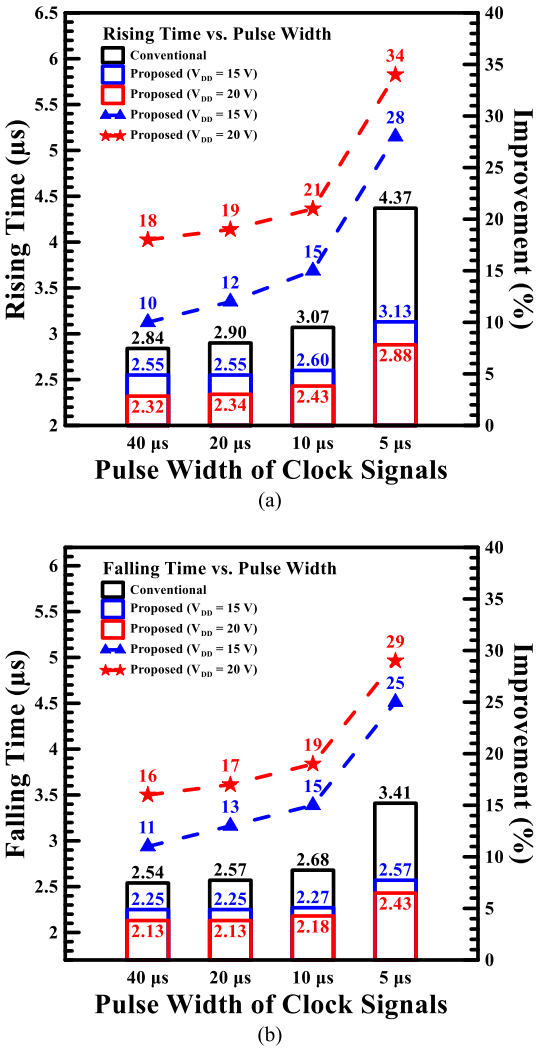

FIGURE 9. Improvements with different pulse width of clock signals as RC loadings are 2.1 kΩ and 160 pF. (a) Rising time. (b) Falling time.

gate pulse using the proposed gate driver, and this method is highly promising for use in high-resolution applications.

IV. CONCLUSION

This work presents a new capacitive coupling method to enlarge the gate voltage of a-Si:H TFTs to improve the performance of gate drivers. Since the high voltage of a global power source line can be entirely transferred to the gate node of the driving TFT of the gate driver, the reductions of the rising and falling time of the output waveforms are related to the settings of V_{DD}. Consequently, the analytical results that are based on the measurements of fabricated a-Si:H TFTs show that the driving capability of the gate driver is enhanced by more than 21% at a V_{DD} of 20 V when the pulse width of the clock signals is only 5 μs, which is suitable for high-resolution displays.

ACKNOWLEDGMENT

AU Optronics Corporation is appreciated for its technical and funding support.

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