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Effects of Fluorine on the NBTI Reliability and Low-Frequency Noise Characteristics of p-MOSFETs

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ABSTRACT The concurrent effect of fluorine implantation with various energy and dose on reliability and low-frequency noise characteristics of p-MOSFETs was investigated. The ΔV_T degradation that represents device lifetime of p-MOSFETs with fluorine implantation under negative-bias temperature instability stress was less than that without fluorine implantation. The device lifetimes were improved as the fluorine implantation energy and dose increase. The power law exponent n with the fluorine implantation was larger than that without fluorine implantation. This was related to boron diffusion within the gate oxide because the F atoms enhance the diffusivity of the boron. The difference of flicker noise levels between simulation and measurement data at 1 kHz was much greater than that at 10 Hz, which means that F atoms were mainly located near the Si/SiO_2 interface rather than in the bulk oxide. The fluorine implantation reduced the I_D-RTS noise amplitude, which was believed to contribute to the effective passivation of the dominant traps within the gate oxide. Also, the flicker noise was less dependent on implantation energy. But, flicker noise was reduced with increasing implantation dose. Therefore, fluorine implantation is potentially significant for reducing low-frequency noise as well as improving reliability characteristics.

INDEX TERMS Fluorine (F), activation energy (Ea), negative bias temperature instability (NBTI), low-frequency noise (LFN), random telegraph signal (RTS) noise.

I. INTRODUCTION

As device dimensions of complementary metal oxide semiconductor field effect transistors (CMOSFETs) are scaled down, the reliability of the gate dielectric and the occurrence of low-frequency noise, which mainly determine the performance of analog mixed-signal (AMS) and radio frequency (RF) circuits, have become important issues [1], [2]. In particular, the allowable amplitude of low frequency noise is expected to become much lower in AMS and RF applications, because the decrease in low-frequency noise is crucial to improving the margin for circuit design. This allows that an adequate signal-to-noise ratio (SNR) can be maintained, and the minimum input signal of amplifiers can be extended when designing high-performance AMS/RF circuits [2]. Therefore, several research efforts have been undertaken to improve low-frequency noise characteristics in AMS and RF devices [3], [4]. The low-frequency noise has generally been thought to be related to traps near the gate dielectric interface that are caused by various factors such as temperature, doping, impurities, quality of the gate dielectric, *etc.* [2], [4]. Also, thinner gate dielectrics cause many serious reliability problems such as negative-bias temperature

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instability (NBTI), interface state generation, *etc.* [4]. Since, both the low frequency noise and the reliability characteristics are related to defects within gate oxide [5]. Therefore, the low-frequency noise has been used as a diagnostic tool for understanding processes and mechanisms affecting device reliability. The low-frequency noise also constitutes a critical technology parameter [6]. It can be used to determine the quality of the gate stack when the sources of the current fluctuations are charge trapping/de-trapping events [7], [8]. To solve these problems, incorporating fluorine (F) into the gate oxide has been suggested and investigated because F atoms that diffuse into the gate dielectric react with the silicon dangling bonds within the gate dielectric, and these passivate the traps at the Si/SiO_2 interface [9]–[13]. Also, *Si-F* bonds are less likely to be broken than *Si-H* under electrical and thermal stress because of their higher binding energy [9]–[13]. Although the NBTI reliability and low-frequency noise characteristics realized by incorporating fluorine have been reported separately [12]–[16], there was little report on the concurrent effect of fluorine ion implantation on the NBTI reliability and low-frequency noise. Therefore, the effect of the fluorine on the low frequency, as well as NBTI reliability, needs to be analyzed.

In this paper, hence, the concurrent effects on NBTI reliability and low-frequency noise characteristics caused by incorporating fluorine are investigated by varying the implant dose and energy of fluorine. Moreover, the optimization of the fluorine energy and dose to improve NBTI reliability and low-frequency noise characteristics while minimizing the impact of fluorine on other electrical parameters.

II. FABRICATION AND EXPERIMENT

P-channel FETs were fabricated using standard 0.18 μm CMOS technology on 8" (100) p-type silicon substrates. Shallow trench isolation (STI), retrograde twin well, and gate oxide processes were applied sequentially. After patterning the poly-Si gate electrode, fluorine was implanted. The dose and energy of fluorine ion implantation were varied to optimize the effect of fluorine incorporation on reliability and low-frequency noise characteristics. The energy (E) was split into E, 1.25E and 1.5E and the dose (D) was split into D, 1.5D and 2D (1.5E means 1.5 times greater energy than E and 2D means 2 times greater dose than D.). The implantation energy and dose are expressed as relative magnitudes because the exact condition of implantation cannot be disclosed. The maximum fluorine concentration in the gate oxide was estimated by SIMS measurement to be 1.0×10^{20} atom/cm^3. Forming gas annealing was applied to all wafers at 400 °C. A device without fluorine ion implantation was also fabricated as a reference. The normalized stress bias ($V_G - V_T$ where gate voltage, V_G and threshold voltage, V_T) was applied to the gate for the constant stress electric field among the wafers. Because the fluorine incorporation effect causes the slight change in gate oxide thickness as a result of oxygen atoms being released during the *Si-F* bond formation and re-oxidizing at the Si/SiO_2 interface [10]. The device lifetimes are defined as the point where the increase of threshold voltage, ΔV_T becomes 50 mV. The noise measurement system is consisted of a semiconductor parameter analyzer, a dynamic signal analyzer, and a low noise current preamplifier [17]. The flicker noise characteristics were measured at $V_D = 1.65V$, and $V_G = V_T + 0.4V$. Then the noise PSD at 100Hz was sampled to compare each split. The RTS noise measurements were carried out in the linear regime at the constant drain voltage $V_D = 0.1V$ and ate the gate voltage where the drain current, I_D becomes 1μA.

III. FLICKER NOISE MODEL

Flicker noise is found to exist in various electronic systems. In general, flicker noise is commonly called as 1/f noise, because the power spectrum of flicker noise is proportional to the inverse of frequency. That is the power spectrum density can be expressed as

$$S_{I_d}(f) = \frac{\text{constant}}{f^{EF}} \tag{1}$$

where the exponent EF varies within 0.7~1.3 as shown in Fig. 1 [18]. There exist several physical models explaining 1/ f noise. McWhorter model explains that 1/ f is originally due to the carrier number fluctuation (Δn) in channel caused by trapping/de-trapping of carrier [19]. Hooge model, on the other hand, proposes that noise is from mobility fluctuation ($\Delta\mu$), due to carriers scattered by phonons [20]. Hung *et al.* [21] proposed a unified model to fit experimental data. As all cases were supported by experimental data, the source of 1/f noise still remains unclear.

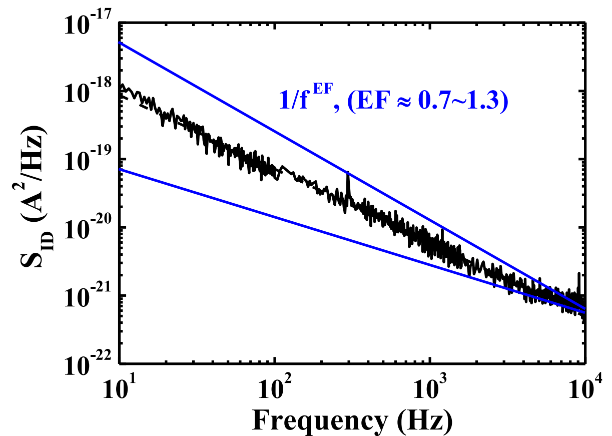

FIGURE 1. Typical power spectrum density of 1/f noise (black line) and the eligible range of flicker noise exponent distribution (blue line).

BSIM 3v3 (level 49 in HSPICE) were applied for short-channel devices in the simulations. Then, the noise characteristics were simulated by choosing the appropriate noise equation selector (NLEV = 2&3), flicker noise exponent, and flicker noise coefficient in SPICE. The flicker noise model with the drain noise current spectral density proportional to g_m^2,

$$S_{I_d}(f) = \frac{KF\, g_m^2}{C_{OX} W_{eff} L_{eff} f^{EF}} \tag{2}$$

where S_{Id} is the drain noise current spectral density, KF is the flicker noise coefficient, EF is the flicker noise exponent ($\approx$ 0.7~1.3), g_m is transconductance and W_{eff} and L_{eff} is effective channel width and length, respectively. Then the simulation results were compared with the experimental data to implement trap contributions.

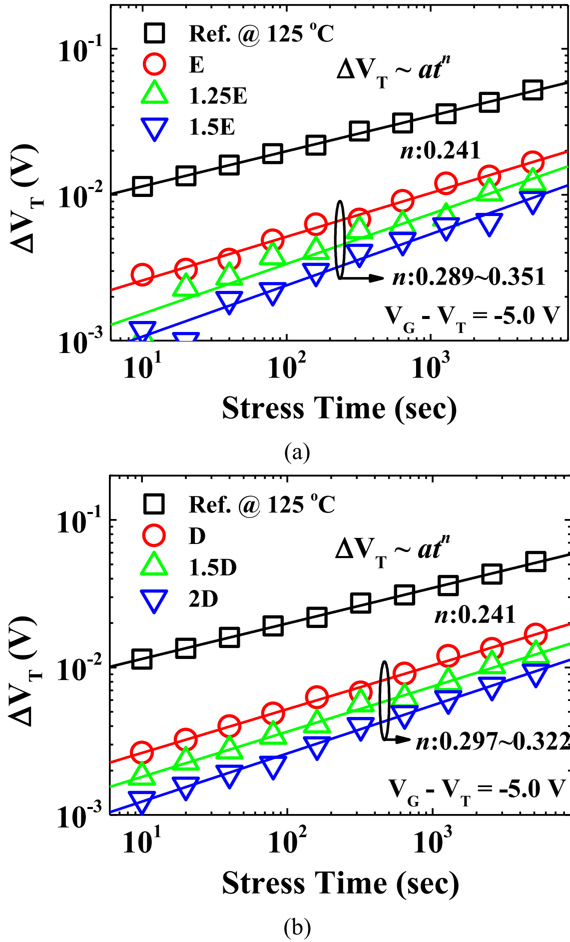

FIGURE 2. Dependence of threshold voltage degradation (ΔV_T) on (a) fluorine implantation energy, and (b) implantation dose induced by negative bias instability (NBTI) stress. The power law time dependency of ΔV_T degradation with fluorine implantation is different from that without fluorine implantation.

IV. RESULTS AND DISCUSSION

The effect of fluorine incorporation on threshold voltage degradation (ΔV_T) under NBTI stress at constant stress voltage of $V_G - V_T = -5.0$ V is shown in Fig. 2. Fluorine-implanted devices show much less ΔV_T degradation than devices without fluorine implantation. The time dependency of the ΔV_T degradation can be described by a power law expression: $\Delta V_T \sim t^n$. The exponent n without fluorine implantation is 0.241, which is similar to the general NBTI degradation mechanism as previously reported because n is close to 0.25 [22]. However, it is quite interesting that the exponent n with fluorine implantation is in the range of 0.297~0.322 which mean that dominant degradation mechanism in devices with fluorine implantation is different from the mechanism in those without fluorine implantation. These results suggest that boron diffuses within the gate oxide because fluorine enhances the diffusivity of the boron, resulting in the generation of positive oxide defects in the gate dielectric, while the interface traps are suppressed [10]–[12]. Device lifetimes with fluorine implantation are longer than those of devices without fluorine implantation. As shown in Fig. 3, device lifetimes also increase with the increase of implantation energy and/or dose.

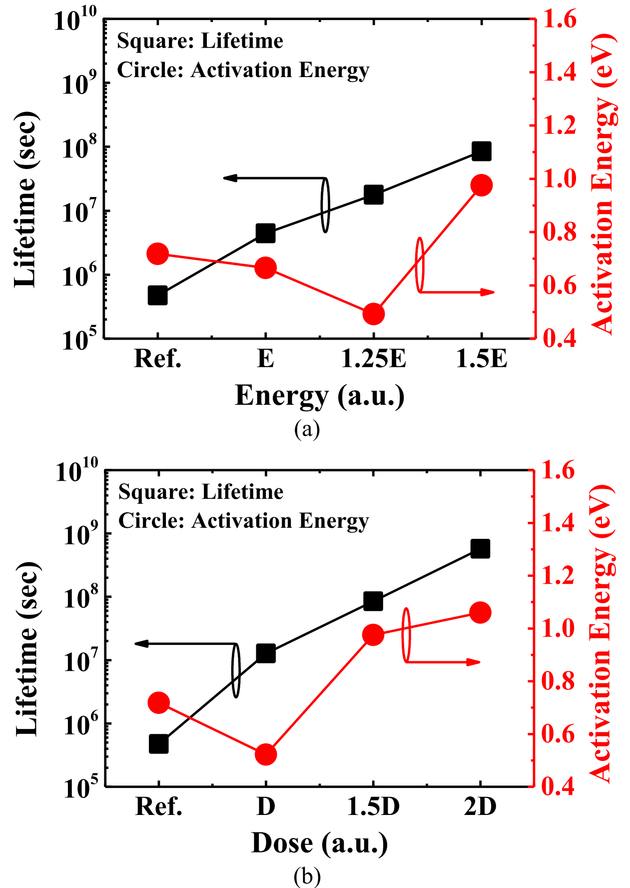

FIGURE 3. Device lifetime (black square) and activation energy (red circle) under NBTI stress as a function of (a) fluorine implantation energy, and (b) implantation dose. Device lifetimes with the fluorine implantation are greater than without fluorine implantation.

The improvement in device lifetimes can be explained by the fact that F atoms in the gate oxide replace *Si-O* and/or *Si* dangling bonds with *Si-F* during the fluorine implantation and that *Si-H* (3.18 eV) bonds are more breakable than *Si-F* (5.73 eV) under NBTI stress [9]–[13], as depicted in Fig. 4. Hence, it takes longer to break them, which can improve device lifetime and suppress the generation of interface traps at the SiO_2/Si interface due to a high binding energy. In addition, it may be necessary to analyze the activation energy to investigate the dominant degradation. It is

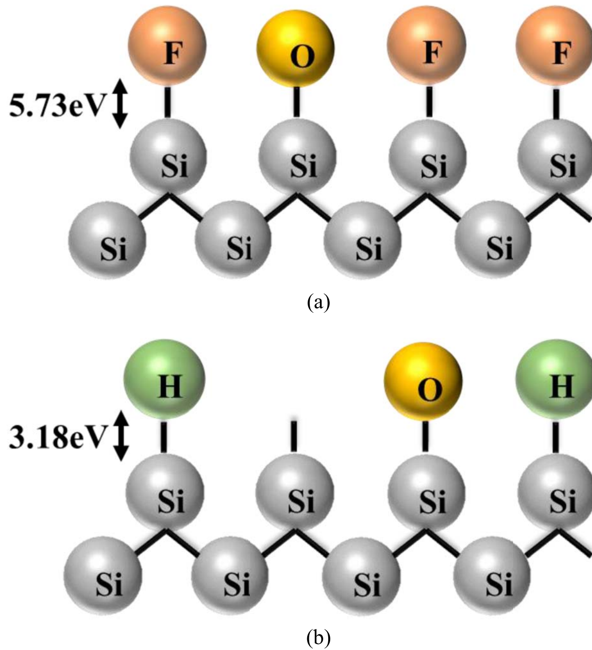

FIGURE 4. Illustration of the Si/SiO_2 interface bonding structure: (a) passivated interface with fluorine atoms; (b) passivated interface with hydrogen atoms. *Si-H* bonds breaks easier than *Si-F* bonds under stress condition.

interesting that the activation energy of devices with low fluorine implantation energy or low dose is lower than that of devices without the fluorine implantation; this may be related to the effect of boron within the gate oxide as mentioned earlier. Therefore, it is necessary to analyze and evaluate the effect of incorporating fluorine on the reliability and activation energy before applications to CMOS AMS and RF technology can be considered.

A normalized drain current noise power spectral density (S_{ID}/I_D^2) with and without fluorine implantation for various doses and energies is shown in Fig. 5. The normalized drain current noise without the fluorine implantation are almost consistent with HSPICE simulation data even though the experimental data shows a slightly higher PSD in the 10 Hz region. On the other hand, the reduction of the measured flicker noise by fluorine implantation compared with the HSPICE simulation at 1 kHz is much greater than that at 10 Hz, which means that F atoms are mainly located near the Si/SiO_2 interface rather than in the bulk oxide [2], [4].

Although the reduction of flicker noise depends on the fluorine implantation dose at the same energy as shown in Fig. 5(b) and 6(b), the improvement of flicker noise with the fluorine implantation energy at the same dose is not observed as shown in Fig. 5(a) and 6(a). In any event, the fluorine implantation within the gate oxide still has a beneficial effect on the flicker noise characteristics.

The relative variation of I_D-RTS noise amplitude ($\Delta I_D/I_D$) with and without fluorine implantation for various energies and doses is shown in Fig. 7. The I_D-RTS noise amplitude without fluorine implantation is much greater than that with

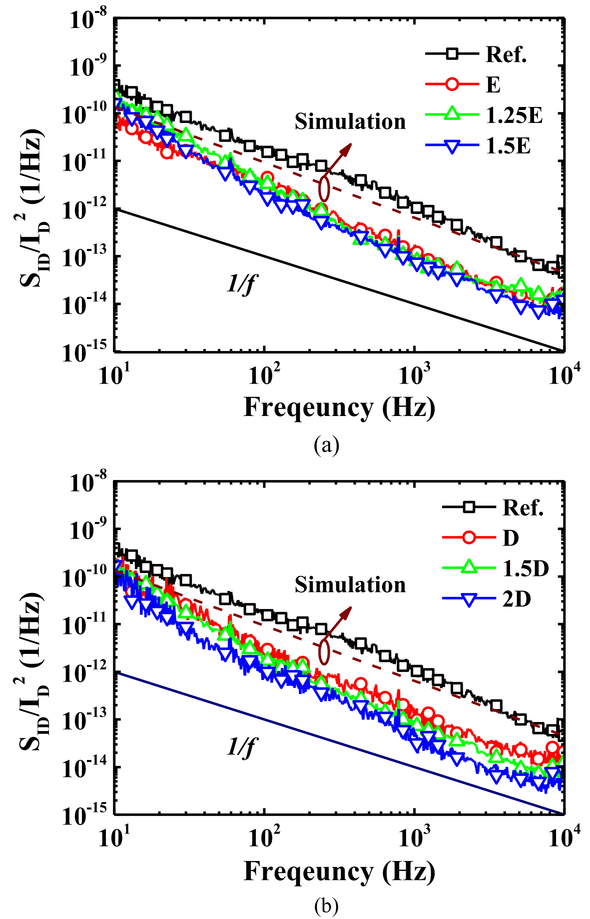

FIGURE 5. Dependence of normalized drain current noise power spectral density (S_{ID}/I_D^2) on (a) fluorine implantation energy and (b) fluorine implantation dose, compared with HSPICE simulation data (Dashed line).

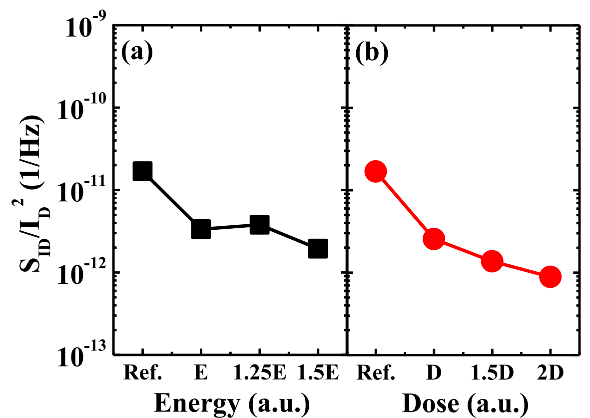

FIGURE 6. (a) Normalized drain current noise power spectral density (S_{ID}/I_D^2) at 100 Hz as a function of (a) fluorine implantation energy, (b) fluorine implantation dose. Reduction of the flicker noise is dependent on the fluorine implantation dose.

any amount of fluorine implantation. Interestingly, however, the differences in the I_D-RTS noise amplitude as a function of the fluorine implantation energy and as a function of the dose are similar to each other. The reduction of I_D-RTS noise

amplitude with the fluorine implantation at an average point is about 50%. This I_D-RTS noise amplitude can be related to the dominant trap depth within the gate oxide [4]. That is, the active traps for single-carrier trapping/de-trapping centers are distributed near the Si/SiO_2 [4]. Hence, the fluorine implantation can effectively passivate the dominant traps within the gate oxide as well as the interface traps.

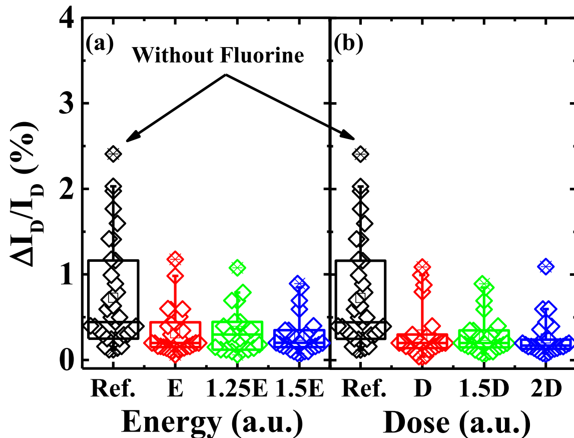

FIGURE 7. Relative variation of I_D-RTS noise amplitude ($\Delta I_D/I_D$) in box chart as a function of (a) fluorine implantation energy, (b) fluorine implantation dose.

V. CONCLUSION

In this paper, the concurrent effect of incorporating fluorine on reliability and low-frequency characteristics of p-MOSFETs were investigated. The ΔV_T degradation under NBTI stress of the devices with fluorine implantation was less than in the case of those without fluorine implantation. The dominant degradation mechanism between devices with and without fluorine implantation was different; this was related to the effect of boron diffusion within the gate oxide. Device lifetimes with fluorine implantation were greater than without fluorine implantation. The reduction or difference in measured flicker noise with fluorine implantation compared with HSPICE simulation data at 1 kHz was greater than at 10 Hz, which meant that F atoms were mainly located near the Si/SiO_2 interface and the interface traps were passivated by F atoms. Finally, the fluorine implantation reduced the I_D-RTS noise amplitude, which is believed to be attributed to the effective passivation of the dominant traps within the gate oxide as well as the interface traps. Therefore, the effects of incorporating fluorine on the low-frequency noise characteristics are one of the key points of this paper. These results are potentially significant and essential for CMOS AMS and RF applications.

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