Received 31 March 2018; revised 26 May 2018; accepted 14 June 2018. Date of publication 25 June 2018; date of current version 24 July 2018.
The review of this paper was arranged by Editor C. C. McAndrew.

*Digital Object Identifier 10.1109/JEDS.2018.2850063*

# An Investigation of Anode Hole Injection-Induced Abnormal Body Current in n-Channel $HfO_2$/TiN MOSFETs

**JIH-CHIEN LIAO[1], TING-CHANG CHANG[2] (Senior Member, IEEE), WEI-REN SYONG[2], KAI-CHUN CHANG[2], YING-HSIN LU[2], HSI-WEN LIU[2], CHIEN-YU LIN[3], LI-HUI CHEN[3], FU-YUAN JIN[2], YU-HSUAN CHEN[1], CHEN-HSIN LIEN[1], OSBERT CHENG[4], CHENG-TUNG HUANG[4], AND YI-HAN YE[4]**

1 Department of Electronics Engineering, National Tsing-Hua University, Hsinchu 30013, Taiwan
2 Department of Physics, National Sun Yat-sen University, Kaohsiung 80424, Taiwan
3 Department of Photonics, National Sun Yat-sen University, Kaohsiung 80424, Taiwan
4 Device Department, United Microelectronics Corporation, Tainan 744, Taiwan

CORRESPONDING AUTHORS: T.-C. CHANG AND C.-H. LIEN (e-mail: tcchang3708@gmail.com; chlien@ee.nthu.edu.tw)

This work was supported in part by the Ministry of Science and Technology (MOST) Core Facilities Laboratory for Nano-Science and Nano-Technology in Kaohsiung-Pingtung Area and in part by the Ministry of Science and Technology, Taiwan, under Contract MOST-106-2112-M-110-008-MY3 and Contract MOST 107-2622-8-110-003-TE1.

**ABSTRACT** This paper investigates an anode hole injection (AHI)-induced abnormal body current (abn $I_B$) in n-channel $HfO_2$/TiN MOSFETs. Traditionally, body current is independent of gate voltage during initial electrical characteristic measurements. Nevertheless, in this paper, the opposite is found in our experiment. Therefore, two different measurement techniques are employed, with the body current attributed to electrons in the inversion layer under the grounded source/drain. This indicates that the dominant mechanism is AHI rather than electron tunneling from the valence band. Moreover, the abn $I_B$ is dominated by tunneling mechanisms because it is independent of temperature.

**INDEX TERMS** Body current, anode hole injection, MOSFET.

## I. INTRODUCTION

As metal oxide semiconductor field-effect transistors (MOSFETs) scale down, traditional $SiO_2$-based dielectrics are only a few atomic layers in thickness, resulting in increased gate leakage current, increased power dissipation, and reduced performance. To overcome these problems, conventional $SiO_2$ gate dielectrics are being replaced by high-k dielectric, specifically $HfO_2$ gate dielectric [1]. In addition, high-k gate dielectrics can be integrated with strained silicon, a silicon-on-insulator (SOI) structure, and fin field-effect transistor (FinFET) devices [2]–[4]. At present the FinFET is one promising structure because of its excellent overall performance as well as the gate control ability which suppresses short-channel effects. In this letter, we investigate the anode hole injection-induced abnormal body current (abn $I_B$) in n-channel $HfO_2$/TiN MOSFETs. In general, body current is an indicator of reliability and can be used to predict the lifetime of a device, as the impact ionization current is generated near the drain side when the device is operated in the saturation region [5]. In addition, when the transistor is turned off and $V_{GD} < -1V$, the generation of electron-hole pairs is caused by band-to-band tunneling (BTBT), and the body current and drain current increases are termed gate-induced drain leakage (GIDL) current [6]. However, the abnormal body current we note operates in the linear region, unlike the case explained above. Further details will be explained later.

## II. EXPERIMENT

The $HfO_2$/TiN n-FinFETs used in this letter were fabricated by 16 nm technology with a gate-last process. To begin, high quality 1 nm thermal oxide was grown as an interfacial layer for the core device. Then 2 nm of $HfO_2$ dielectric was deposited by atomic layer deposition (ALD). Furthermore, after the deposition of the $HfO_2$, the process was divided into two parts: one group was annealed at high temperature in $N_2$ ambient (normal devices), while the other was not annealed (abnormal current devices). Finally, work function metal (WFM) layers of TiN were deposited by ALD. In this work, the dimensions of devices were width = 154 nm and

2168-6734 © 2018 IEEE. Translations and content mining are permitted for academic research only.
Personal use is also permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

length = 20, 38, 60, 80, and 100 nm. Figure 1(a) shows the structure of a FinFET device. A cross-section of corresponding point A to A′ in this FinFET 3D structure is shown in Figure 1(b). All experimental curves were measured using an Agilent B1500 semiconductor parameter analyzer and a Cascade M150 probe station.

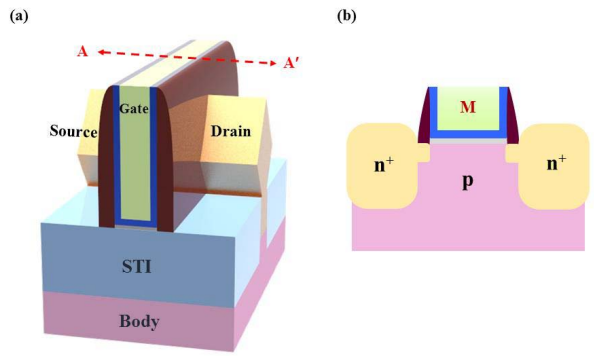


**FIGURE 1. (a) The structure of a FinFET device. (b) A cross-section of corresponding point A to A′ in the FinFET 3D structure.**

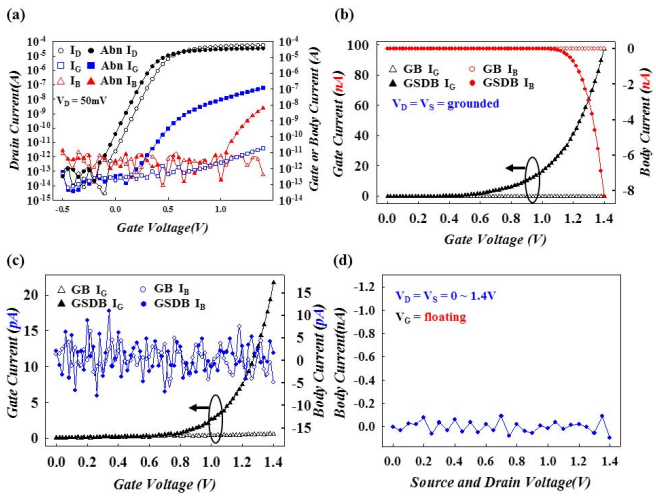


**FIGURE 2. (a) $I_D - V_G$, $I_G - V_G$, and $I_B - V_G$ log-scale curve at linear region measurement for abnormal current/normal devices. $I_G - V_G$ and $I_B - V_G$ electrical characteristics under grounded and floating S/D operations for (b) abnormal current device and (c) normal device. (d) IB-VS/D electrical characteristics under floating gate operation.**

## III. RESULT AND DISCUSSION

Figure 2(a) shows the drain current-gate voltage ($I_D - V_G$), gate current-gate voltage ($I_G - V_G$), and body current-gate voltage ($I_B - V_G$) log-scale curve at the linear region ($V_D$ = 50mV). The $I_D - V_G$ curves indicate that the subthreshold swing (S.S.) of both devices are similar, as would be expected for initial electrical characteristics. However, when $V_G > V_T$ an inversion n-channel is formed, $I_G$ increases significantly as the $V_G$ rises in the abnormal current devices, which have more bulk traps in the $HfO_2$. Additionally, abnormal $I_B$ can be clearly observed at high $V_G$ in the linear region measurement. Figure 2(b) shows the abnormal $I_B$ measured at $V_G = 0 \sim 1.4$ V with grounded source, drain, and body (GSDB) for abnormal current devices. Clearly, an increase in gate current ($I_G$), causes a significant enhancement in $I_B$, which means that the source of $I_B$ is strongly dependent on $I_G$. In general, $I_B$ is independent of gate voltage in initial electrical characteristics, and usually appears as shown in Figure 2(c). Therefore, to clarify whether the PN junction leakage contributes to the abnormal $I_B$, measurements are made with grounded body and floating gate at $V_{S/D} = 0 \sim 1.4$ V, as shown in Figure 2(d). Clearly, the PN junction current is smaller than abnormal $I_B$, so this abnormal $I_B$ is not affected by the PN junction leakage.

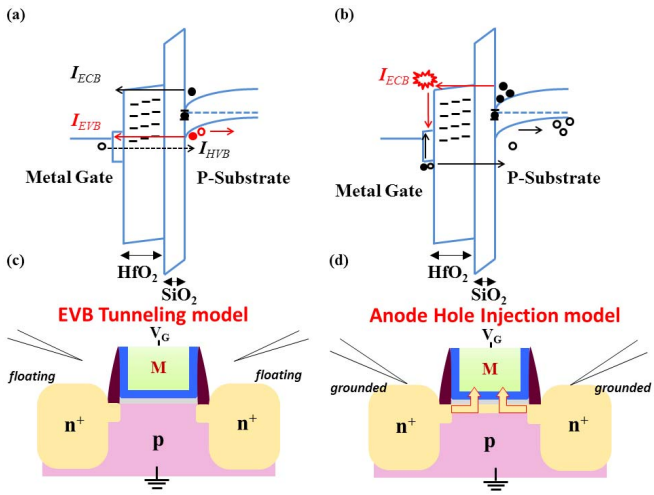


**FIGURE 3. (a)(b) The band diagrams of HVB, EVB, and ECB models for high-k metal gate n-FinFETs. (c)(d) The device under floating and grounded S/D operations.**

To further investigate the mechanism of abnormal $I_B$, we investigate models used in previous reports [7]–[10], which have proposed that the significant tunneling current components of the poly-Si gate are hole tunneling from the valence band (HVB), electron tunneling from the valence band (EVB), and electron tunneling from the conduction band (ECB), as shown in Figure 3(a). One of these gate leakage currents is likely to be the main cause of abnormal $I_B$. First, the HVB model can be eliminated because the TiN metal gate has fewer holes in the FinFET structure. Second, the band diagram of EVB indicates the electrons tunnel from the valence band of the Si substrate to the TiN metal gate. The remaining holes collect in the substrate. The EVB model may, then, explain the cause. Third, Figure 3(b) shows the electrons tunneling from the inversion layer to the metal gate (anode), and generating electron-hole pairs by impact ionization at the $HfO_2$/metal interface; these holes can then inject to the body (cathode); this model is similar to anode hole injection (AHI) [8], which corresponds to ECB in previous reports [7]. The EVB and AHI mechanisms generate holes that contribute to body current; however, an important difference between the EVB and the AHI model

is the source of electrons. In the EVB model, the electrons come from the valence band, but the electrons come from the conduction band under the AHI model. Therefore, two operation conditions which can be used to distinguish the different sources of electrons are floating (GB) and grounded (GSDB) source/drain (S/D) operations, schematics of which are shown in Figure 3(c) and (d). Because the S/D cannot supply sufficient electrons to the inversion layer under GB operation, the gate leakage current becomes insignificant, as shown in Figure 2(b). Similarly, the $I_B$ is negligible in this operation. In contrast, both currents show very pronounced increases under GSDB operation. These results demonstrate that the origin of abnormal $I_B$ can be attributed to the electrons in the inversion layer rather than the electron-hole pairs separated in the valence band of the substrate. Consequently, the AHI model is confirmed to be the dominant mechanism contributing to abnormal $I_B$.

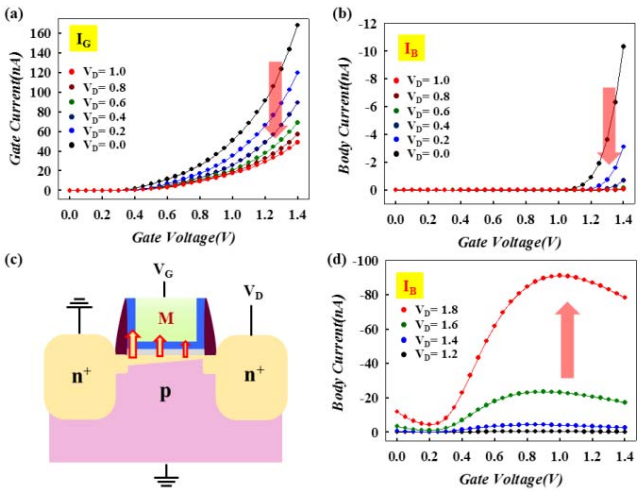


**FIGURE 4. (a) $I_G - V_G$, (b) $I_B - V_G$, and (d) $I_B - V_G$ electrical characteristics at different $V_D$ in abnormal current devices. (c) Schematic diagram showing the lower vertical electric field at drain side in linear region.**

Figure 4(a) and (b) shows $I_G - V_G$ and $I_B - V_G$ curves under different $V_D$ in abnormal current devices. It can be clearly observed that $I_G$ and $I_B$ become smaller with increasing $V_D$. The reduction of the vertical electric field near the drain side leads to the reduction of electrons tunneling from the inversion layer, as shown in Figure 4(c). In other words, the lateral electric field becomes stronger so that the electrons tend to drift into drains. Therefore, the generation of electron-hole pairs by electron impact ionization at the $HfO_2$/metal interface is also reduced. In addition, when these abnormal current devices are operated under the condition of large $V_D$ measurement, the electrons undergo impact ionization on the drain side, as shown in Figure 4(d). In conclusion, the impact ionization occurs at the gate when abnormal current devices are operated in the linear region and the impact ionization occurs at the drain when abnormal current devices are operated in the saturation region.

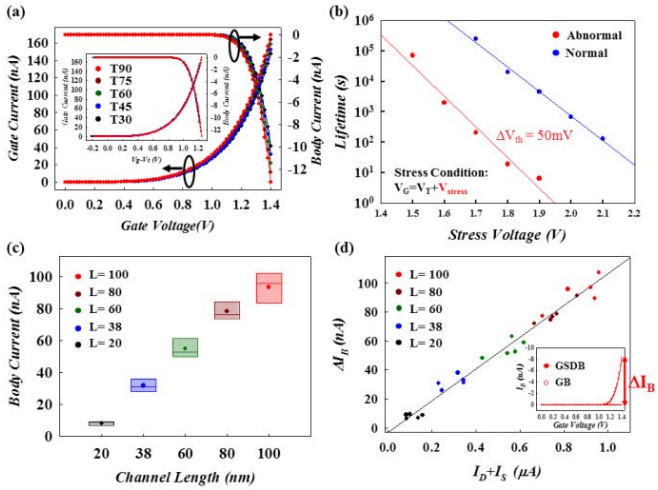


**FIGURE 5. (a) $I_G - V_G$ and $I_B - V_G$ electrical characteristics with $V_T$ correction at different temperatures. (b) PBS with $\Delta V_{th}$ = 50 mV lifetime plot for abnormal current/normal devices with different stress voltages ($V_{stress}$ = 1.5V ~ 2.1V). (c) $I_B$ shows a linear relationship for different channel lengths. (d) $\Delta I_B$versus $I_S + I_D$ indicates a linear relationship for different channel lengths. Inset shows the $I_B - V_G$ electrical characteristics under floating and grounded S/D operations.**

Figure 5(a) shows $I_G - V_G$ and $I_B - V_G$ at different temperatures for $V_D = 0$V. It is clear that $I_B$ and $I_G$ increase significantly with increasing temperature. However, they have insignificant changes after a $V_T$ correction for different temperatures, as shown in the inset of Figure 5(a). In general, the dominant mechanism of $I_G$ is Poole-Frenkel ($I_{P-F}$) in the hafnium oxide rather than the tunneling ($I_T$) mechanism in the silicon oxide [11]. Because the Poole-Frenkel current path and tunneling current path are in series, the current fitting is dominated by the smaller one. Therefore, the $I_G$ and $I_B$are dominated by tunneling mechanism because they are independent of temperature. Accordingly, the $HfO_2$ has more bulk traps, resulting in the tunneling mechanism ($I_{P-F} > I_T$), as confirmed by current fitting.

To further verify that the $HfO_2$ has more bulk traps in the abnormal current devices than the normal devices, we performed measurements of the reliability of positive bias stress (PBS) [12]. Thus, we define device failure criteria as 50mV $V_T$ shift, the lifetime for the device to reach this degradation value. Figure 5(b) shows the lifetime during PBS at $V_G = V_T + V_{stress}$ with $V_{stress} = 1.5V \sim 1.9$ V and 1.7V~2.1V for abnormal current/normal devices, respectively. Clearly, the lifetime of the abnormal current devices is 3 orders of magnitude shorter than that of the normal devices. Consequently, many bulk traps in $HfO_2$ lead to the abnormal body current. Because the electron can easily tunnel from the inversion layer to the metal gate and generate electron-hole pairs by impact ionization at the $HfO_2$/metal interface, these holes can easily tunnel to the body.

Figure 5(c) shows that $I_B$ has a linear relationship to channel length, which is measured by grounded source, drain, and body at $V_G = 1.4$V for different channel lengths. Because the abnormal $I_B$ is caused by the AHI model, longer channel

lengths lead to a larger body current. Furthermore, the AHI model-induced hole current has a linear dependence on the electron current tunneling from the inversion layer, as shown in Figure 5(d), with the $I_S + I_D$ indicating the electron tunneling current from the inversion layer. The $\Delta I_B$ is obtained by subtracting the GB component from the GSDB of $I_B$, which is the pure hole current induced by AHI model. These results provide further proof that the AHI model indeed exists and is the dominant mechanism contributing to abnormal body current in n-FinFETs. However, it is worth noting that since metal has no energy gap, holes are not easily generated in metal. Therefore, impact ionization is more likely to occur at the $HfO_2$/metal interface. Previous reports have indicated that doping $TiO_2$ with nitrogen will reduce the bandgap [13], [14]. In contrast, we believe that TiN will be oxidized to TiON at the $HfO_2$/TiN interface such that there will be a small bandgap at the interface. However, it is difficult to verify this model with simulation, so we use sputtering to deposit a layer of TiN thin film on a dummy wafer under a trace oxygen atmosphere at thicknesses of 2.59, 5.02, and 10.75 nm. After deposition of the thin films, the $E_g$ values measured by the N&K analyzer [15] were 1.41, 1.59, and 1.71 eV, respectively, as shown in Table 1. This also corresponds to the voltage at which the body current rises significantly in the $I_B - V_G$ diagram, which is approximately 1.1V, as shown in Figure 4 (b). After the flatband voltage correction, according to the formula $V_G - V_{fb} = V_{ox} + 2\phi_B$, the $V_{ox} + 2\phi_B$ value is approximately 1.6 to 1.9V. This voltage difference causes the electrons to gain energy, which is sufficient for generation of electron-hole pairs by electron impact ionization at the $HfO_2$/TiN interface.

**TABLE 1. The $E_g$ of TiON thin films of different thicknesses as measured by the N&K analyzer.**

| TiON Thickness(nm) | Eg(eV) | Goodness of Fit |
|---|---|---|
| 2.59nm | 1.41 | 0.9957 |
| 5.02nm | 1.59 | 0.9963 |
| 10.75nm | 1.71 | 0.9974 |

## IV. CONCLUSION

In this letter, different measurement techniques demonstrate that the abnormal $I_B$ is dominated by the AHI model. Additionally, $I_G$ and $I_B$ exhibit the tunneling mechanism because they have insignificant changes after a $V_T$ correction for different temperatures. Therefore, the $HfO_2$ has more bulk traps, resulting in the tunneling mechanism ($I_{P-F} > I_T$). Finally, the $V_{ox} + 2\phi_B$ value approximates the TiON band gap, demonstrating that impact ionization occurs at the $HfO_2$/metal interface.

## ACKNOWLEDGMENT

Part of this work was performed at United Microelectronics Corporation. This work was performed at the National Science Council Core Facilities Laboratory for Nano-Science and NanoTechnology, Kaohsiung-Pingtung Area, NSYSU Center for Nanoscience and Nanotechnology.

## REFERENCES

[1] G. Ribes *et al.*, "Review on high-k dielectrics reliability issues," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 1, pp. 5–19, Mar. 2005, doi: 10.1109/TDMR.2005.845236.

[2] H.-K. Lim and J. G. Fossum, "Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-30, no. 10, pp. 1244–1251, Oct. 1983, doi: 10.1109/T-ED.1983.21282.

[3] D. Hisamoto *et al.*, "FinFET—A self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Trans. Electron Devices*, vol. 47, no. 12, pp. 2320–2325, Dec. 2000, doi: 10.1109/16.887014.

[4] K. Mistry *et al.*, "A 45nm logic technology with high-k+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193nm dry patterning, and 100% Pb-free packaging," in *Proc. Int. Electron Devices Meeting*, Washington, DC, USA, Dec. 2007, pp. 247–250, doi: 10.1109/IEDM.2007.4418914.

[5] C. Hu *et al.*, "Hot-electron-induced MOSFET degradation—Model, monitor, and improvement," *IEEE J. Solid-State Circuits*, vol. SSC-20, no. 1, pp. 295–305, Feb. 1985, doi: 10.1109/JSSC.1985.1052306.

[6] T. Y. Chan, J. Chen, P. K. Ko, and C. Hu, "The impact of gate-induced drain leakage current on MOSFET scaling," in *Proc. Int. Electron Devices Meeting*, Washington, DC, USA, 1987, pp. 718–721, doi: 10.1109/IEDM.1987.191531.

[7] W.-C. Lee and C. Hu, "Modeling CMOS tunneling currents through ultrathin gate oxide due to conduction- and valence-band electron and hole tunneling," *IEEE Trans. Electron Devices*, vol. 48, no. 7, pp. 1366–1373, Jul. 2001, doi: 10.1109/16.930653.

[8] T. Kauerauf *et al.*, "Towards understanding degradation and breakdown of $SiO_2$/high-k stacks," in *Proc. Int. Electron Devices Meeting*, San Francisco, CA, USA, Dec. 2002, pp. 521–524, doi: 10.1109/IEDM.2002.1175894.

[9] K. F. Schuegraf and C. Hu, "Hole injection oxide breakdown model for very low voltage lifetime extrapolation," in *Proc. IRPS*, Atlanta, GA, USA, 1993, pp. 7–12, doi: 10.1109/RELPHY.1993.283311.

[10] J. Luo *et al.*, "Temperature dependence of hysteresis effect in partially depleted silicon-on-insulator MOSFETs," *IEEE Trans. Device Mater. Rel.*, vol. 12, no. 1, pp. 63–67, Mar. 2012, doi: 10.1109/TDMR.2011.2165282.

[11] D. P. Ioannou, "HKMG CMOS technology qualification: The PBTI reliability challenge," *Microelectron. Rel.*, vol. 54, no. 8, pp. 1489–1499, Aug. 2014, doi: 10.1016/j.microrel.2014.03.018.

[12] E. Cartier, B. P. Linder, V. Narayanan, and V. K. Paruchuri, "Fundamental understanding and optimization of PBTI in nFETs with $SiO_2/HfO_2$ gate stack," in *Proc. Int. Electron Devices Meeting*, San Francisco, CA, USA, 2006, pp. 321–324, doi: 10.1109/IEDM.2006.346773.

[13] P.-G. Wu, C.-H. Ma, and J. K. Shang, "Effects of nitrogen doping on optical properties of $TiO_2$ thin films," *Appl. Phys. A, Solids Surf.*, vol. 81, no. 7, pp. 1411–1417, Nov. 2005, doi: 10.1007/s00339-004-3101-4.

[14] Q. Li and J.-K. Shang, "Heavily nitrogen-doped dual-phase titanium oxide thin films by reactive sputtering and rapid thermal annealing," *J. Amer. Ceramic Soc.*, vol. 91, no. 10, pp. 3167–3172, Oct. 2008, doi: 10.1111/j.1551-2916.2008.02608.x.

[15] A. Callegari *et al.*, "Physical and electrical characterization of Hafnium oxide and Hafnium silicate sputtered films," *J. Appl. Phys.*, vol. 90, no. 12, pp. 6466–6475, Nov. 2001, doi: 10.1063/1.1417991.

**JIH-CHIEN LIAO** is currently pursuing the Ph.D. degree with the Institute of Electronics Engineering, National Tsing-Hua University, Hsinchu, Taiwan.

**TING-CHANG CHANG** (SM'12) received the Ph.D. degree from the Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, in 1994.

He is currently a Chair Professor with the Department of Physics, National Sun Yat-sen University, Kaohsiung, Taiwan. He has authored over 400 articles in SCI journals. He holds 49 U.S. patents and 127 Taiwan patents. His current research includes thin film transistor, MOSFET, and resistive random access memory.

**WEI-REN SYONG** is currently pursuing the B.S. degree with the Department of Physics, National Sun Yat-sen University, Kaohsiung, Taiwan.

**KAI-CHUN CHANG** is currently pursuing the M.S. degree with the Department of Physics, National Sun Yat-sen University, Kaohsiung, Taiwan.

**YING-HSIN LU** is currently pursuing the Ph.D. degree with the Department of Physics, National Sun Yat-sen University, Kaohsiung, Taiwan.

**HSI-WEN LIU** is currently pursuing the Ph.D. degree with the Department of Physics, National Sun Yat-sen University, Kaohsiung, Taiwan.

**CHIEN-YU LIN** is currently pursuing the Ph.D. degree with the Department of Photonics, National Sun Yat-sen University, Kaohsiung, Taiwan.

**LI-HUI CHEN** received the M.S. degree from the Department of Photonics, National Sun Yat-sen University, Kaohsiung, Taiwan, in 2017.

She is currently with Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan.

**FU-YUAN JIN** is currently pursuing the Ph.D. degree with the Department of Physics, National Sun Yat-sen University, Kaohsiung, Taiwan.

**YU-HSUAN CHEN** is currently pursuing the Ph.D. degree with the Institute of Electronics Engineering, National Tsing-Hua University, Hsinchu, Taiwan.

**CHEN-HSIN LIEN** received the B.S. degree in physics from the National Tsing-Hua University (NTHU), Hsinchu, Taiwan, in 1975 and the Ph.D. degree in physics from Ohio State University, USA, in 1982. He is the a Professor with the Department of Electrical Engineering, NTHU. His research has primarily focused on the solid-state devices ranging from the quantum optoelectronic devices, CMOS devices, and nanoelectronic devices to memories.

Since 1983, he has been with the Department of Electrical Engineering, NTHU, where he was the Director of the Institute of Electronic Engineering from 2004 to 2006. From 2006 to 2010, he was the Chair of the Department of Electrical Engineering, NTHU. In 2010, he was the Acting Dean with the College of Electrical Engineering and Computer Science, NTHU. His recent research interests including the studies of 2-D semiconductor devices and nonvolatile memories.

**OSBERT CHENG** is with United Microelectronics Corporation, Tainan, Taiwan.

**CHENG-TUNG HUANG** is with United Microelectronics Corporation, Tainan, Taiwan.

**YI-HAN YE** is with United Microelectronics Corporation, Tainan, Taiwan.