Received 1 February 2018; revised 27 March 2018; accepted 20 April 2018. Date of publication 25 June 2018;
date of current version 6 July 2018. The review of this paper was arranged by Editor E. Sangiorgi.

Digital Object Identifier 10.1109/JEDS.2018.2831278

A Substrate-Dissipating (SD) Mechanism for a Ruggedness-Improved SOI LDMOS Device

BING WANG [1], ZHIGANG WANG [1], AND JAMES B. KUO [2] (Fellow, IEEE)

1 School of Information Science and Technology, Southwest Jiao Tong University, Chengdu 611756, China
2 Department of Electrical Engineering, National Taiwan University, Taipei 10617, Taiwan

CORRESPONDING AUTHOR: Z. WANG (e-mail: zhigangwang@swjtu.edu.cn)

This work was supported in part by the National Natural Science Foundation of China under Grant 61404110, and in part by the National Higher-Education Institution General Research and Development Project under Grant 2682014CX097.

ABSTRACT An SOI LDMOS device with improved ruggedness under unclamped inductive switching (UIS) is described based on the substrate-dissipating (SD) mechanism. The key feature of this device is the introduction of a Γ-shape P-island window with a relatively high doping concentration to connect the N-drift region to the P-substrate under the source, which is designed to achieve an avalanche breakdown point at the edge of the P-island instead of near the gate contact. Thus, the avalanche current is shortened to the substrate contact through the P-island and the P-substrate, avoiding the avalanche current to pass through the N^+ source/P-well junction and thus suppressing the activation of the parasitic bipolar transistor with a relaxed self-heating effect especially in the P-well region. As verified by the Medici device simulation results, the SD mechanism of the device under the UIS condition, may endure a remarkably higher avalanche current as compared with the conventional SOI LDMOS device.

INDEX TERMS Unclamped inductive switching (UIS), SOI LDMOS, avalanche current, parasitic BJT, substrate-dissipating (SD), self-heating.

I. INTRODUCTION

Silicon-on-insulator lateral diffused metal-oxide semiconductor (SOI LDMOS) devices are widely used in power electronic control systems owing to their fast switching speed and high-impedance capability [1]–[3]. Many efforts have been done to achieve the high breakdown voltage (BV) and low on-state resistance (R_{on}) [4]–[6] of the SOI LDMOS devices. However, as the switching control device, their energy handing capability and ruggedness performance should also be considered. Unclamped inductive switching (UIS) test is used as an extremely severe condition to evaluate the ruggedness of the device under an inductive load, where the device must dissipate all of the energy stored in the inductor during the on-state when turned off. As a consequence, a simultaneous high voltage and large current may cause a high power loss, which may destroy the device. Specifically, the failure of a power MOSFET during a UIS test is mainly due to the activation of the parasitic bipolar transistor (BJT), which increases the current and raises the junction temperature, eventually forcing the device into the thermal runaway condition [7]–[9]. In order to suppress the activation of the parasitic BJT in the device, several methods have been reported [10]–[13]. These methods include reducing the sheet resistance of the P-well beneath the N^+ source by using a high-energy boron implantation or a deep diffusion [10]–[11] or minimizing the N^+ source/P-well junction with a very thin vertical source region [12], [13]. As a result, these techniques have improved the UIS performance considerably. However, the control of the additional delicate process to define the high dose body implant is difficult [10], [11] and minimizing the N^+ source region may bring in problems in contacting or threshold-voltage (V_{th}) shifting [12], [13].

There is also another method by diverting the avalanche current direction from the edge to the bottom of the P-well by employing a segmented trench body contact [14], [15]. However, the use of trench contact to reroute the avalanche current path requires more complex contacting technology, especially for the devices with narrow cell pitches. In addition, the avalanche current flowing to the P-well may also cause a rise in temperature to lower the carrier mobilities

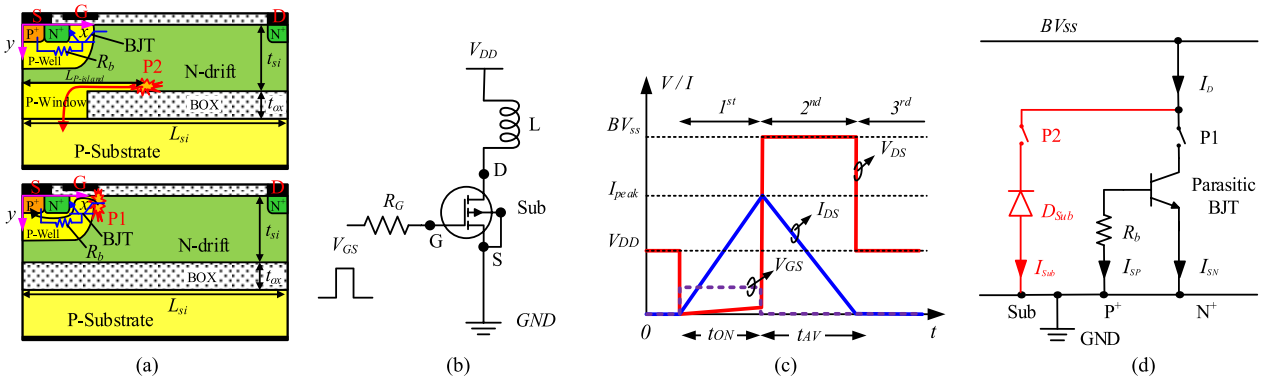

FIGURE 1. **(a) Structures of PW-SOI LDMOS device (top) and conventional SOI LDMOS device (bottom). (b) The UIS test setup and (c) the typical relevant waveforms for the DUT under the UIS test condition. (d) The equivalent circuit of the proposed device during the UIS avalanche breakdown period (2nd stage). I_D is the total avalanche current in the device. $I_{SP}/I_{SN}/I_{Sub}$ is the avalanche current flowing to the source P^+/source N^+/substrate.**

in the region, prompting the easier turn-on of the parasitic BJT and thus offset the improvement in UIS.

In this paper, a substrate-dissipating (SD) mechanism in the PW-SOI LDMOS device as shown in Fig. 1(a) is proposed to improve the UIS durability. The SD mechanism is implemented by introducing an auxiliary pathway to dissipate the UIS energy to the substrate. Based on this SD mechanism, an SOI LDMOS device with a Γ- shape P-island window (PW) using partial technique is proposed. In this PW-SOI LDMOS device, the Γ- shape P-island window with the drift region connected to the substrate offers an auxiliary substrate-dissipated pathway for expunging the UIS energy. In particular, the P-island window can move the avalanche breakdown point at the drain side of the channel to the edge of the P-island window. Thus, the avalanche current is shorted to the substrate through the window without activating the parasitic bipolar transistor. Furthermore, this avalanche current pathway can dramatically relax the self-heating effect during the UIS-mode operation. Hence, the UIS durability of this PW-SOI LDMOS may be enhanced remarkably by the SD mechanism, as compared with conventional SOI LDMOS (C-SOI LDMOS) device. Additionally, the aforementioned contact problem or V_{th} shifting is avoided.

II. STRUCTURE AND MECHANISM

The schematic cross-section views of the proposed PW-SOI LDMOS device and the C-SOI LDMOS device are given Fig. 1(a), with the inherent parasitic bipolar junction transistors (BJTs), which are made of an N^+ source as the emitter, a P-well as the base, and an N-drift region as the collector. As shown in Fig. 1(a), the base resistance R_b comprises the P-well series resistance connected to the parasitic BJT base. Unlike the C-SOI LDMOS device, the proposed device features a highly-doped P-island window, connecting the N-drift region to the P-substrate. Moreover, this P-island window is designed in a specific way, stretching into the N-drift region on the top surface of the buried oxide (BOX) for ensuring the vertical SD channel.

Figs. 1(b) and (c) show the schematic UIS test setup and its typical relevant waveforms. The UIS test can be divided into three stages. The 1st stage is the turn-on stage, where the device under test (DUT) is switched on by the pulse voltage generator (V_{GS}) and the inductance current is at its peak value (I_{peak}) in a time period of t_{ON}. The 2nd stage is the breakdown stage, where the avalanche breakdown state is generated by the switch-off of the DUT. In the breakdown stage, the DUT must tolerate a breakdown voltage ($BVss$) until the drain current decreases from I_{peak} to zero in a time period t_{AV}. The 3rd stage is where the device sustains a drain applied voltage (V_{DD}). Here, the device is analyzed only during the second stage.

Based on the description in Figs. 1(a)–(c), an equivalent circuit of the device during the second stage under the UIS condition is given in Fig. 1(d). In the C-SOI LDMOS device, the avalanche breakdown is occurred at point P1 as shown in Fig. 1(a). At this point, a vast number of impact-generated carriers are created to form the avalanche current to consume the UIS energy. The avalanche-breakdown-induced holes are attracted to the P^+ source contact through the P-well region to generate the current (I_{SP}), developing a voltage drop V_b across R_b. When V_b grows to be larger than the built-in potential of the N^+ source/P-well junction (~0.7 V), the parasitic BJT is triggered to form the current path (I_{SN}) with a thermal breakdown.

The avalanche-current handling capacity can be improved by the introduction of the P-island window in the PW-SOI LDMOS device as shown in Fig. 1(a). As seen from the Medici simulation results, the SD mechanism with the P-island window connecting the drift region to the substrate offers an avalanche-current pathway to dissipate the UIS energy. In addition, the P-island window and the N-drift region form an island junction in the vertical direction, where pre-breakdown is easier to occur and thus the avalanche point is occurred at location P2, where the avalanche-induced current flows to the substrate through the P-island window. As shown in the Fig. 1(d), this substrate-conduct pathway may prevent the forward bias of the base-emitter junction

of the parasitic BJT. Thus, the trigger of parasitic BJT can be suppressed. Furthermore, the P-island window provides a self-heating channel for achieving a good thermal capability.

III. RESULT AND DISCUSSION

Two-dimensional (2D) MEDICI device simulation of the test device is carried out in this study. In the test setup as shown in Fig. 1(b), the test device is connected to V_{DD} with an inductive load of 50 μH. The power supply V_{DD} is 50 V and V_{GS} is 15 V. t_{ON} is the charge time during the turn-on stage, (t_{ON} = 50 μs). A short time of 1μs after the t_{ON} is defined as the quasi-static point for analyzing the working mechanism under the UIS avalanche breakdown condition. The active area of the device is 13 mm^2 and other main physical parameters are listed in Table 1.

TABLE 1. Device Parameters Specification

Parameters	PW-SOI LDMOS	C-SOI LDMOS
N-drift Doping, N_d /cm^{-3}	7×10^{15}	7×10^{15}
P-island Doping, $N_{P\text{-}island}$/ cm^{-3}	$(1\sim25)\times10^{16}$	—
P-well Doping, N_{well}/cm^{-3}	1×10^{17}	1×10^{17}
P-Substrate Doping, N_{Sub}/cm^{-3}	5×10^{15}	5×10^{15}
Device Length, L_{si}/μm	13	13
BOX layer Length, L_{ox}/μm	12	13
P-island Length, $L_{P\text{-}island}$/μm	2 ~ 4	—
N-drift Thickness, t_{si}/μm	2.5	2.5
BOX layer Thickness, t_{ox}/μm	1.0	1.0
Device Width, W_{si}/mm	10^3	10^3

In particular, the doping concentration $N_D = 7\times10^{15}$ cm^{-3} is the optimal doping for a best BV of 172 V in the C-SOI LDMOS. For comparison purposes, this $N_D = 7\times10^{15}$ cm^{-3} is also selected in proposed device. At this $N_D = 7\times10^{15}$ cm^{-3}, the proposed device with an optimal $N_{P\text{-}island}$ of 1.2×10^{17} cm^{-3} and $L_{P\text{-}island}$ of 3.5 μm can achieve a BV of 169 V. These results can be verified from the Fig. 2(a). The V_{th} and R_{on} are also simulated and shown in Fig. 2(b). Apparently, the C-SOI LDMOS and PW-SOI LDMOS devices share almost the same V_{th} and R_{on}, that is, problems such as the V_{th} shifting and conductive degradation are all avoided in the proposed device.

Fig. 3 shows the distributions of the impact ionization rate in the PW-SOI LDMOS and C-SOI LDMOS device under the quasi-static condition. In the C-SOI LDMOS device, the avalanche breakdown point is located at P1. In contrast, the avalanche breakdown point in the PW-SOI LDMOS device is switched to P2 due to the pre-breakdown occurring at the island junction. This avalanche breakdown point switched to P2, may result in reshaping the avalanche-current pathway. The corresponding distributions of the avalanche current are shown in Fig. 4, where the avalanche current injects into the P$^+$ source through the P-well in the C-SOI LDMOS device.

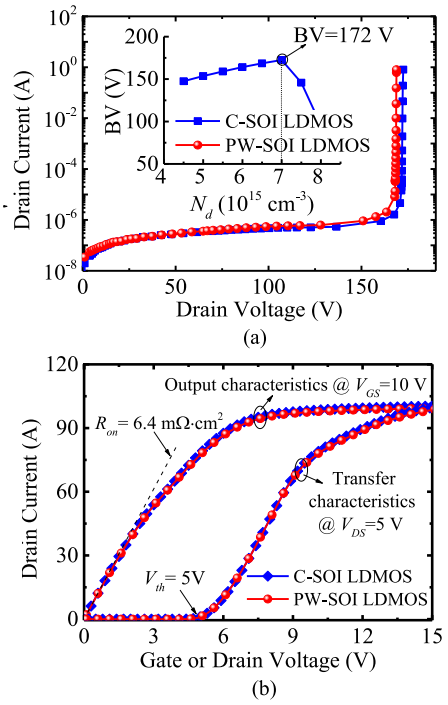

FIGURE 2. (a) Output characteristics under the blocking state and (b) Output characteristics and transfer characteristics in the PW-SOI LDMOS device and the C-SOI LDMOS device. Insert in (a) is the influence of N-drain region doping on BV in C-SOI LDMOS.

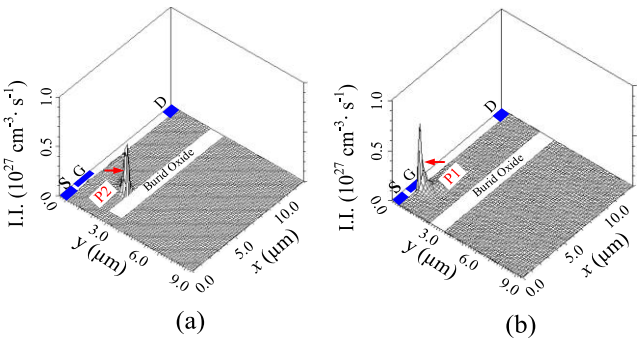

FIGURE 3. Impact ionization rate distribution in (a) the PW-SOI LDMOS and (b) the C-SOI LDMOS device during the UIS avalanche breakdown.

In contrast, the avalanche current goes into substrate contact directly in the PW-SOI LDMOS device when the avalanche breakdown point switched to P2. Under the UIS test condition as given in Fig. 1(b), at the avalanche breakdown point, the impact-generated electrons are swept into drain and holes into ground electrode (source or substrate). Thus, a different location of avalanche breakdown may result in a different pathway of avalanche current.

Fig. 5(a) shows I_{SN}, I_{SP} and I_{Sub} in the PW-SOI LDMOS device and C-SOI LDMOS device. It is clearly both devices keep conductive by the I_{SN} during the period of t_{ON}. These I_{SN} increase linearly with the time until devices are turned off. When devices are turned off, the avalanche current flows mainly as I_{SP} in the C-SOI LDMOS device as predicted. In

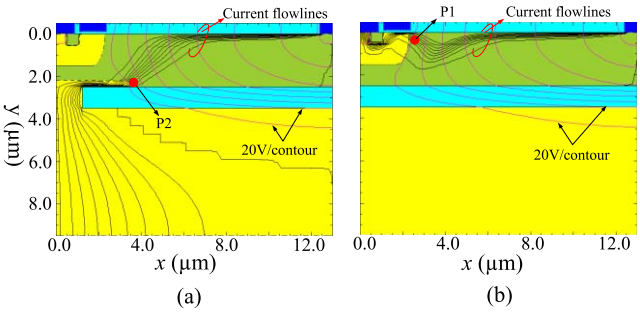

FIGURE 4. Avalanche current distribution of (a) PW-SOI LDMOS and (b) C-SOI LDMOS device during the UIS avalanche breakdown.

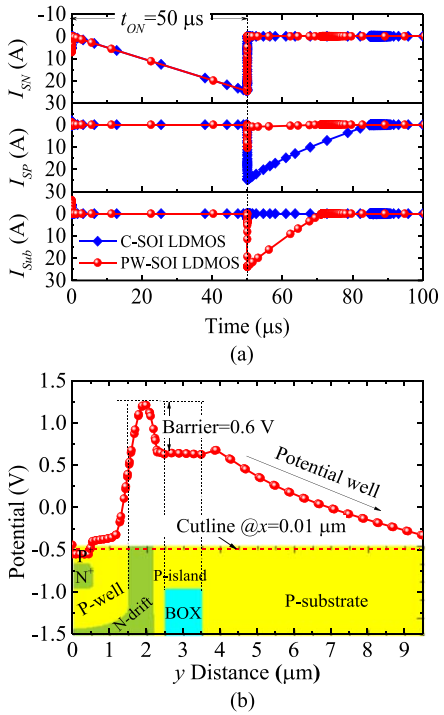

FIGURE 5. (a) I_{SN}, I_{SP} and I_{Sub} in the PW-SOI LDMOS device and the C-SOI LDMOS device, (b) the potential distribution in the substrate direction at $x = 0.01\mu$m in the PW-SOI LDMOS device during the UIS avalanche breakdown based on Medici simulation results.

contrast, in the PW-SOI LDMOS device, a high barrier along the substrate direction is achieved in the N-drift between the P-well and the P-island. Thus, most avalanche current is driven to the substrate and I_{SP} has little effects, which confirms the SD mechanism.

Fig. 5(b) gives the potential in the substrate direction at $x = 0.01$ μm in the PW-SOI LDMOS device during the avalanche breakdown. A potential barrier of about 0.6 V in the P-well region is induced in the drift region, driving the avalanche-induced holes to the substrate instead of the source.

Fig. 6 shows the potential distribution along $y = 0.6$ μm in the x direction in the P-well region of the PW-SOI LDMOS device and C-SOI LDMOS device based on the Medici simulation results. The potential contours in the P-well region are

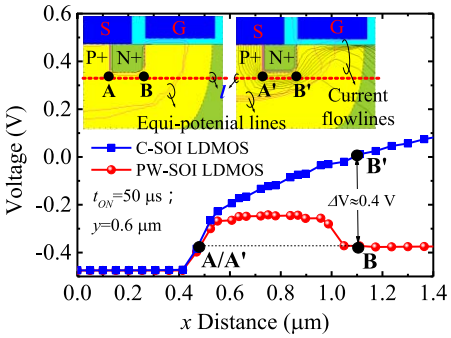

FIGURE 6. Potential distribution along the lateral direction at y = 0.6 μm (line *I*) in the P-well region in the PW-SOI LDMOS device and the C-SOI LDMOS device during the UIS avalanche breakdown based on Medici simulation results. Inserts are the corresponding potential contours and current flowlines in the P-well region in these both devices.

given in the inserts of Fig. 6. In the C-SOI LDMOS device, the voltage drop between A'-B' is about 0.4 V. However, in the proposed device, the voltage drop between A-B is about 0 V. The existence of Γ-shape P-island window impels the avalanche current and flowing into the substrate contact to avoid a voltage drop at R_b. Thus, the parasitic BJT is more difficult to trigger. The inserted illustration also demonstrates that no avalanche current flows through the P-well region in the proposed device without the voltage drop in the P-well underneath the N^+ region. In contrast, a large avalanche current in the C-SOI LDMOS device flows through the P-well with a voltage drop of ~ 0.4 V.

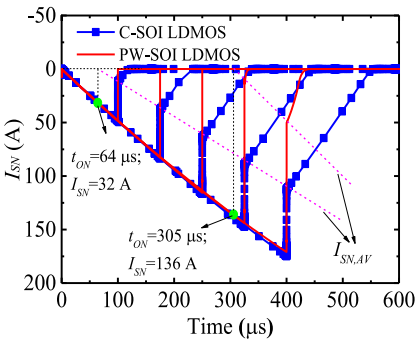

FIGURE 7. I_{SN} at different t_{ON} in the PW-SOI LDMOS device and the C-SOI LDMOS device during the UIS avalanche breakdown based on the Medici simulation results. $I_{SN,AV}$ is the maximal avalanche current flowing into the N^+ source when the device is turned off. The condition $I_{SN,AV} > 0$ means an activation of parasitic BJT.

If the charge time t_{ON} is big enough to develop a voltage drop V_b over 0.7 V, the parasitic BJT is triggered on with a current flowing into the N^+ source contact (I_{SN}) during the time t_{AV}. Fig. 7 shows the I_{SN} at different t_{ON}'s of the PW-SOI LDMOS device and the C-SOI LDMOS device and the corresponding $I_{SN,AV}$ (the maximal I_{SN} during the second stage under the UIS test) based on the Medici simulation results. $I_{SN,AV}$ in the proposed structure begins to increase at about $t_{ON} > 305$ μs, while $I_{SN,AV}$ in C-SOI LDMOS device

begins to express a rising trend only about $t_{ON} > 65$ μs. That is, the activation of parasitic BJT in PW-SOI LDMOS needs more charging time. In particular, the maximum of the sustainable avalanche current ($I_{AV,max}$) in the C-SOI LDMOS device is extracted to be 32 A at $t_{ON} = 64$ μs. In contrast, the $I_{AV,max}$ in PW-SOI LDMOS device is extracted to an even high avalanche current of ∼136 A at $t_{ON} = 305$ μs. This implies that the sustained avalanche current of the PW-SOI LDMOS device is about 4.25 times higher than the conventional one, which is due to the fact that the proposed device offers a wider vertical pathway to drive the avalanche current away from the turn-on of the parasitic BJT.

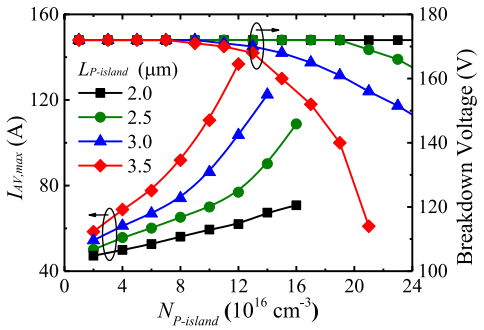

FIGURE 8. Influence of the doping concentration of the P-island ($N_{P\text{-}island}$) and the varying length of the P-island ($L_{P\text{-}island}$) in I_{AV_max} and BV of the PW-SOI LDMOS device.

Fig. 8 illustrates $I_{AV,max}$ and BV varying the P-island doping concentration ($N_{P\text{-}island}$) at various lengths of the P-island ($L_{P\text{-}island}$). At a given $L_{P\text{-}island}$, $I_{AV,max}$ increases with the increment of $N_{P\text{-}island}$. An increase in $N_{P\text{-}island}$ offers a much higher peak in the electric field at the island-junction. When this electric field peak is larger than the critical electric field, the pre-avalanche breakdown is generated at the island junction. This pre-avalanche at the island junction leads to more avalanche currents to flow into the substrate directly, thus the avalanche current to trigger the parasitic BJT is enhanced. A longer $L_{P\text{-}island}$ can also lead to an increment in $I_{AV,max}$ for the same reason that a pre-avalanche breakdown is easier to occur at the island junction. Therefore, a high $N_{P\text{-}island}$ or long $L_{P\text{-}island}$ is a considerate way to achieve an improved-UIS capacity. However, a high $N_{P\text{-}island}$ or long $L_{P\text{-}island}$ brings in a pre-breakdown at the island-junction and thus results in a decrease in BV. Namely, under a high $N_{P\text{-}island}$ or long $L_{P\text{-}island}$, island-junction work as the main junction to determine the BV. Moreover, the higher $N_{P\text{-}island}$ or longer $L_{P\text{-}island}$ is, the higher impact ionization at island-junction occurs and the lower BV is obtained in novel device. The maximum BV can be guaranteed with low $N_{P\text{-}island}$ or short $L_{P\text{-}island}$. The reason is P/N junction at P1 behaves as the main junction to determine the BV and such a P-island behaves very little influence on blocking avalanche breakdown.

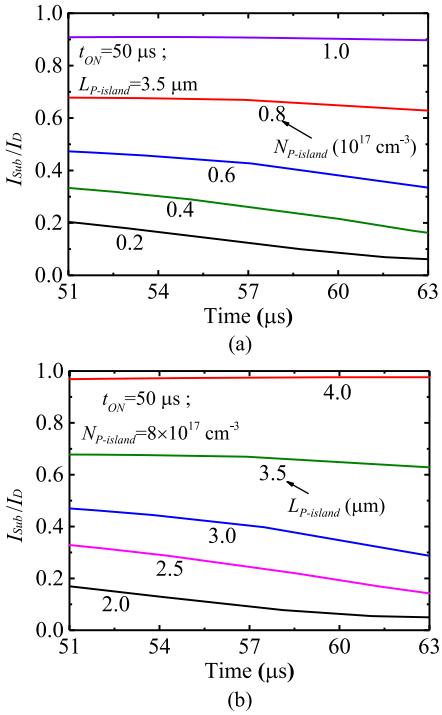

FIGURE 9. Influence of (a) the doping concentration of the P-island ($N_{P\text{-}island}$) and (b) the length of the P-island ($L_{P\text{-}island}$) in I_{Sub}/I_D.

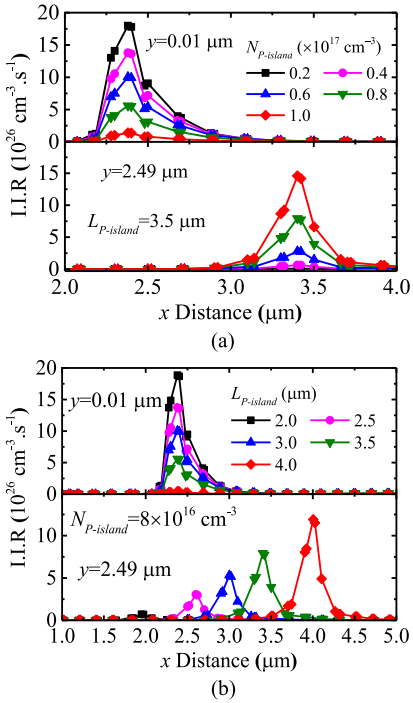

FIGURE 10. Influence of (a) $N_{P\text{-}island}$ and (b) $L_{P\text{-}island}$ in the impact ionization rate in PW-SOI LDMOS devices based on the Medici.

Fig. 9 shows the influence of the $N_{P\text{-}island}$ at various lengths of the $L_{P\text{-}island}$ in I_{Sub}/I_D of the PW-SOI LDMOS device. A high $N_{P\text{-}island}$ may result in a pre-avalanche breakdown occurring at the island junction, rendering the

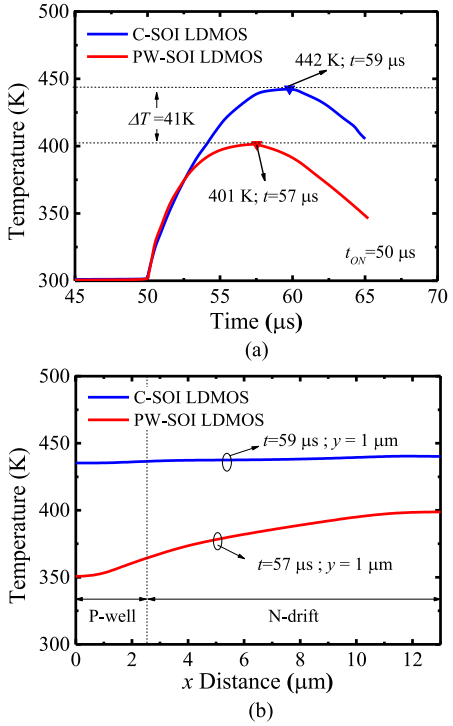

FIGURE 11. **(a) The maximal lattice temperature during the UIS test and (b) the lattice temperature along the horizontal direction at y=1 μm at the time of the maximal lattice temperature achieved in both the PW-SOI LDMOS and the C-SOI LDMOS devices.**

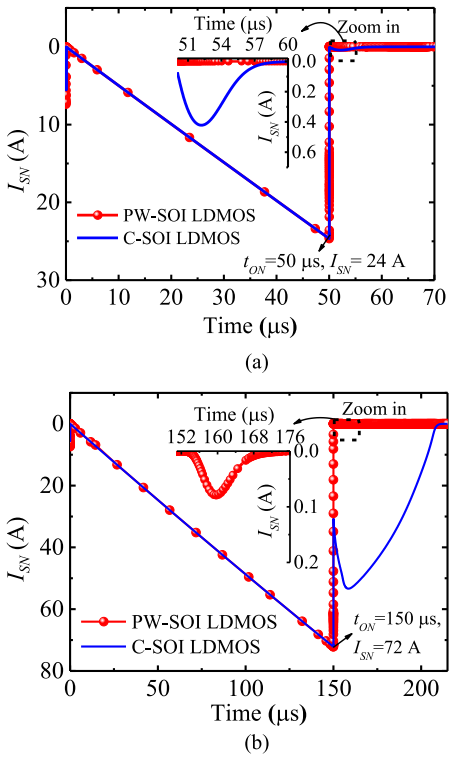

FIGURE 12. **Simulated I_{SN} in both the PW-SOI LDMOS device and the C-SOI LDMOS device during the avalanche breakdown under a non-isothermal condition with t_{ON} = 50 μs and (b) t_{ON} = 150 μs, respectively. Insert Figs are zoom-in diagram of I_{SN} *vs.* time when devices are turned off.**

avalanche current flowing to the substrate. In Fig. 9(a), at a given length $L_{P\text{-}island}$ of 3.5 μm, I_{Sub}/I_D is increased with the increment in the $N_{P\text{-}island}$. In particular, at a high $N_{P\text{-}island}$ of 1.0×10^{17} cm^{-3}, about 90% of the avalanche current injects into the substrate. In contrast, at a low $N_{P\text{-}island}$ of 0.2×10^{17} cm^{-3}, the avalanche current injects into the substrate is lower than the 20 percent of the total current. In Fig. 9(b), at the $N_{P\text{-}island} = 8 \times 10^{16}$ cm^{-3}, a long $L_{P\text{-}island}$ can also lead an increment in I_{Sub}/I_D for the same reason that a pre-avalanche breakdown is easier to occur at the island junction. If all the avalanche current works as I_{Sub}, the parasitic BJT in the device would never be triggered.

Fig. 10 shows the influence of $N_{P\text{-}island}$ and $L_{P\text{-}island}$ on the impact ionization rate of the PW-SOI LDMOS device. In Fig. 10(a), at a given $L_{P\text{-}island}$ of 3.5 μm, the impact ionization rate at the island-junction is increased with an increase in $N_{P\text{-}island}$, but the impact ionization rate at the gate edge is decreased. In Fig. 10(b), at $N_{P\text{-}island} = 8 \times 10^{16}$ cm^{-3}, the impact ionization rate at the island-junction can be increased with an increase in $L_{P\text{-}island}$, but the impact ionization rate at the gate edge decreases. These Medici simulation results confirm the trends described in Figs. 8 and 9.

Results presented above are based on the isothermal condition. In fact, a large amount of energy dumped into the device during the UIS condition may cause considerable self-heating of the devices [7], [8]. The self-heating and the ambient temperature rise may cause the depression of the carrier mobilities and an easier turn-on of the parasitic bipolar device. Therefore, it is important to improve the UIS capacity even under the non-isothermal conditions. Considering the non-isothermal conditions, the thermal electrode along the top and bottom are created, respectively. The corresponding thermal resistances of 2.59×10^6 W/K·μm with packaging material of Kapton and 5×10^3 W/K·μm with heatsink material of AlSiC material are specialized referring to [16], [17]. Moreover, some temperature-dependent models such as the temperature-dependent mobility and impact ionization, have also been considered in the simulation.

Fig. 11(a) shows the maximal lattice temperature at t_{ON} = 50 μs in both the PW-SOI LDMOS device and the C-SOI LDMOS device based on the Medici simulation results. During the first stage of the UIS test, the lattice temperature keeps at about 300 K due to a low resistance at ON state. When the device is turned off, the lattice temperature rises sharply at first and then decreases slowly. In particular, the maximal lattice temperature in the C-SOI LDMOS is about 442 K at t = 59 μs, in contrast, the maximal lattice temperature in the proposed device is just 401 K at t = 57 μs. Hence, the self-heating effect in the proposed device is eased remarkably. Fig. 11(b) shows the lattice temperature along the horizontal direction at y = 1 μm at the time of maximal lattice temperature achieved. It is noted that the lattice temperature at the P-well region is only smaller

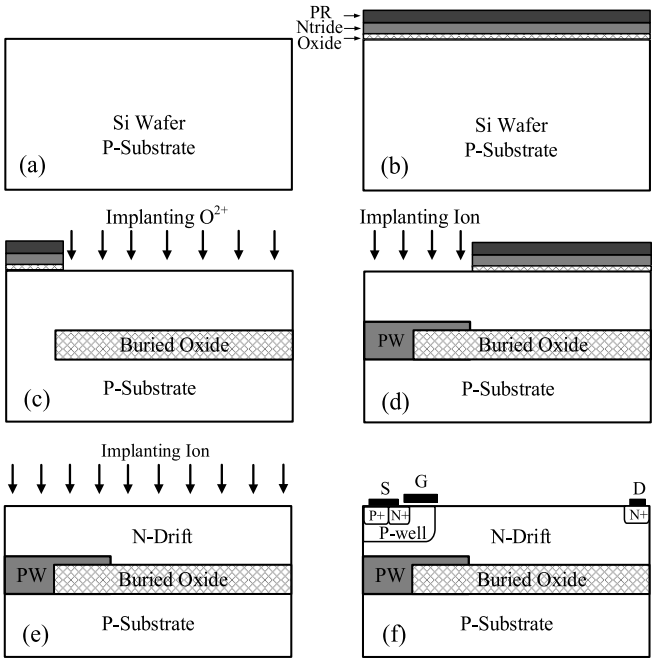

FIGURE 13. **The key process steps for the new device: (a) P-type Si wafer; (b) P-type Si wafer with grown thin thermal oxide; (c) implanting O^{2+} and annealing to form the Partial SOI; (d) implanting boron ion and annealing to form the P-island window; (e) implanting ion and annealing to form the N- drift; (f) forming the source, P-well and drain region.**

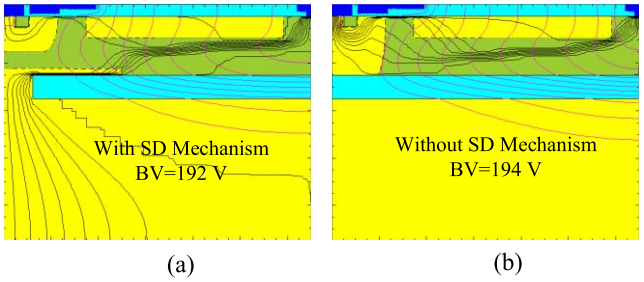

FIGURE 14. **Avalanche current distribution of RESURF LDMOS (a) with and (b) without SD mechanism during the UIS avalanche breakdown.**

than 365 K in the proposed device and ~438 K in the C-SOI LDMOS device. Because of the P-island window at the source side offering a heat-dissipating pathway, a lower lattice temperature is achieved to reduce the effect on the depression of the carrier mobilities especially at the source side for enhancing the UIS capability of the novel device.

Fig. 12(a) shows the I_{SN} in the PW-SOI LDMOS device and the C-SOI LDMOS device under the non-isothermal condition. When t_{ON} is 50 μs, I_{SN} in the C-SOI LDMOS device is raised from 0 A up to ~0.4 A as the current peak when device is turned off. This phenomenon indicates that the UIS sustainable avalanche current ($I_{AV,max}$) in the C-SOI LDMOS device is degraded to about 24 A due to a rise in temperature. In contrast, in the PW-SOI LDMOS device, the parasitic BJT is more difficult to turn on even at $I_{AV,max} = 72$ A, about 3 times bigger than that in C-SOI LDMOS device. This is due to, on one hand, the fact a relatively low lattice temperature is achieved by the heat-dissipating pathway to relax the depression of the carrier mobilities. On the other hand, the avalanche current vertically injected into the substrate may directly avoid a high voltage drop on the base resistance R_b even at a high lattice temperature. Hence, a well UIS capacity can be achieved in the proposed device even under the non-isothermal condition.

Fig. 13 shows the key process steps for realizing the PW-SOI LDMOS based on the reference [18]. Firstly, the P-type substrate wafer is prepared as shown in Fig. 13(a). Then, a thin thermal oxide is grown on the wafer for preventing oxygen implantation and structured by using photolithography (PR) and reactive ion etching as shown Fig. 13(b). The next step is to implant the O^{2+} with proper dose and optimized implant energies to form the partial buried oxide layer as shown in Fig. 13(c). Fig. 13(d) shows that p-type impurities with proper dose and optimized implant energies are implanted to form the P-island window after annealing. As shown in Fig. 13(e), N-type impurities are implanted to form the N-drift region. The last processes of forming the P-well, source and drain region are equivalent of the conventional CMOS process as shown in Fig. 13(f).

Finally, it is noted that the substrate-dissipating (SD) mechanism can also be applied to the power LDMOS with RESURF and plate technology. For example, implementation of the SD mechanism to a double-RESURF SOI LDMOS with gate plate is given in Fig. 14 under UIS condition. Obviously, most of avalanche current is swept away into the substrate contact due to SD effect. However, the BV in Fig. 14(a) with SD effect is just decreased by 2 V compared with the conventional one as shown in Fig. 14(b).

IV. CONCLUSION

A ruggedness-improved SOI LDMOS device using the P-island window structure with its performance under unclamped inductive switching is described, as verified by the MEDICI simulation results. In the new device, the avalanche current is shortened to the grounded substrate contact through the P-island and the P-substrate, successfully avoiding the avalanche current to pass through the N^+ source/P-well junction and thus avoiding the activation of the parasitic bipolar transistor. With the P-island window, self-heating is relaxed and thus the proposed device can sustain a larger avalanche current, as compared with a conventional SOI LDMOS device.

REFERENCES

[1] J. Kim *et al.*, "High-voltage power integrated circuit technology using SOI for driving plasma display panels," *IEEE Trans. Electron Devices*, vol. 48, no. 6, pp. 1256–1263, Jun. 2001, doi: 10.1109/16.925257.
[2] D. M. Garner *et al.*, "Silicon-on-insulator power integrated circuits," *Microelectron. J.*, vol. 32, nos. 5–6, pp. 517–526, Jun. 2001, doi: 10.1016/S0026-2692(01)00024-6.
[3] F. Udrea, "SOI-based devices and technologies for high voltage ICs," in *Proc. Bipolar/BiCMOS Circuits Technol. Meeting*, Boston, MA, USA, Oct. 2007, pp. 74–81, doi: 10.1109/BIPOL.2007.4351842.

[4] A. W. Ludikhuize, "A review of RESURF technology," in *Proc. Power Semicond. Devices ICs*, May 2000, pp. 11–18, doi: 10.1109/ISPSD.2000.856763.
[5] I.-Y. Park and C. A. T. Salama, "New superjunction LDMOST with N-buffer layer," *IEEE Trans. Electron Devices*, vol. 53, no. 8, pp. 1909–1913, Aug. 2006, doi: 10.1109/TED.2006.877007.
[6] B. Zhang, Z. Li, S. Hu, and X. Luo, "Field enhancement for dielectric layer of high-voltage devices on silicon on insulator," *IEEE Trans. Electron Devices*, vol. 56, no. 10, pp. 2327–2334, Oct. 2009, doi: 10.1109/TED.2009.2028405.
[7] K. Fischer and K. Shenai, "Dynamics of power MOSFET switching under unclamped inductive loading conditions," *IEEE Trans. Electron Devices*, vol. 43, no. 6, pp. 1007–1015, Jun. 1996, doi: 10.1109/16.502137.
[8] K. Fischer and K. Shenai, "Electrothermal effects during unclamped inductive switching (UIS) of power MOSFET's," *IEEE Trans. Electron Devices*, vol. 44, no. 5, pp. 874–878, May 1997, doi: 10.1109/16.568052.
[9] K. Chinnaswamy, P. Khandelwal, M. Trivedi, and K. Shenai, "Unclamped inductive switching dynamics in lateral and vertical power DMOSFETs," in *Proc. Ind. Appl. Conf.*, Phoenix, AZ, USA, Oct. 1999, pp. 1085–1092, doi: 10.1109/IAS.1999.801639.
[10] A. Narazaki, K. Takano, K. Oku, H. Hamachi, and T. Minato, "A marvelous low on-resistance 20V rated self alignment trench MOSFET (SAT-MOS) in a 0.35 μm LSI design rule with both high forward blocking voltage yield and large current capability," in *Proc. Int. Symp. Power Semicond. Devices ICs*, May 2004, pp. 393–396, doi: 10.1109/WCT.2004.240223.
[11] C. Kocon, J. Zeng, and R. Stokes, "Implant spacer optimization for the improvement of power MOSFETs' unclamped inductive switching (UIS) and high temperature breakdown," in *Proc. Power Semicond. Devices ICs*, May 2000, pp. 157–160, doi: 10.1109/ISPSD.2000.856795.
[12] J. C. W. Ng *et al.*, "A novel low-voltage trench power MOSFET with improved avalanche capability," in *Proc. Power Semicond. Devices IC's (ISPSD)*, Jun. 2010, pp. 201–204.
[13] J. C. W. Ng *et al.*, "A new trench power MOSFET with an inverted L-shaped source region," *IEEE Electron Device Lett.*, vol. 31, no. 11, pp. 1284–1286, Nov. 2010, doi: 10.1109/LED.2010.2068032.
[14] S.-S. Kim, J.-K. Oh, and M.-K. Han, "A new trenched source power MOSFET improving avalanche energy," *Jpn. J. Appl. Phys.*, vol. 42, no. 4B, p. 2156, Apr. 2003, doi: 10.1143/JJAP.42.2156.
[15] I.-H. Ji *et al.*, "New power MOSFET employing segmented trench body contact for improving the avalanche energy," in *Proc. Power Semicond. Devices IC's*, Orlando, FL, USA, May 2008, pp. 115–118, doi: 10.1109/ISPSD.2008.4538911.
[16] *Taurus Medici User Guide, Version D-2010.03*, Synopsys Inc., Mountain View, CA, USA, Mar. 2010.
[17] J. Lutz, H. Schlangenotto, U. Schlangenotto, and R. De Doncker, *Semiconductor Power Devices: Physics, Characteristics, Reliability*. New York, NY, USA: Springer-Verlag, 2011, pp. 358–360.
[18] S. E. J. Mahabadi, A. A. Orouji, P. Keshavarzi, and H. A. Moghadam, "A new partial SOI-LDMOSFET with a modified buried oxide layer for improving self-heating and breakdown voltage," *Semicond. Sci. Technol.*, vol. 26, no. 9, Jul. 2011, Art. no. 095005, doi: 10.1088/0268-1242/26/9/095005.

BING WANG received the B.S. degree from Southwest Jiao Tong University, Chengdu, China, in 2015, where he is currently pursuing the M.S. degree in microelectronics. His current research interests include TCAD and modeling of silicon power devices, wide bandgap power devices, and smart power ICs.

ZHIGANG WANG received the Ph.D. degree in microelectronics and solid state electronics from the University of Electronics Science and Technology of China in 2013. In 2013, he joined Southwest Jiao Tong University. His current research interests include TCAD and modeling of silicon power devices, wide bandgap power devices, and smart power ICs.

JAMES B. KUO (S'85–M'85–SM'92–F'00) received the B.S.E.E. degree from National Taiwan University, Taipei, Taiwan, the M.S.E.E. degree from Ohio State University, Columbus, OH, USA, and the Ph.D. degree from Stanford University, Stanford, CA, USA. He is currently a Professor with the Department of Electrical Engineering, National Taiwan University. His current research interests include low-voltage CMOS circuits and compact modeling of SOI CMOS devices.