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Dual-Surface Modification of AlGaN/GaN HEMTs Using TMAH and Piranha Solutions for Enhancing Current and 1/f-Noise Characteristics

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ABSTRACT We demonstrated dual-surface modification of GaN/AlGaN/GaN high-electron mobility transistors using tetramethylammonium hydroxide (TMAH) and piranha solutions prior to gate metallization. The TMAH-treated device exhibits improved performances with lower I-V hysteresis, in off-state leakage current and gate leakage current. The device performances were further significantly improved with applies additional piranha solution treatment right after the TMAH treatment, especially in hysteresis and 1/f-noise characteristics. It is found that the Schottky barrier height is high and ideality factor is low measured from I-V characteristics for the TMAH and piranha solution treated device. Reasonable gate leakage mechanisms were also discussed using Poole–Frenkel and Schottky emissions. In addition, it is observed that the magnitude of interface state density for the TMAH treatment after the piranha solution treated device shows significantly low compared to other devices. These excellent device-performances are observed due to the reason of dual-surface treatment which effectively decreases the surface trap density with an appropriate etching and passivation of the device surface exposed prior to the gate metallization.

INDEX TERMS AlGaN/GaN, HEMTs, dual-surface treatment, counter-clockwise hysteresis, 1/f-noise characteristics.

I. INTRODUCTION

AlGaN/GaN-based high-electron mobility transistors (HEMTs) are attractive devices for high power and radio frequency applications because of remarkable material characteristics related to III-nitrides such as wide energy band-gap, high breakdown electrical field, and high saturation velocity [1], [2]. However, the performances of the devices are inherently limited by the surface conditions. It is therefore essential to remove the native oxide layer from the device surface and stabilize the surface. Many efforts such as *in-situ* or *ex-situ* wet etching, dry etching, and pre/post annealing [3] were given to improve the device performances. Various wet chemical solutions such as hydrogen fluoride (HF), hydrochloric acid (HCl), sulfuric acid (H_2SO_4), and hydroxide-based solutions such as NaOH, KOH and TMAH have been widely used as a method of the surface treatment on the AlGaN/GaN HEMTs [3]–[10]. The surface treatment, however, can generate N (or Ga) deficiency on the (Al)GaN surface and hence can alter the surface state density through the formation of donor (acceptor)-like states [3]–[4], which is strongly related to the device performances.

Many experimental studies have reported to enhance the device performance of the GaN related devices using TMAH surface treatment [11]–[14]. In particular, before depositing insulating dielectric material such as Al_2O_3 must remove

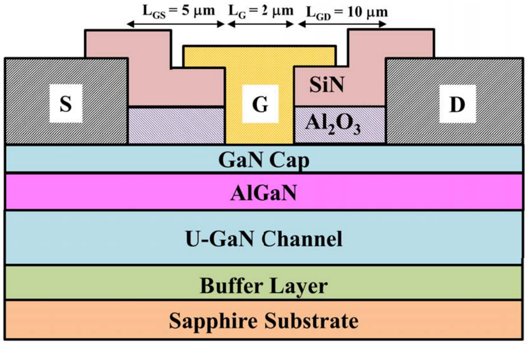

FIGURE 1. Schematic illustration of the proposed GaN/AlGaN/GaN HEMTs.

native oxides, carbon and other contamination while leaving the surface smooth. Thus, reducing contamination (for example: particulate, chemical and metallic) is significant factor for fabricating high performance devices, as this prevents gate oxide breakdown, reduce contact resistance, and minimize threshold voltage shift. Furthermore interesting advanced surface modifications have been applied to develop high performance device concept called dual-surface modification [15]–[18].

Piranha solution, a strong oxidizing agent and it will remove organic materials (i.e., photoresist residue), and it will also hydroxylate semiconductor surfaces to make them highly hydrophilic nature. Few researchers have used piranha solution treatment for the fabrication of prior to Al_2O_3 deposition on GaN devices [7]–[19]. Nepal *et al.* [7] reveal that the GaN surface by piranha treatment produced the lowest total trapped charge density and smoothest Al_2O_3 films. Their findings motivated our study to investigate the effect of surface treatment using piranha solution after TMAH treatment. The purpose of utilizing this type of combination treatment is, further smoothing the roughened surface; remove the carbon contamination, and effective neutralization of the surface caused by the piranha solution. Until now, dual-surface modification based on TMAH treatment after using piranha solution has not been explored as a surface treatment on GaN-based devices.

With this aim in mind, in this work, we have fabricated GaN/AlGaN/GaN HEMTs by utilizing TMAH and piranha solutions as dual-surface treatment before the gate metallization. The reference device with conventional buffered oxide etchant (BOE) surface treatment was also fabricated to compare the effects of the surface treatments on the I-V and C-V, characteristics, and the 1/f-noise performances of the AlGaN/GaN HEMTs.

II. GROWTH AND DEVICE FABRICATION

Fig. 1 shows schematic structure of the AlGaN/GaN heterostructure grown on sapphire substrate by metal-organic chemical vapor deposition (MOCVD). The thicknesses of the GaN cap and AlGaN barrier layer are 3 and 14 nm, respectively. Hall effect measurement showed carrier density of 8.8×10^{12} cm^{-3} and electron mobility of 1800 $cm^2/V{\cdot}s$.

For device fabrication, the active region was isolated by transformer-coupled plasma reactive-ion etching (TCP-RIE) using BCl_3/Cl_2 mixture. Before ohmic metallization, an 8 nm-thick Al_2O_3 layer was deposited by using plasma-enhanced atomic layer deposition (PEALD) to protect the device surface during high-temperature rapid thermal annealing (RTP) [20]. Si/Ti/Al/Ni/Au (1/25/160/40/100 nm) metal stack-layers were deposited for the ohmic contact and followed by RTP at 800 °C for 30 s in N_2 ambient. Then, 50 nm-thick Si_3N_4 layer was deposited by plasma enhanced chemical vapor deposition (PECVD) as a hard mask for the Al_2O_3 layer to protect from TMAH treatment and the gate region was defined and exposed with TCP-RIE. The surface treatments were performed in the TMAH solution (H_2O:TMAH = 5 : 1) for 8 min 30 sec at room temperature and followed by additional treatment in the piranha solution (H_2O_2:H_2SO_4 = 1 : 3) for 30 sec. For comparison, the reference device without the surface treatment was also prepared only employing the surface etching in buffered oxide etchant (BOE, H_2O:HF = 6:1) for 15 sec at room temperature to remove the native oxide layer from the surface. Finally, Ni/Au (30/200 nm) as gate metals were deposited. The gate length and width of these devices are 2 and 10 μm, respectively.

III. RESULTS AND DISCUSSION

Fig. 2(a) shows the transfer characteristics for the fabricated devices at V_D = 7 V. The threshold voltage (V_T) of the

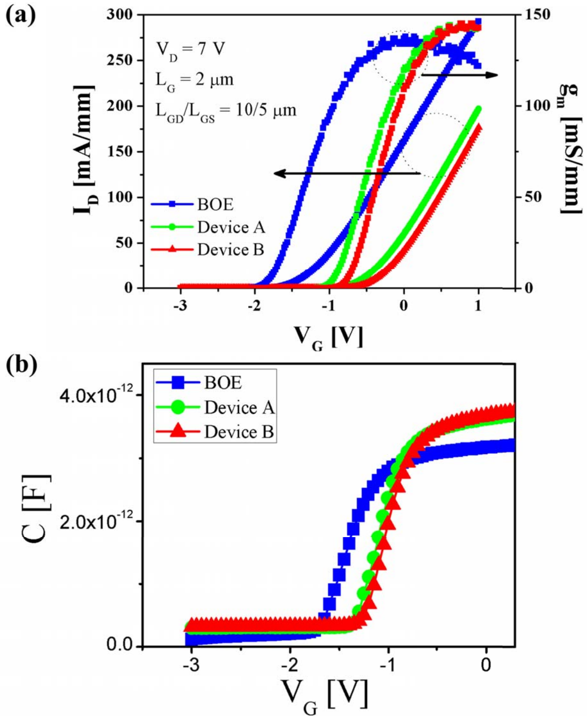

FIGURE 2. (a) I_D-V_G characteristics and transfer curve of all devices in the saturation region (V_D = 7 V). (b) Capacitance-voltage characteristics of BOE-treated and TMAH-treated HEMTs at room temperature.

TMAH-treated HEMT (device A) shifts in positive direction, compared to that of the reference device. The shift of V_T is also clearly observable from the C-V characteristics from the Fig. 2(b). The positive shift of V_T is due to the increased Schottky barrier height (SBH). The TMAH solution removes the native oxide layer formed on the GaN cap layer, such as Ga_xO, which would lead to a Ga deficiency on the surface. This explains the V_T shift in positive direction for the TMAH-treated device because the Ga deficiency on the surface forms acceptor-like states, which is responsible for the increase of SBH [4]. It is also noticed that the device with additional subsequent piranha treatment (device B) shows slightly shifted V_T further in positive direction. This is because the piranha treatment probably further stabilizes the TMAH-treated GaN surface with sulfur passivation effects [21]–[22].

The subthreshold characteristics for devices at $V_D = 0.1$ V are shown in Fig. 3. The TMAH-treated devices (both A and B) exhibits the subthreshold swing of 72 mV/dec, almost half of the value of 140 mV/dec observed from the reference device. The off-state drain leakage currents of the TMAH-treated devices are nearly of $\sim 10^{-8}$ A/mm, approximately two orders lower than that of the reference device. The reason for the improved subthreshold characteristics and off-state drain leakage current is mainly due to the improved surface quality and the increased SBH (i.e., 0.56 eV, 0.72 eV and 0.76 eV for BOE, device A and device B) and decreased ideality factor (i.e., 3.44, 2.33 and 1.85 for BOE, device A and device B) with TMAH treatment. The SBH and ideality factor values were evaluated from the intercept and slope values of the forward gate I-V characteristics using thermionic emission theory [23]. The increased SBH in the TMAH-treated devices apparently results in the reduced gate leakage currents shown in the Fig. 3.

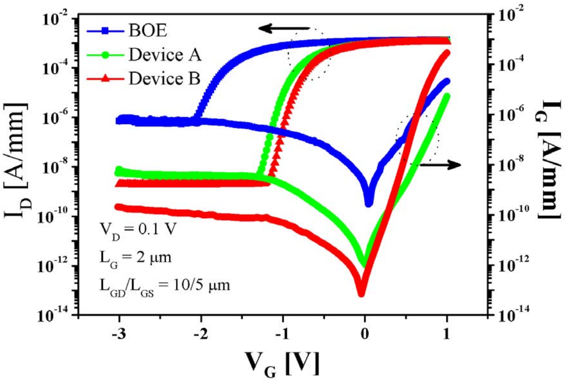

FIGURE 3. Semi-logarithmic scale of drain and gate currents versus gate voltage in fabricated devices at $V_D = 0.1$ V.

The gate leakage mechanisms were analyzed using Schottky emission (SE) and Poole-Frenkel emission (PFE) models from the plots of ln (I_G) *vs.* $V_G^{1/2}$ as shown in Fig. 4. The gate current conduction mechanism when dominated by PFE is given by [24] and [25]

$$I_G = I_0 \exp\left(\frac{S_{PFE}\sqrt{V}}{kT\sqrt{d}}\right) \tag{1}$$

and the lowering the of Schottky barrier is [24]–[26]

$$I_G = A^* T^2 A \exp\left(\frac{-\phi_b}{kT}\right) \exp\left(\frac{S_{SE}\sqrt{V}}{kT\sqrt{d}}\right) \tag{2}$$

where S_{PFE} and S_{SE} are the Poole-Frenkel and Schottky emission lowering coefficients, respectively. The theoretical value of the S_{PFE} and S_{SE} can be defined as

$$S_{PFE} = \left(\frac{q^3}{\pi \varepsilon_0 \varepsilon_r}\right)^{1/2} \tag{3}$$

and

$$S_{SE} = \frac{1}{2}\left(\frac{q^3}{\pi \varepsilon_0 \varepsilon_r}\right)^{1/2} \tag{4}$$

The comparisons in Fig. 4 show that the conduction of device A is affected by SE at lower voltages up to 0.56 V (region I) and PFE at higher voltages above 0.56V (region II) whereas the device B is subjected to SE at very lower voltages up to 0.18 V (region I) and PFE at >0.18 V (region II). In general, PFE is closely related to tunneling of carriers and also is related to the wide distribution of traps in the band gap of dielectric materials. The traps may be related to impurities and/or structural defects which cause the enhancement in the trapping/de-trapping performance of the carriers. The

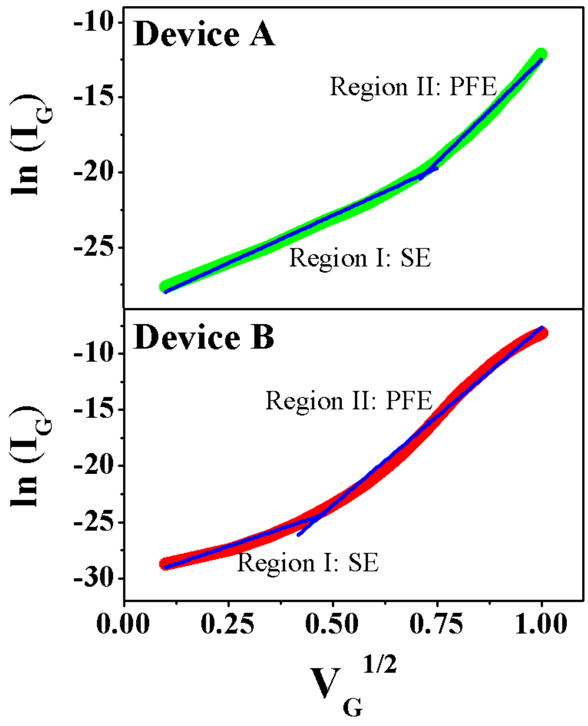

FIGURE 4. Plots of Log (I_G) *vs.* $V_G^{1/2}$ of device A and device B obtained from the gate leakage characteristics.

SE leads to current conduction through the contact interface rather than from bulk material. The better gate characteristics for the device B are directly related to reduction of the interface state density and the decrease in tunneling probability over the device operation. In general, as a barrier height increases the tunneling probability is decreases [27].

Fig. 5(a) shows the hysteresis characteristics. For the forward sweep, the gate voltage (V_G) was changed from – 3 to 1 V at $V_D = 0.1$ V and vice versa for the reverse sweep. The TMAH-treated devices (device A and B) exhibit less hysteresis than the reference device, as expected from the improved surface quality explained above. It is noticed that the TMAH-treated devices exhibit a counter-clockwise type hysteresis which is unusual compared to the hysteresis characteristics observed from most AlGaN/GaN HEMT devices similar to the case of the reference device in this work. The reason for the counter-clockwise hysteresis is because the surface states formed with the TMAH treatment become acceptor-like [4], [5] while the surface states of the device without TMAH treatment become donor-like. Moreover, the device B exhibited almost low hysteresis of -9.9 mV (the data of device A and B are clearly shown from the Figs. 6 (b) and (c)) due to the effective neutralization of the surface caused by the sulfur passivation. For the surface with donor-like surface states, when the gate voltage is high, surface states become mostly filled with electrons and neutralized to deplete the 2DEG density in the channel [28], [29] and to decrease the channel current which results in clockwise hysteresis. For the surface with acceptor-like surface states, on the other hand, no surface states available to capture electrons at high gate voltage and electron density in 2DEG channel thus increases to increase the channel current which results in counter-clockwise hysteresis. Similar results of hysteresis behavior were found for GaN-based devices [29], [30]. The detailed device characteristics are summarized in the Table 1, including the interface trap density (D_{it}) and the current collapse due to the gate lag. D_{it} was extracted from the conductance method (from 10 kHz to 6 MHz). A ~40% reduction of the interface trap density of the device B is obtained compared to the device A. The gate lag effect was measured at $V_G = -3$ V and $V_D = 0$ V with pulse width/period of 500 μs/1 ms current collapse. The device B shows the lowest D_{it} and the smallest current collapse. Verifying the effectiveness of the dual surface treatment (i.e., piranha solution after TMAH treatment) is very critical to support our data. To meet this, we carried out the roughness of surface treatments using BOE, TMAH and dual-surface (TMAH + piranha) modification using atomic force measurements (not shown here). The measurement showed that the roughness is found to be 2.14, 1.31 and 1.20 nm for BOE, device A and device B, respectively.

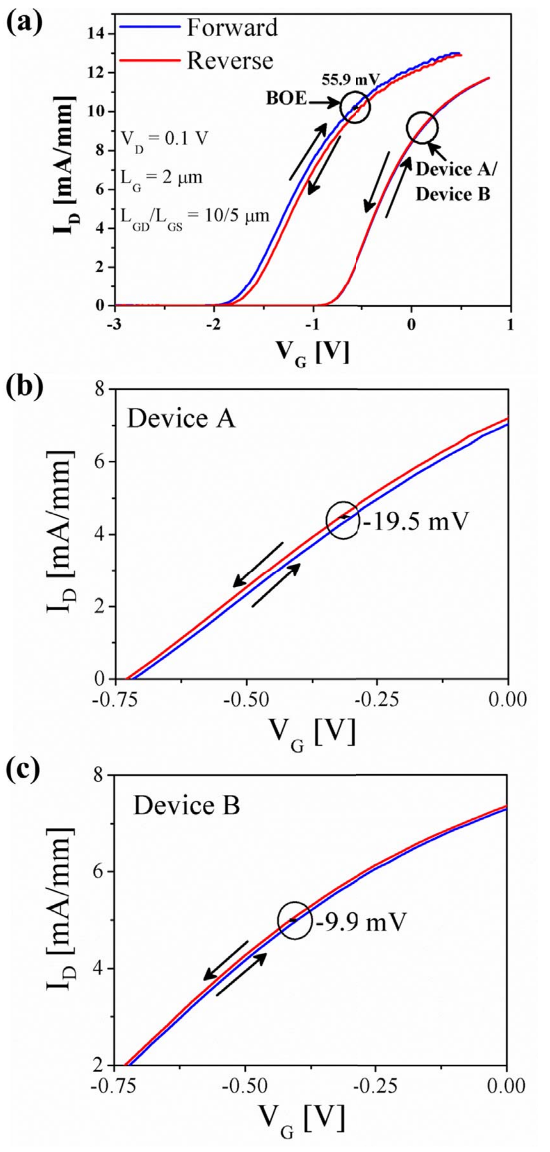

FIGURE 5. (a) Hysteresis characteristics of BOE-treated and TMAH-treated HEMTs, (b) device A and (c) device B at $V_D = 0.1$ V, respectively.

TABLE 1. Comparison of crucial device characteristics of the fabricated HEMTs with different surface treatments.

	Hysteresis (mV)	D_{it} ($cm^{-2}\cdot eV^{-1}$)	Current collapse (%)
BOE	55.9	1.33×10^{12}	53.7
Device A	–19.5	6.95×10^{11}	25.2
Device B	– 9.9	4.21×10^{11}	23.3

Next, the low frequency noise or 1/f-noise measurements are technologically inevitable to study impurity and trap-levels in semiconductor structures and to diagnose the standard quality and reliability of semiconductor devices [31]–[32]. Fig. 6 shows the 1/f-noise characteristics, measured at $V_D = 0.1$ V, V_G - $V_T = -0.35$ V, and $f = 10 \sim 10^3$ Hz. In 1/f-noise characteristics, the variation of normalized spectral power density of voltage fluctuations with frequency is measured [31]–[33]. The noise spectra in Fig. 6 are rather Lorentzian-like ($1/f^{\gamma}$, $\gamma = 2$) due

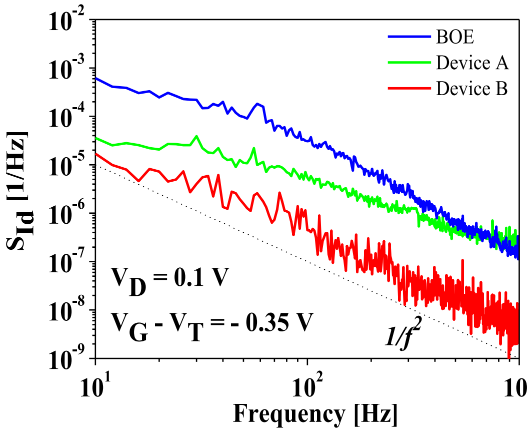

FIGURE 6. Normalized drain current spectral density (S_{Id}) as a function of frequency of all devices with different chemical treatments.

to generation-recombination (GR) noise or existence of trapping/detrapping centers. This is directly related to the presence of electron traps and/or detrapping between the 2DEG channel and traps in GaN buffer layer [34]. It was found that the S_{Id} of the device B is one order lower than that of the reference device and even the device A in all frequency ranges, as expected from the improved surface quality.

IV. CONCLUSION

We successfully demonstrated GaN/AlGaN/GaN HEMTs using TMAH and piranha solutions treatment prior to gate metallization and compared to other devices. The TMAH solution produces the acceptor-like state by resultant Ga deficiency and it enhanced the SBH, which result in the improved off-state performances. Furthermore, the additional piranha solution treatment decreases the surface states, and it improves device performance such as current, hysteresis and 1/f-noise characteristics. The relevant gate leakage mechanisms are explained by using Poole-Frenkel emission and Schottky emission. The interface state density obtained from the calculations based on the conductance method is quite sensitive to the TMAH and piranha solution treated device. These experimental results are significant for the development of high-performance GaN-based HEMT devices.

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