Received 1 March 2018; revised 9 April 2018; accepted 24 April 2018. Date of publication 8 June 2018;
date of current version 15 June 2018. The review of this paper was arranged by Editor M. Liu.

Digital Object Identifier 10.1109/JEDS.2018.2830999

Novel Computing Method for Short Programming Time and Low Energy Consumption in HfO_2 Based RRAM Arrays

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ABSTRACT This paper proposes a novel technique for reducing programming time and energy consumption in resistive random access memory (RRAM) arrays based on ramped voltage stress (RVS). RVS method is correlated to conventional constant voltage stress method (CVS) using an analytical model validating RVS as a reliable technique for switching time characterization in RRAM arrays. RVS method is optimized to reduce programming time and energy consumption providing a quantitative and qualitative link between programming method and tails improvement in memory arrays. Switching time distribution is much more controlled: half a decade using optimized RVS in comparison with ~3 decades distribution using conventional CVS method. Energy consumption is reduced by 4 orders of magnitude at $+5\sigma$ quantiles using our proposed technique compared to CVS.

INDEX TERMS Energy consumption, programming time, reliability, resistive random access memory (RRAM).

I. INTRODUCTION

Resistive random access memory (RRAM) technologies have experienced an increasing interest as next generation non-volatile memory devices. Thanks to their scalability [1] and performances such as fast switching speed [2], high retention [3], good endurance [4], and great compatibility with CMOS technology [5], RRAM are believed to become a good choice for Storage Class Memory (SCM) [6], [7]. Lots of efforts have been done lately trying to identify the pros and cons of different RRAM technologies at device level [8]–[12] or memory arrays prototypes [13]–[15]. To achieve extremely high density, RRAMs need to be connected together into memory arrays. Although sub 10 nm devices integration has been demonstrated [16], sneak paths through unselected devices are still an inherent disadvantage. Authors have proposed to introduce selectors in series with the switch in the memory cell [17], [18], others have presented complementary resistive switching (CRS) [19], [20] to solve the problem. However, technological and physical comprehension challenges need to be overcome before considering this solution at an industrial level. Due to its CMOS compatibility [5] RRAM can be integrated with a transistor into what is called 1-transistor-1-resistor (1T1R) array architecture. This structure has been identified as an efficient solution for sneak path current problem in memory arrays and it is particularly adapted to embedded memory applications where lower densities are required. In this work we use 1T1R configuration to focus on RRAM behavior without being affected by back-end selector properties.

With all the features presented above, RRAM is considered a viable technology for SCMs. However, one of the main challenges to be overcome before RRAM technologies can integrate the market is the large programming time (T_{prog}). Large programming time affects system performances, in particular its programming energy.

There have been several studies on switching time characterization for reliability prediction [21]–[24]. Switching time measurements for RRAMs have been reviewed and compiled in [25]. For reliability evaluation in RRAM technologies,

conventional characterization methods for oxides are traditionally used. Conventional constant voltage stress (CVS) is widely used to evaluate time to breakdown (t_{bd}) in oxides, and thus RRAM switching time [26], [27]. On the other hand, ramp voltage stress (RVS) has been considered as the workhorse of oxides measurements. It is a fast measurement method which can provide breakdown strengths of the device with good resolution [26], [28]. CVS being time and power consuming, RVS has been widely adopted as a powerful tool to replace CVS in t_{bd} evaluation.

In [29] the energy dissipation of RRAMs was discussed and experimentally shown using CVS measurements that the lowest energy is obtained with the fastest switching events. Here, in the aim of reducing programming time and consequently energy consumption in memory arrays, new programing paradigm is optimized to identify switching time in RRAM for SET and RESET mode. In this article, we refer to SET mode as the switching from a high resistive state (HRS) to a low resistive state (LRS), and RESET as the switching from LRS to HRS.

Our study is organized as follows: first, based on a comparative study including an analytical model, RVS measurement method is validated as an efficient method to characterize switching time in RRAM programming schemes. Afterwards, RVS is optimized to reduce programming time mean value and dispersion in 4kb 1T1R memory arrays. Energy consumption is quantified and compared for several patterns. Impact of tails is discussed for all investigated programming schemes.

II. EXPERIMENTAL PROCEDURE

RRAM technology was integrated in 4 kb arrays. The stack was deposited using Atomic Layer Deposition (ALD) where 5nm of Hafnium dioxide (HfO_2) was deposited on top of TiN Bottom electrode (BE). Ti/TiN bilayer structure was deposited as top electrode (TE) by Physical Vapor Deposition (PVD). Devices are integrated in 1T1R configuration using 130 nm CMOS transistor as selector (figure 1). Aiming the validation of RVS as an efficient method to characterize switching time in RRAM devices, we start by applying CVS method as a reference, CVS being frequently used to identify the time to breakdown in oxides [26]. In our study, CVS is used to characterize RRAM switching time (T_{switch}). Then RVS, known as an efficient method to characterize breakdown voltage [28] is applied for switching voltage (V_{switch}) evaluation. Thus, switching voltage will be converted to switching time using an analytical model [21], [28], [30] and compared to switching time in CVS. The interrelation between CVS and RVS systems has been discussed in [31], also providing an analytical model. Measurements are done on 4kb 1T1R arrays. At first, a smart forming (sequence of increased voltage pulses with 0.1V read between each pulse) is applied on fresh RRAM devices. The pattern is stopped once a predefined resistance value is achieved. Once the devices are formed (pristine state to LRS), a sequence of 20 RESET/SET pulses are applied to ensure cycling ability (preconditioning). CVS and RVS are applied after preconditioning step.

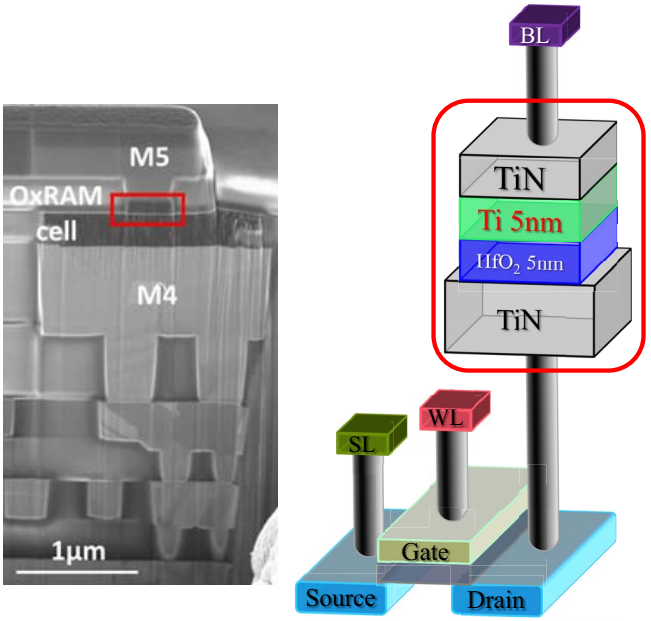

FIGURE 1. Scanning Electron Microscopy (SEM) cross section of RRAM cell integrated on top of Metal 4 level and a schematic representing the 1T1R device.

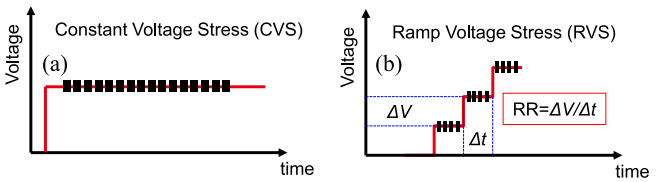

FIGURE 2. (a) Schematic of Constant Voltage stress (CVS), various voltages are applied in our study. (b) Schematic of Ramp Voltage Stress (RVS). Ramp Rate (RR) is a key factor for fast reliability tests.

A. CONSTANT VOLTAGE STRESS (CVS)

In this approach, a constant voltage is applied to the device under test as shown in figure 2.a. Various voltages are applied in order to switch devices in both SET and RESET modes. The current through the device is measured until switching occurs.

Figure 3.a shows an example of current versus stress time (I-t) at a given voltage for both SET and RESET. Based on these curves, characteristics can be extracted. In our case, based on the technology, a fixed resistance criterion was chosen to identify switching in the oxide. This method is well known as a powerful method to assess reliability. However, accounting for oxide based RRAM switching variability [32], its major issue is being time and power consuming [26].

B. RAMP VOLTAGE STRESS (RVS)

RVS is a fast measurement method which can provide breakdown strength with good resolution. The principle of this

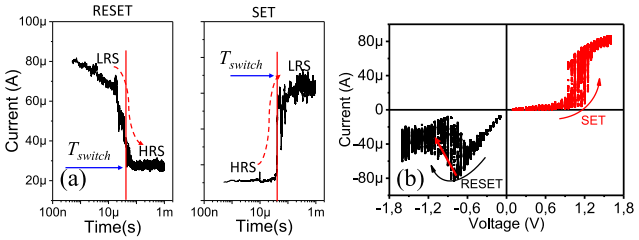

FIGURE 3. **(a) Current time characteristics during CVS measurements in both SET and RESET modes. Two fixed resistance values switching criteria were chosen for SET and RESET (respectively 20kΩ and 60kΩ) allowing to extract switching time. (b) Current voltage characteristics for SET and RESET switching obtained by RVS method. A resistance switching criterion was fixed for SET. As for RESET, switching is identified based on the inflection of the IV curves as indicated in the straight red arrow.**

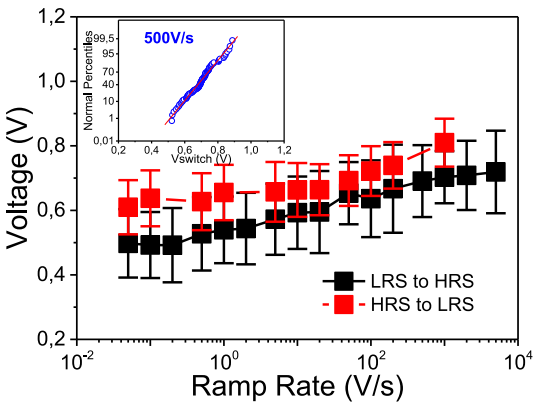

FIGURE 4. **Switching voltage as a function of RVS Ramp Rate (RR) for SET and RESET measured on 4kb array. In both cases, switching voltage increases with RR. Inset: example of switching voltage distribution in normal scale at a fixed RR. Tight switching voltage distribution is obtained (0.5V < V_{switch} < 0.9V).**

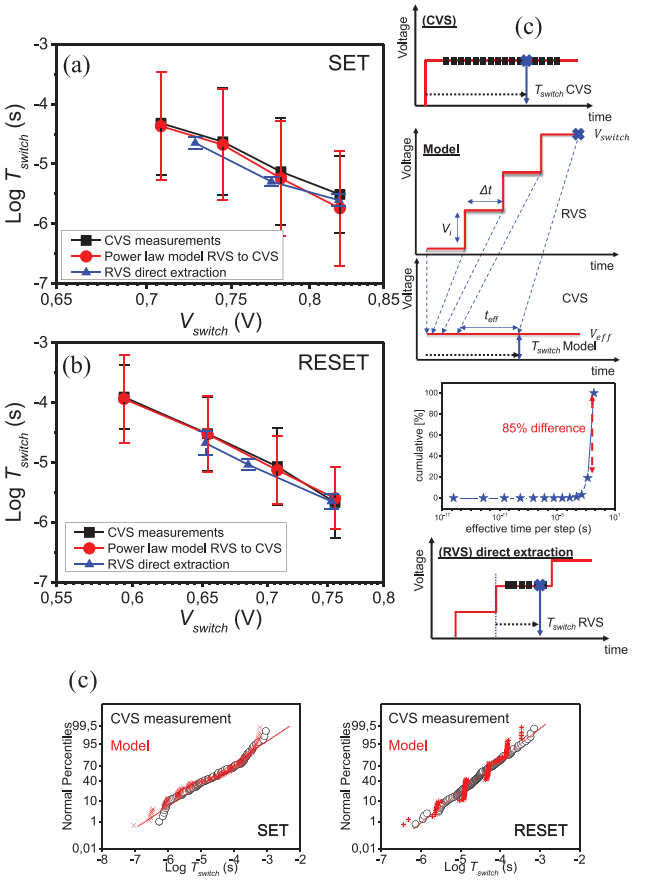

FIGURE 5. **(a) and (b) Switching time vs switching voltage characteristics for SET and RESET, respectively. Black squares represent the switching time extracted from CVS measurements (T_{switch}CVS) at a given applied voltage (switching voltage) as shown in the schematic top of (c). Red circles represent the calculated switching time using the analytical model based on the extracted switching voltage from RVS measurements as shown in the model representation (c). Each time step Δt at a given voltage Vi can be converted to an equivalent effective time (t_{eff}) at a constant effective voltage (V_{eff}) in CVS. Blue triangles are the switching time directly extracted from RVS measurements (T_{switch} RVS) using the non-cumulative effect based on calculated effective time per step as shown in (c). The step where the switching occurs contributes to up to 85% of the stress time. The initial time t = 0s is fixed at the beginning of the step where the switching occurs. Error bars represents ±1σ statistics in all cases. (c) from top to bottom, the extraction method in CVS measurements, schema representing the analytical model detailed in Section III-A, the effective time spent by step in RVS at an equivalent constant voltage in CVS and finally the RVS direct T_{switch} extraction based on the non-cumulative effect. (d) Examples of distributions in normal scale for measured switching time in CVS (T_{switch} CVS) at a given voltage (black empty circles) and converted time (red crosses) based on the analytical model (RVS switching voltage to effective CVS switching time) for both SET and RESET.**

method consists in increasing continuously the applied voltage until breakdown occurs (figure 2.b). The key factor of this method is the ramp rate (RR) defined as a constant voltage step (ΔV) over a constant time step (Δt). RVS guarantees switching within a short time compared to CVS. Current response to the applied voltage is shown in figure 3.b. A fixed resistance criterion was optimized in order to extract SET and RESET switching voltage respectively. Figure 4 shows the increasing trend of switching voltage with RR in both SET and RESET. Switching voltage presented in Figure 4 is what the memory device (1R) undergoes in the 1T1R structure. Taking into account the voltage drop on the selected transistor, the voltage applied on the RRAM could be extracted. The inset of figure 4 shows the normal distribution of switching voltage for a given RR. The gradual voltage increase in RVS increases programming strength, reducing the impact of intrinsic RRAM switching time dispersion as it will be discussed in the next section. In the following, V_{switch} will refer to the RRAM voltage.

III. RESULTS AND DISCUSSION

To evaluate RVS as an efficient method for characterizing switching time in memory devices, switching voltage needs to be converted to an effective CVS switching time. Figure 5.a and b show the power law voltage time relation (black squares for CVS measurements). The power law acceleration model has been adopted as the best fit in ultrathin oxides [33], [34]:

$$t_1 = t_2 \left(\frac{V_2}{V_1} \right)^n \tag{1}$$

where t_1, t_2 and V_1, V_2 are respectively switching times and voltages for two different CVS measurements. Exponential

law for t_{bd} voltage dependence has been historically used for reliability extrapolation. However, this law becomes questionable for ultra-thin oxides. Wu *et al.* have demonstrated that t_{bd} (V) exponential law can yield unphysical results [34], hence our choice of power law.

A. ANALYTICAL MODEL

RVS method is equivalent to a series of discrete CVS with linearly ascending voltage (figure 5.c). Each time step Δt at a given voltage V_i can be converted to an equivalent effective time (t_{eff}) at a constant effective voltage (V_{eff}) as in [30].

$$t_{eff} = \Delta t \left(\frac{V_i}{V_{eff}} \right)^n \tag{2}$$

By integrating all RVS time steps (Δt) until switching voltage, we can obtain the equivalent switching time for an effective voltage in CVS:

$$T_{switch} = \frac{Veff}{RR\,(n+1)} \left(\frac{V_{switch}}{V_{eff}} \right)^{n+1} \tag{3}$$

V_{switch} is the switching voltage in RVS for a given ramp rate RR. n can be extracted from power law fitting (1) for CVS measurements in figure 5.a and b (13 for SET and 18 for RESET). As we can clearly see, the calculated switching time based on the presented model using RVS measurements are in perfect match with CVS measurements in both SET and RESET modes (red circles in figure 5.a and b).

As effective time increases with V_i at each step in RVS according to (2), we have noticed that the step time where the switching occurs presents the highest contribution to the total calculated switching time. In Figure 5.c we show an example of calculated effective time per step (a graphical illustration of equation (2)) where we can clearly see that the step where switching occurs in RVS contributes to up to 85% of total stress time. In other word, Δt of the step where the switching occurs dominates total stress time. Based on this observation, we consider that RRAM device undergoes electric stress only at the step where V_{switch} occurs. Therefore, switching time can directly be extracted at 1st order from RVS measurements by considering a non-cumulative effect.

The initial time $t = 0$s is fixed at the beginning of the step where V_{switch} is detected (inset of figure 5.c).

This method can be considered as a reliable approximation for T_{switch} extraction as can be noticed in figure 5.a and b. Switching time directly extracted from RVS measurements (blue triangles in figure 5.a and b) shows a very good agreement with switching time measured by CVS and calculated based on RVS. Figure 5.d presents distributions examples in normal scale for measured switching time (CVS) and converted time (RVS switching voltage to effective CVS switching time) for both SET and RESET.

Moreover, based on the error bars in figure 5 a and b and the cumulative distributions in figure 5 d, we can clearly see the impact of intrinsic RRAM variability on switching time (up to three orders of magnitude variation). On the other hand, due to the tight distribution of switching voltage using RVS method (inset of figure 4), the variance of switching time using this method is drastically reduced [32] as we can clearly see based on the error bars of the time extracted from RVS (blue curves in figure 5 a and b).

Based on these results, it is possible to quantify RRAM performances in terms of programming speed depending on the applied voltage. Moreover, investigations at lower voltages allow to analyze RRAM intrinsic immunity to read disturb, and to extrapolate the maximum number of reading operations a RRAM technology can sustain for a given reading voltage and time before failure.

B. RVS TO REDUCE PROGRAMMING TIME

As shown in the previous section, RVS can be considered as an efficient and fast [26] method to characterize switching time in RRAM arrays. According to experimental results coupled to phenomenological model observations, this method is confirmed as a powerful tool to extract (V_{switch}, T_{switch}) without specific conversion need. In this section, we show how, based on the chosen RRAM technology and the size of the memory array, optimizing RVS could lead to programming time reduction.

As clearly noticed in our experimental results, conventional CVS method leads to wide switching time spread (up to 3 decades spread at $\pm 2\sigma$ in figure 5.d). On the other hand, as clearly seen in the inset of figure 4, V_{switch} distribution is very tight in RVS ($0.5\text{V} < V_{switch} < 0.9\text{V}$ for 99% of RRAM cells). Based on this advantage, RVS is optimized to reduce programming time as follows:

- First, RR is aggressively increased.
- Second, knowing RRAM switching voltage distribution, ramp starting voltage can be chosen depending on the size of the memory array.

Figure 6.a shows the distribution of V_{switch} of an RVS measurement for RR=140kV/s in RESET mode (blue dots). For $\pm 2\sigma$ statistics, V_{switch} spread is of the order of 0.25V. Start and stop points are identified. RVS measurement consists in a ramp where a voltage is increasing with time (V-t relationship). In this case, the time spent between 0 and 0.5V is wasted, since the fastest device in the array switches at 0.5V.

Moreover, for $+2\sigma$ statistics, the slowest device in the array switches around 0.75V. Thus, for the chosen technology (HfO_2/Ti) at $\pm 2\sigma$ (representing the aimed size of the array) we need to apply a ramp voltage pattern between 0.5V and 0.75V to switch all the devices. Voltage above 0.75V could induce an unwanted electrical stress leading to potentially degraded reliability and higher power consumption. The red line shows the Normal spread of the switching voltage. Based on this trend, for a given technology at a given RR, start and stop voltages could be extracted for any given memory array size (figure 6.a). In Figure 6.b and c we can clearly see the impact of optimized RVS ($V_{start} > 0$ and $V_{stop} < V_{max}$) on programming time spread compared to conventional CVS

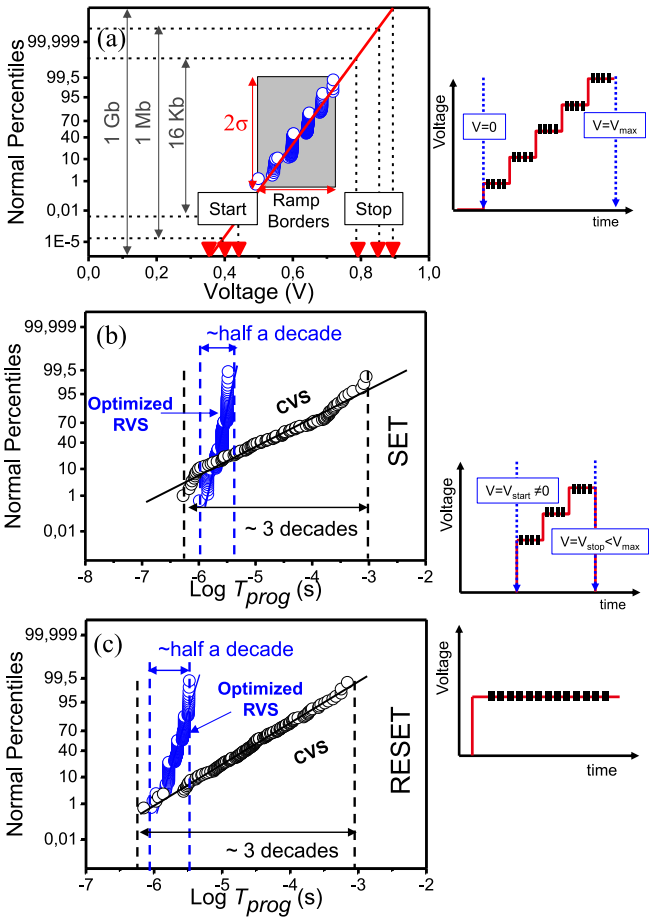

FIGURE 6. (a) Switching voltage distribution in normal scale extracted from RVS measurements on kb array at RR=140kV/s. the first switching point is situated around 0.5V. As RVS measurement consists in a ramp where a voltage is increasing with time, the time spent below 0.5V is wasted (below 0.5V is not needed for switching). On the other hand for a given memory size (± n*σ), ±2σ in this example, voltage above 0.75V is not needed because all of the aimed cells have switched before. Based on the normal trend of switching voltage distribution (red line) the starting and stopping voltages are extracted for different memory array size (up to 1Gb in this example) (b) and (c) represent the distribution of programming time measured by conventional CVS method and the optimized RVS method for SET and RESET respectively. The optimized RVS method gives one order of magnitude improvement of programming time at median and 5 order of magnitude improvement of tails @ + 2σ. On the right side, the schema of patterns used in this study.

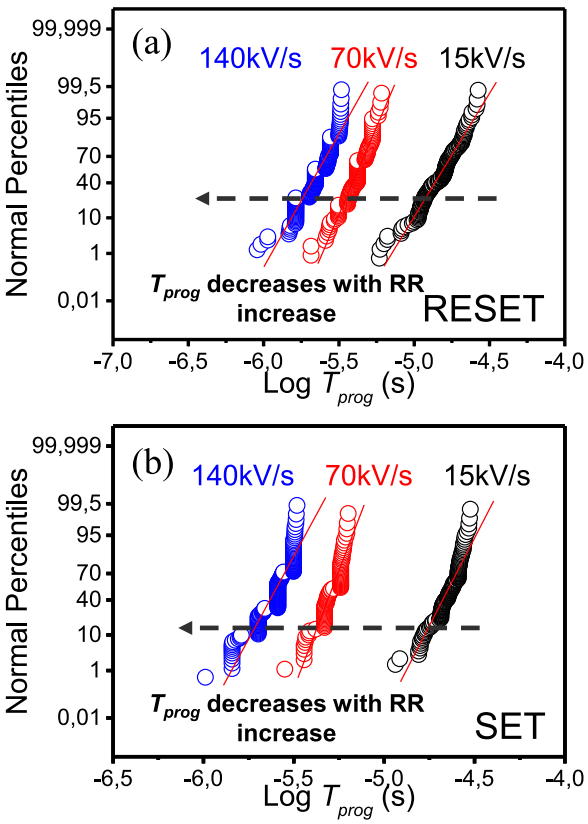

FIGURE 7. (a) and (b) show how by increasing RR in RVS pattern we decrease the programming time in RRAM array for both RESET and SET.

method. In these measurements, voltage ramp was applied between 0.5V and 0.75V as illustrated in the inset of figure 6.

While up to one decade decrease of programming time at median level is noticed using our method compared to CVS, a huge tails improvement is observed at $\pm 2\sigma$ statistics. Programming time spread is more than 3 times lower (3 decades vs half a decade for CVS and RVS respectively) for SET and RESET. In summary, typical programming time standard deviation in CVS is 2×10^{-4}s. On the other hand, with optimized RVS, programming voltage standard deviation is 0.5V, what corresponds to a programming time standard deviation pf 2.7×10^{-6} assuming RR=140kV/s. This result clearly demonstrates the advantage of RVS for fast RRAM programming efficiency.

In figure 7.b and 7.c we can clearly notice the impact of ramp speed on programming time in RRAM matrices. The fastest the RR is, the lower the programming time gets. In particular, about one decade of programming time improvement is reached when RR is increased from 15kV/s to 140kV/s in both SET and RESET operations.

C. ENERGY CONSUMPTION

In this section we discuss how reducing programming time impacts the energy consumption in RRAM arrays.

Energy consumption is estimated at the first order by [35]:

$$E = V_{switch} * I_{prog} * T_{prog} \tag{4}$$

V_{switch} and I_{prog} being the programing voltage and current, respectively, and I_{prog} the highest current during the switching process. During SET, current is low as RRAM is initially in the high resistive state before switching. During RESET, RRAM is initially ON and the programming current flows through the device. Energy consumption increases with programming time increase. Based on the results obtained with the optimized RVS pattern, energy consumption in SET and RESET was calculated (figure 8). Comparison is made between optimized RVS and CVS. Two advantages of optimized RVS over CVS could be identified: 1) more than one

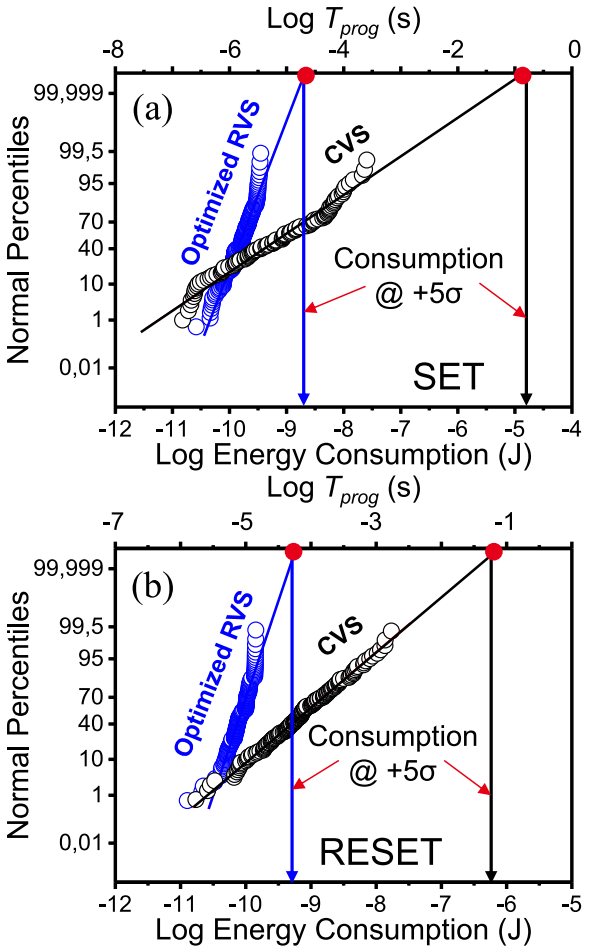

FIGURE 8. (a) and (b) Programming time and corresponding calculated energy consumption in RRAM array for SET and RESET using CVS and optimized RVS. While more than 3 decades improvement of programming time at bit tails (+5σ) using the optimized RVS method, more than 4 order of magnitude difference of energy consumption is obtained between conventional CVS and the proposed RVS programming at +5σ in SET and RESET.

order of magnitude of median energy consumption reduction for both SET and RESET. 2) Huge tail reduction in RVS, up to 4 orders of magnitude improvement at $+5\sigma$ statistics could be identified.

In this comparative study RR=140kV/s (total pattern duration = 3µs) is used in RVS method. Based on (4), using 50ns plateau durations leads to lower energy consumption (500 fJ and 1pJ for SET and RESET respectively [32]). Reducing tails consumption is a key factor toward integrating a technology in large-scale arrays. Moreover, we believe that for energy consumption reduction, reducing programming time is more effective than reducing programming current [32], [34]. While the impact of the proposed programming method on performances such as endurance and retention stability needs to be deeply studied, we believe that our method could represent a solution for reducing programming time and energy consumption in RRAM arrays. In particular, we demonstrated in [36] that optimized RVS patterns with reduced voltage range significantly improves RRAM endurance due to lower stress applied to the RRAM stack.

IV. CONCLUSION

This paper discussed RVS technique for switching time characterization of RRAM kb arrays. Correlation with CVS method was found using a phenomenological model. Subsequently, RVS technique was optimized by adjusting start (>0) and stop ($<V_{max}$) voltages depending on the chosen technology and the memory array size. This new method improves programming time and reduces the tails in RRAM arrays for SET and RESET. Thus, switching time distribution is lowered from 3 decades to half a decade using optimized RVS patterns. Finally, energy consumption was reduced by 4 orders of magnitude in RRAM arrays at $+5\sigma$ statistics. Using this programming method with aggressive RR ($\sim$ 50ns pattern time could reduce energy consumption to sub pJ.

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GILBERT SASSINE, photograph and biography not available at the time of publication.

CARLO CAGLI, photograph and biography not available at the time of publication.

JEAN-FRANÇOIS NODIN, photograph and biography not available at the time of publication.

GABRIEL MOLAS, photograph and biography not available at the time of publication.

ETIENNE NOWAK, photograph and biography not available at the time of publication.