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In-Line Tunnel Field Effect Transistor: Drive Current Improvement

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ABSTRACT A new architecture of tunnel field effect transistor (TFET) with in-line (vertical) tunneling area is introduced. By adding the vertical tunneling area, the in-line TFET architecture outperformed the normal TFET in terms of the drive current, the subthreshold swing, and the intrinsic time delay, etc. The drive current of the in-line TFET is enhanced nearly 7× compared to the conventional TFET. It also shows a significantly reduced subthreshold swing of 37.2 mV/dec.

INDEX TERMS TFET, in-line tunneling, silicon, vertical structure, tunneling distance, tunneling probability.

I. INTRODUCTION

Modern, semiconductor technology has developed with a continued miniaturization of transistor dimension to increase circuit density and functionality over past two decades. Although improved performances have been provided by device scaling, since the supply voltage (V_{DD}) cannot be scaled proportionately with transistor scaling, power per unit area of a chip has gradually increased as well. In order to achieve low leakage current in the scaled devices, a reduction of the subthreshold swing (SS) is required and considered as one of the most important challenges. Therefore, a variety of new emerging device structures has been suggested to overcome the scaling limitation of the conventional transistors. In particular, tunneling field effect transistor (TFET) has been considered as a potential successor of metal oxide semiconductor field effect transistor (MOSFET) and attracted intense attention due to its band-to-band tunneling (BTBT) transport model which has less electron thermal voltage (kT) dependence [1]–[6]. Until now, low SS (less than 60 mV/dec) of TFETs have been suggested theoretically and experimentally [6], [7]–[10].

Even though reduction of SS of TFET has been demonstrated, just few studies have suggested several approaches to improve the drive current. Improving drive current is also an important challenge, since the overall circuit speed can be effectively improved by increasing the drive current.

In the conventional MOSFET, scaling is the most effective approach to increase the drive current [11]. But, as the dimension scaled to the nanometer regime, since the gate oxide is also scaled down to a thickness of only a few atomic layers, we confront a problem of the rapid rise in standby power. Meanwhile, in the TFET, the device performance improvements can be realized with different approaches: lower band gap source, lower equivalent oxide thickness (EOT), and achieving more abrupt junction. Over above traditional approaches, introducing additional vertical tunneling (or line tunneling) region can be another countermeasure for low drive current of TFET.

Here we introduce an in-line TFET concept to utilize the combination of lateral and vertical tunneling area. The schematic of the in-line TFET is in Fig. 1(a). In the normal TFET, carriers are injected through the tunnel barrier with lateral tunneling (or point tunneling) model, in which carriers tunnel through from source to channel (Fig. 1(b)) [12]. Basically, lateral tunneling has low carrier BTBT generation rate due to the small tunneling area. On the other hand, in the vertical tunneling (or in- line tunneling) model, higher carrier BTBT generation rate can be achieved, providing higher tunneling current (Fig. 1(c)) [13], [14]. Especially, this model

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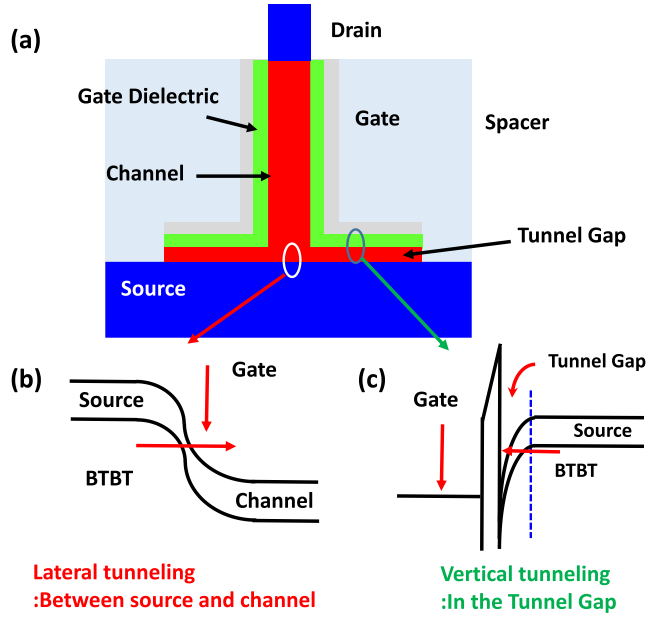

FIGURE 1. **(a) A schematic of the conceptualized silicon in-line TFET. The energy band diagram for (b) the lateral tunneling model with the source-to-channel direction and (c) the vertical tunneling model with the gate-to-source direction.**

can provide the information of the vertical tunneling from the valence band to the conduction band in Si [15].

The operation of the in-line TFET is described below. In the off-state, the potential barrier is very large and the resulting current (off-state current) is small. In the on-state, the gate voltage lowers potential barrier, resulting in carrier injection. There are different contributions of two main BTBT parts in the on-state. First, the lateral tunneling part, middle point of the tunnel-gap in the schematic, partially contributes to the total drive current. Second, the vertical tunneling part, the both side lines of the lateral tunneling part in the schematic, is the main factor which can mostly determine the device working.

Overall, by adding the vertical tunneling area, the in-line TFET architecture shows better performances over the normal TFET in terms of the drive current, the subthreshold swing (SS), and the intrinsic time delay, etc. We also observed the performance change with various channel doping concentration, showing the designed device can be optimized.

II. EXPERIMENT

To design and characterize the in-line TFET, Sentaurus technology on computer aided design (TCAD) was used based on the non-local BTBT model and hydrodynamic model to reflects the quantum-confinements in ultra-narrow parts (tunnel-gap parts) [16]. According to Sentaurus Device module manual, this model takes into account nonlocal trap assisted tunneling (TAT) process based on the exact tunneling barrier. The recombination, TAT, BTBT models for

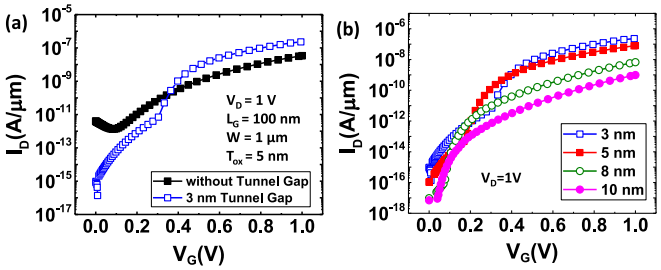

FIGURE 2. **(a) Comparison of transfer (I_D-V_G) characteristics of in-line TFET and normal (without tunnel-gap) TFET. (b) I_D-V_G for in-line TFETs with various tunnel-gap thickness from 3 nm to 10 nm.**

Si tunnel diode were previously studied [17]. Also, to consider thermal scattering, all device simulations incorporate the Phillips unified mobility model which takes into account temperature dependence of the mobility, electron – hole scattering, ionized impurities screening by charge carriers and clustering of impurities [16]. Our simulation was done with effective mass from the model Sentaurus offered. The effective mass is conduction band effective mass. On the silicon (Si) substrate, the line tunnel-gap (for vertical tunneling) and the channel (100 nm) are placed. The doping is also determined by the TCAD simulation. All source, channel and drain are normal Si with ~1.16 eV of bandgap. $N_A = 10^{20}$ cm^{-3} of boron acceptor was doped for the source. Drain and channel are doped with Arsenic donor active concentration $N_D = 10^{16}$ cm^{-3} and $N_D = 10^{18}$ cm^{-3}, respectively. The gate material is used with a work function of 4.0 eV and hafnium oxide (HfO_2) serves as the dielectric layer. Gate dielectric layer is 3.9 nm of HfO_2. We calculated EOT = 0.5 nm. The thickness of device is 1 μm. Channel length and width are 100 nm and 10 nm, respectively.

III. RESULT AND DISCUSSION

Fig. 2(a) shows the width normalized transfer characteristics (I_D-V_G) for an n-type Si in-line TFET with extremely steep doping profiles at the source/channel and drain/channel junctions. It is compared to a conventional TFET transistor (without tunnel-gap). Tunnel-gap thickness is 3 nm in the in-line TFET. Both devices show high I_{ON}/I_{OFF} ratio (the normal TFET: $I_{ON}/I_{OFF} > 10^4$ and the in-line TFET: $I_{ON}/I_{OFF} > 10^8$). It is observed that the in-line TFET with 3 nm tunnel-gap shows better performance than that of the normal TFET in terms of the drive current because it has the additional electron generating area. By adding the tunnel-gap line, a drive current increases by ~7 times. A drive current of 228.4 nA/μm can be achieved in the in-line TFET. Compared to this, the normal TFET of same L_g achieves 33.8 nA/μm of drive current. V_{TH} of the in-line TFET and the normal TFET is 0.736 V and 0.759 V.

At the same time, I_D-V_G was compared with different tunnel-gap thickness from 3 nm to 10 nm to find the optimized condition (Fig. 2(b)). It is to be noted that the drive current increases as the tunnel-gap thickness decreases. The higher performances of the in-line TFET and the differences

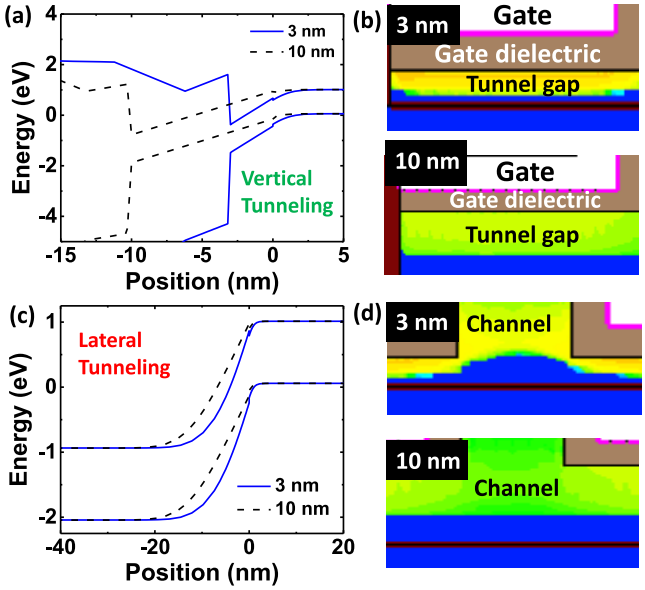

FIGURE 3. **(a) Band diagrams for 3 nm and 10 nm vertical tunnel-gap area and (b) their corresponding electron BTBT generation color maps. (c) Band diagrams for source-to-channel lateral tunneling points of 3 nm and 10 nm tunnel-gap thickness and (d) corresponding electron BTBT generation color maps at those points.**

among various tunnel-gap thickness might be attributed to the carrier generation efficiency through the tunneling barrier. Therefore, we investigated the band diagram and the electron BTBT generation rate in the vertical and lateral tunneling area.

Figs. 3(a) and 3(b) show the band diagrams and their corresponding electron BTBT generation color maps for 3 nm and 10 nm tunnel gap thickness. These band diagrams exhibit the vertical tunneling of electrons through the tunnel-gap barrier. The distance between the conduction band (CB) and the valence band (VB) edges of 3 nm and 10 nm tunnel gap is 3.59 nm and 5.57 nm, respectively. As the tunnel distance reduces, tunneling probability across the tunnel barrier might increase, achieving increased drain current.

It is understood that tunneling through the 3 nm tunnel-gap barrier is easier than 10 nm. At the source/channel lateral tunneling point, higher electron generation rate is observed in the 3 nm tunnel-gap with yellow color ($\sim 4\times10^{31}$ $cm^{-3}s^{-1}$), while the 10 nm tunnel-gap shows relatively less electron generation (4.6×10^{19} $cm^{-3}s^{-1}$ $\sim$ 4.4×10^{23} $cm^{-3}s^{-1}$). Investigation of the band diagrams and the electron BTBT generation rate with different thickness of tunnel-gap showed us that the drive current are enhanced with reduced tunnel-gap thickness.

Fig. 4(a) shows the correlation of SS and I_D for the normal TFET and the 3 nm tunnel-gap in-line TFET. The lowest SS points are 100.0 mV/dec and 37.2 mV/dec for the normal TFET and in-line TFET, respectively. A successfully reduced SS value was achieved in the in-line TFET. The difference of SS can be understood with the tighter electrostatic control of carriers in the tunnel-gap.

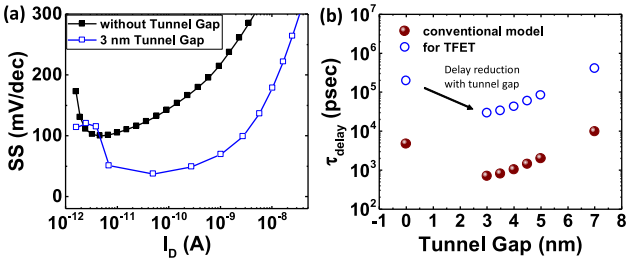

FIGURE 4. **(a) Comparison of the in-line and the normal TFET subthreshold slope. (b) Intrinsic device speed (CV/I) versus tunnel-gap thickness of the in-line TFETs.**

The intrinsic device speed (CV/I, τ_{delay}) of the in-line TFET with respect to the tunnel-gap thickness is shown in Fig. 4(b).

Generally, to evaluate the circuit speed, we use the drain current formula used in conventional Si MOSFET [18]–[20], but it differs from the model of TFET. We calculated τ_{delay} with conventional Si MOSFET and TFET models using effective capacitance and there is a clear difference. In conventional MOSFETs, both gate-to-source capacitance (C_{GS}) and gate-to-drain capacitance (C_{GD}) contribute half of the total charge in the linear region and C_{GD} value becomes smaller in saturation region. This leads to the result that the C_{GS} can mainly contribute to the gate capacitance (C_G). On the other hand, for TFETs, C_G can mainly dominated by C_{GD} due to the early pinch-off of the channel causing higher C_{GD}. More detail explanation was discussed in the reference [21]. τ_{delay} from the CV/I estimation for TFET is longer than that for conventional MOSFET by $\sim$ 41 times. τ_{delay} of the 3 nm tunnel-gap TFET is enhanced 7 times compare to the normal TFET for both models. This improvement is primarily due to the device current enhancement in the in-line TFET. Based on the data, it is estimated that the vertical tunnel-gap improved the electron BTBT generation, providing the increased drive current. Significant improvement of τ_{delay} is also observed as the tunnel-gap thickness decreases due to the reduced electron BTBT generation rate.

We described that the TFET performances can be improved by adding the tunnel-gap. It was also understood that the electrical performances are modulated with different tunnel-gap thickness. To give more information for device performance optimization, we conducted additional studies systematically by changing different electrical parameters and showed corresponding results.

First, drive current change with various boron doping concentration in the channel was estimated. Figure 5 and 6 indicate that band diagrams of the lateral and vertical tunneling area with various doping concentration from 10^{15} cm^{-3} to 10^{18} cm^{-3}. In the lateral tunneling region, the tunnel distance decreased from 4.92 nm to 3.94 nm as the doping concentration is changed from 10^{15} cm^{-3} to 10^{18} cm^{-3}. Tunnel distance reduction was also observed in the vertical tunnel region. The vertical tunnel distance also

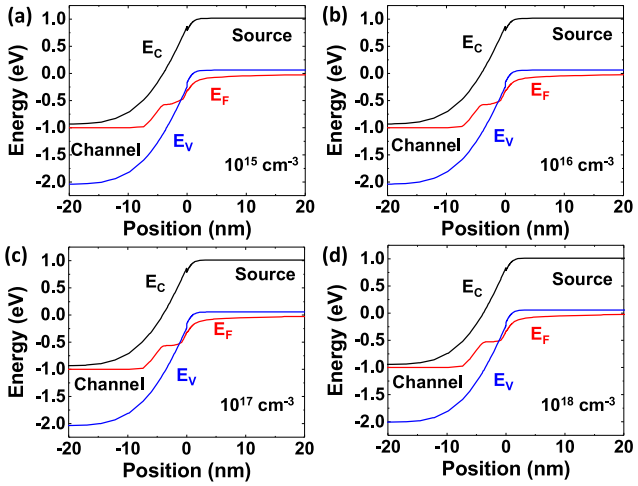

FIGURE 5. Band diagrams for later tunneling with various channel doping concentration.

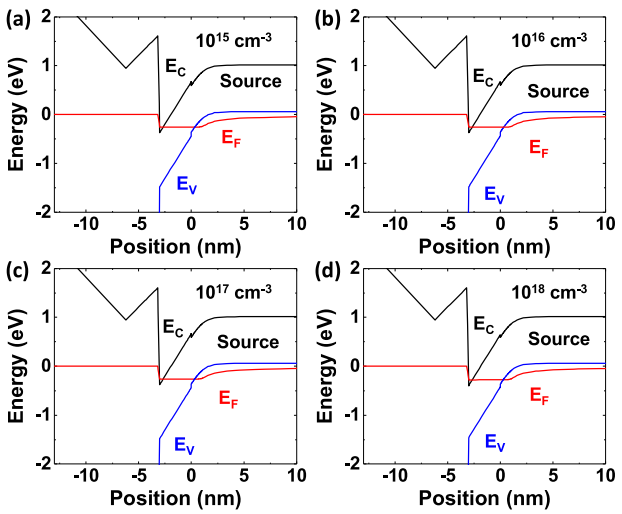

FIGURE 6. Band diagrams for vertical tunneling with various channel doping concentration.

TABLE 1. Summary of drain current for different doping concentration.

N_A (cm^{-3})	10^{15}	10^{16}	10^{17}	10^{18}
I_D (μA/μm)	0.226	0.228	0.239	0.326

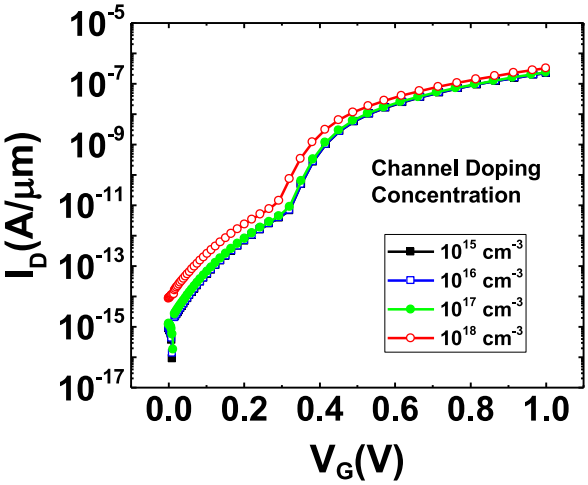

FIGURE 7. Transfer characteristics with various channel doping concentration.

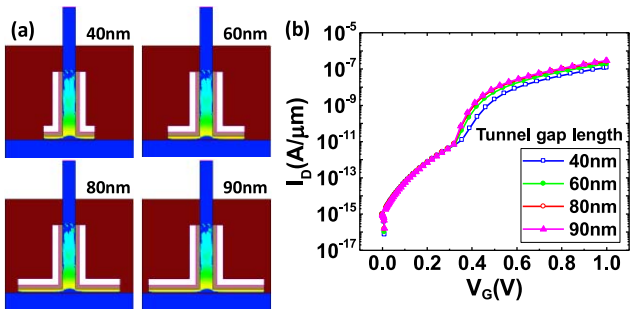

FIGURE 8. (a) Electron BTBT generation and (b) Transfer characteristics with various tunnel-gap lengths.

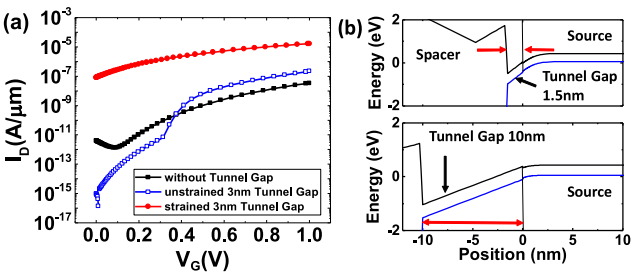

FIGURE 9. (a) Comparison of transfer (I_D-V_G) characteristics of normal (without tunnel-gap), unstrained and strained in-line TFETs (b) Band diagrams for strained Si vertical tunnel-gap area. Reduced band-gap energy and tunneling distance can be achieved with a strained Si condition.

decreased from 3.01 nm to 2.84 nm as the doping concentration is changed from 10^{15} cm^{-3} to 10^{18} cm^{-3}. As the channel doping increases, the Fermi-level becomes closer to the conduction band edge. This means that the band offset between the source and the channel becomes larger, resulting in that the distance between the conduction and valence band edge becomes smaller and tunneling probability can increase (Fig. 7). We summarize the drain current for various doping concentration in the Table 1.

Second, we compared the device performances with different tunnel-gap line lengths 40 nm ∼ 90 nm. In the above data in Fig. 2, we used the length of the horizontal section of the gate is 70 nm. Figure 8 (a) and (b) show the electron BTBT generation maps and corresponding transfer characteristics, respectively. The role of the tunnel-gap section of the gate is inducing the vertical tunneling. The horizontal gate induces tunneling from the valence band of source to the conduction band of source, which can boost the drive current and significantly reduces the OFF current values thus making the device concept appealing for low standby power (LSTP) devices. As expected, longer gate length can help with improving the drain current, achieving more excessive free carriers.

To observe the strain effects on our in-line TFET, we also compared the unstrained and strained Si cases. Figure 9(a) shows the comparison of I_D-V_G for the normal, unstrained and strained Si in-line TFETs. Device performance enhancement is clearly observed. Strained and unstrained Si in-line TFETs have 27.4 μA/μm and 224 nA/μm, respectively. Figure 9(b) shows band diagrams for strained Si. Reduced band-gap energy and tunneling distance can be achieved. Overall, dynamic nonlocal BTBT model includes physical models such as trap-assisted tunneling model and strain effect which we have to consider.

IV. CONCLUSION

In conclusion, we have introduced the concept of in-line vertical tunnel FET. It is observed that the in-line TFET (with tunnel-gap) outperformed the normal TFET (without tunnel-gap). In the in-line TFET structure, the additional tunnel-gap area where the vertical tunneling is occurring can boost the drive current. Reduced subthreshold swing and shorter intrinsic time delay (τ_{delay}) are other benefits. Combination of the lateral tunneling area and the additional vertical tunneling area is capable of delivering enhanced performance in a newly designed structure. Optimization of the in-line TFET is conducted by comparing various tunnel-gap thickness. It is observed that the drive current increases as the thickness of tunnel-gap decreases. With the shorter tunneling distance and the stronger electrostatic control, higher electron BTBT generation rate can be achieved in the thinner tunnel-gap. Additionally, we observed that device can be improved by optimizing the channel doping concentration and the tunnel-gap lengths.

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