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The Simulation Study of the SOI Trench LDMOS With Lateral Super Junction

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ABSTRACT A novel lateral double diffused metal oxide semiconductor (LDMOS) with trench oxide layer, featuring a lateral super junction structure based on the silicon-on-insulator technology is proposed. On the one hand, the lateral super junction combined with the TOL can enhance both the surface and the bulk electric field of the N-drift by the charge compensation. Thus, the breakdown voltage (BV) is improved. On the other hand, the N-Pillar of the lateral super junction provides another current channel for electrons at the forward conduction state, thus the Specific on resistance ($R_{on,sp}$) is decreased. As the simulation results show, the proposed LDMOS exhibits trapezoidal electric field distribution with BV of 422V, and double electron channels with $R_{on,sp}$ of 30.7 m$\Omega\cdot$cm^2, thus the figure of merit (FOM) (FOM = $BV^2/R_{on,sp}$, Baliga's FOM) of 5.82 MW/cm^2 is achieved, breaking through the silicon limit.

INDEX TERMS Lateral double diffused metal oxide semiconductor (LDMOS), breakdown voltage (BV), specific on resistance ($R_{on,sp}$), Baliga's figure of merit (FOM).

I. INTRODUCTION

The SOI-LDMOS (Silicon-On-Insulator Lateral Double-diffused Metal–Oxide–Semiconductor) is widely adopted in power ICs due to its voltage control and high switching frequency characteristics [1], [2]. Two key electrical parameters of LDMOS are the Breakdown Voltage (BV) and the Specific On Resistance ($R_{on,sp}$)[3]–[6]. However, the two parameters are contradicted from each other and the tradeoff can be expressed as $R_{ON} \propto BV^2$. The Baliga's Figure Of Merit (FOM) is used to evaluate the tradeoff relationship [7]–[12]. Many advanced structures are proposed to improve the FOM in recent years. Specifically, the LDMOS with Trench Oxide Layer in the N-drift region (TOL-LDMOS) is widely researched [13]–[17]. At reverse blocking state, the TOL can increase the BV significantly with the enhancement of the surface electric field and the expansion of depletion line in the N-drift region. However, at the forward conduction state, the electron current path of the device is distributed in U shape due to the TOL, which will increase the $R_{on,sp}$ obviously.

Meanwhile, the Super Junction technology is also widely adopted to enhance the bulk electric field of the N-drift region by the charge compensation, which can break through the relationship between the BV and $R_{on,sp}$ [9], [18]–[22]. In this paper, a TOL-LDMOS with Lateral Super Junction in the N-drift region is proposed to achieve better FOM for the BV and the $R_{on,sp}$.

II. THE DEVICE STRUCTURE AND MECHANISMS

The structure and mechanisms of the proposed TOL-LDMOS is shown in Fig. 1. Compared with a SOI LDMOS, a deep trench filled with oxide is inserted into the N-drift region, which is equivalent to the increase of thelength of the N-drift region. The Lateral Super Junction is designed with charge balance, and it is composed by two float P-Pillars and an N-Pillar. The doping of the N-drift region is 5×10^{14} cm^{-3}, the thickness T_d and the width W_d of the N-drift region are 25 μm and 17 μm, and the thickness T_{BOX} of the SOI and the doping of the P-Substrate are 2 μm and 8×10^{14} cm^{-3}, respectively. Additionally, the thickness T_{ox} and the width W_{ox} of the TOL are 11 μm and 10 μm, and the doping N_N for the N-Pillar and the N_P for the P-Pillar are optimized. The electrical characteristics of the device are investigated with TCAD MEDICI [23]. In the simulation the physical and electrical models, including the mobility, ionization and the recombination models, are adopted.

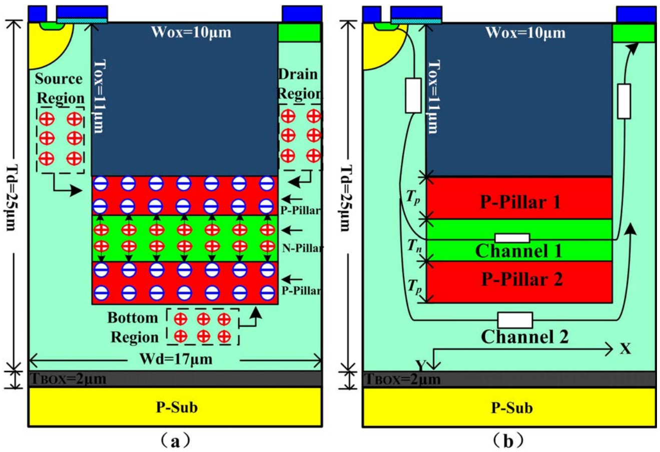

FIGURE 1. **Structure and mechanisms for the proposed TOL-LDMOS (a) space charges distribution at reverse blocking state (b) double electron channels at forward conduction state.**

The space charges distribution at reverse blocking state is illustrated in Fig. 1(a). The fixed charge is positive in the N-Pillar and Negative in the P-Pillar when the pillars are depleted, thus the vertical electric field is enhanced. Moreover, the Source region and Drain region are with fixed positive charge, and the electric field will stop at the P-Pillar 1. Meanwhile, the Bottom region is also with fixed positive charge, and the electric field will stop at the P-Pillar 2, thus the electric field in the whole N-drift region is enhanced and modulated. The double electron paths under conduction state are illustrated in Fig. 1(b), another conduction channel is introduced due to the N-Pillar of the lateral super junction. Futhermore, the doping N_N of the N-Pillar is much higher than that of the N-drift, so the resistance is much lower. Thus, the Specific On Resistance $R_{on,sp}$ is reduced.

III. ELECTRICAL CHARACTERISTICS

A. THE REVERSE BREAKDOWN VOLTAGE BV

Fig. 2 shows the equi-potential contours and the depletion layers of the LDMOSs at breakdown state, the source, gate and the P-Substrate are shorted to the ground. For the conventional LDMOS (CON-LDMOS), the equi-potential contours are sparse and distributed at the surface of the N-drift when the device breaks down at the voltage of 160 V, as shown in Fig. 2(a). For the conventional TOL-LDMOS with T_{ox}=22 μm, the device will breakdown at the drain voltage of 401.4 V, the equi-potential contours get much denser both at the surface and in the bulk of the N-drift as shown in Fig. 2(b). For the proposed LDMOS (NEW-LDMOS), the thickness T_p and T_n of the P-Pillars and N-Pillar are both 3 μm, the doping concentrations N_p and N_n of the P-Pillar and N-Pillar are 8×10^{14} cm^{-3} and 1.5×10^{15} cm^{-3}, respectively. Thus, $2\cdot T_p\cdot N_p \approx T_n\cdot N_n$ satisfies the charge balance according to the charge compensation theory of the super junction [4], [18], and the device will breakdown at the drain voltage of 422 V. The equi-potential contours are almost the same as the TOL-LDMOS, as shown in Fig. 2(c). From the point view of the depletion layers, the whole N-drift are completely depleted at the breakdown state, which indicates that the maximum BV will be achieved for all the devices.

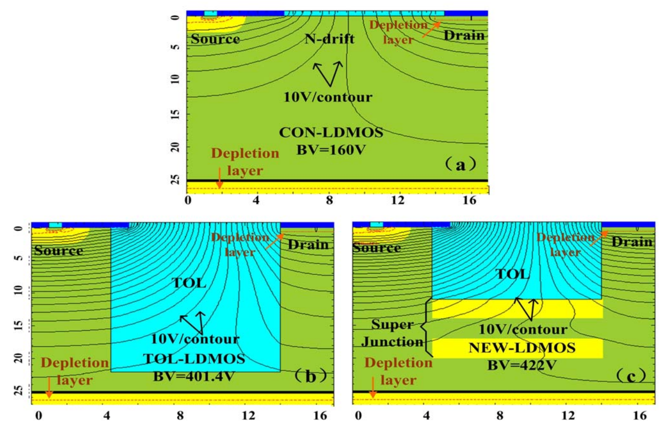

FIGURE 2. **Equi-potential contours and depletion layers (a) for the conventional LDMOS (b) for the TOL-LDMOS (c) for the NEW-LDMOS with lateral super junction, the thickness T_p and T_n are 3 μm, the doping N_p and the N_n of the P-Pillar and N-Pillar are set as 8×10^{14} cm^{-3} and 1.5×10^{15} cm^{-3} respectively.**

Fig. 3 provides the surface and bulk electric field distributions along the lateral direction for the devices. At the cutline y=0.5μm as shown in Fig. 3(a), the interface of the surface is formed by SiO_2/Si for the CON-LDMOS and SiO_2/ SiO_2 for the TOL-LDMOS. Compared with CON-LDMOS, the maximum surface electric field is improved from 2.5×10^5 V/cm to 6.2×10^5 V/cm at the source region, and another peak electric field is improved from 4.7×10^5 V/cm to 6.5×10^5 V/cm at the drain region. The surface electric field for the NEW-LDMOS is almost the same as the TOL-LDMOS at the source region and it is further improved to 7.5×10^5 V/cm at the drain region, thus it exhibits trapezoidal electric field distribution. At the cutline y=5 μm as shown in Fig. 3(b), the N-drift region is formed by Si/Si for the CON-LDMOS and Si/ SiO_2 for the TOL-LDMOS and the NEW-LDMOS, the bulk electric field is improved from 0.7×10^5 V/cm (CON-LDMOS) to 2.8×10^5 V/cm (TOL-LDMOS and the NEW-LDMOS) at the N-drift region. At the cutline y=11μm as shown in Fig. 3(c), the N-drift region is formed by SiO_2/P-Pillar for the NEW-LDMOS, and the electric field is fluctuated at the interface. At the cutline y=15μm as shown in Fig. 3(d), the

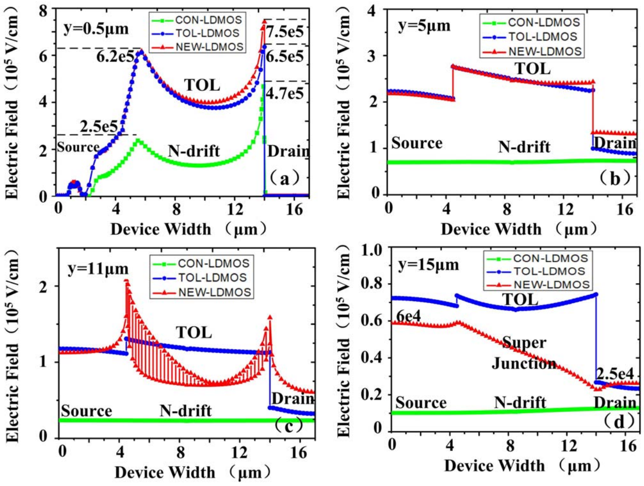

FIGURE 3. The surface and bulk electric field distributions along the lateral direction for the CON-LDMOS, TOL-LDMOS and the NEW- LDMOS at the cutline (a) y=0.5 μm, (b) y=5 μm, (c) y=11 μm, (d) y=15 μm.

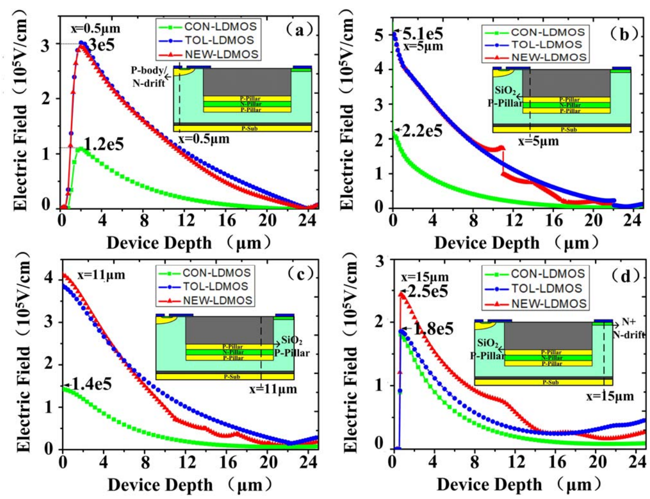

FIGURE 4. The electric field distributions along the vertical direction for the CON-LDMOS, TOL-LDMOS and the NEW- LDMOS at the cutline (a) x=0.5 μm, (b) x=5 μm, (c) x=11 μm, (d) x=15 μm.

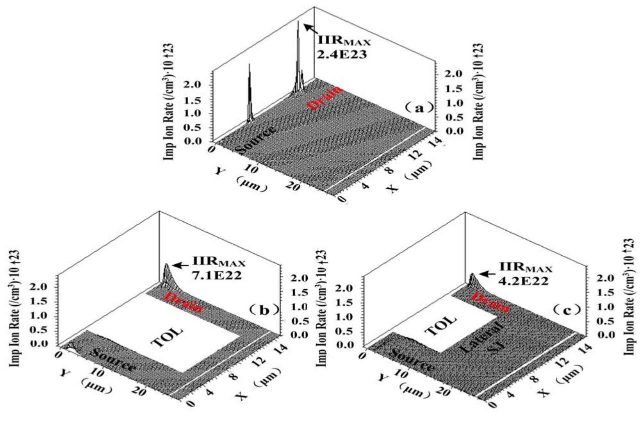

FIGURE 5. The Maximum impact ionization rate IIR_{MAX} at the breakdown state for (a) CON-LDMOS (b) TOL-LDMOS (c) NEW-LDMOS.

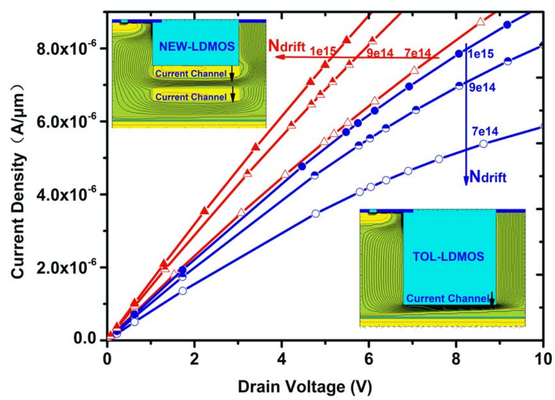

FIGURE 6. Forward conduction characteristics of the NEW-LDMOS with double current channels and the TOL-LDMOS with single current channel at the N_{drift} doping from 7e14 to 1e15 (the current distribution are given in the inset pictures).

N-drift is formed by Super Junction for the NEW-LDMOS, and the electric field is decreased from 6×10^4 V/cm at the source region to 2.5×10^4 V/cm at the drain region.

Fig. 4 shows the electric field distributions along the vertical direction of the devices. At the cutline x=0.5μm as shown in Fig. 4(a), the junction is formed by P-body/N-drift for all the devices, and the maximum electric field is improved from 1.2×10^5 V/cm for the conventional LDMOS to 3×10^5 V/cm for the TOL-LDMOS and the NEW-LDMOS at the P-body/N-drift junction. Moreover, the electric field is stopped at the N-drift region for the conventional, and it is extended vertically to the SOI for the TOL-LDMOS and NEW-LDMOS. At the cutline x=5μm as shown in Fig. 4(b), the junction is formed by SiO_2/Si at the surface for the CON-LDMOS, SiO_2/ SiO_2 at the surface for the TOL-LDMOS, SiO_2/ SiO_2 at the surface and SiO_2/ P-Pillar at the N-drift region for the NEW-LDMOS. The electric field is improved from 2.2×10^5 V/cm for the conventional to 5.1×10^5 V/cm for the TOL-LDMOS and the NEW-LDMOS at the surface. At the cutline x=11μm as shown in Fig. 4(c), the situation is almost the same as the Fig. 4 (b) with x=5μm. At the cutline x=15μm as shown in Fig. 4(d), the junction is formed by N+/N-drift for all the devices. The maximum electric field is 1.8×10^5 V/cm for the conventional LDMOS and the TOL-LDMOS, and it is improved to 2.5×10^5 V/cm for the NEW-LDMOS at the N+/N-drift junction, because the Super Junction helps to deplete the N-drift by charge compensation.

Fig. 5 shows the corresponding impact ionization rate under the breakdown state. It can be seen that the Maximum Impact ionization rate IIR_{MAX} are observed at the drain region for all the devices. For the conventional LDMOS as shown in Fig. 5(a), there is another peak value of impact ionization rate at the source region, so it is easier to breakdown. For the TOL-LDMOS and NEW-LDMOS as shown in Fig. 5(b) and Fig. 5(c), the IIR_{MAX} is much lower than the CON-LDMOS, so higher BV can be achieved.

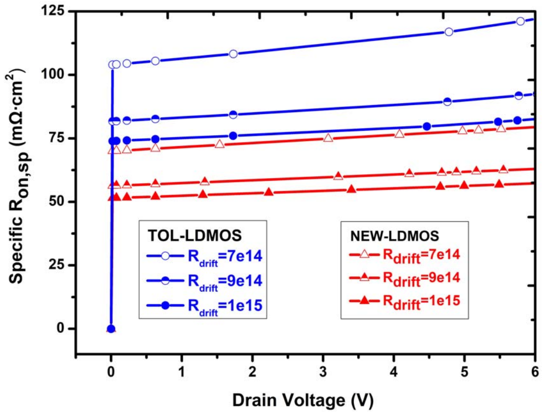

FIGURE 7. The specific On Resistance $R_{on,sp}$ of the NEW-LDMOS and the TOL-LDMOS at the N_{drift} doping from 7e14 to 1e15.

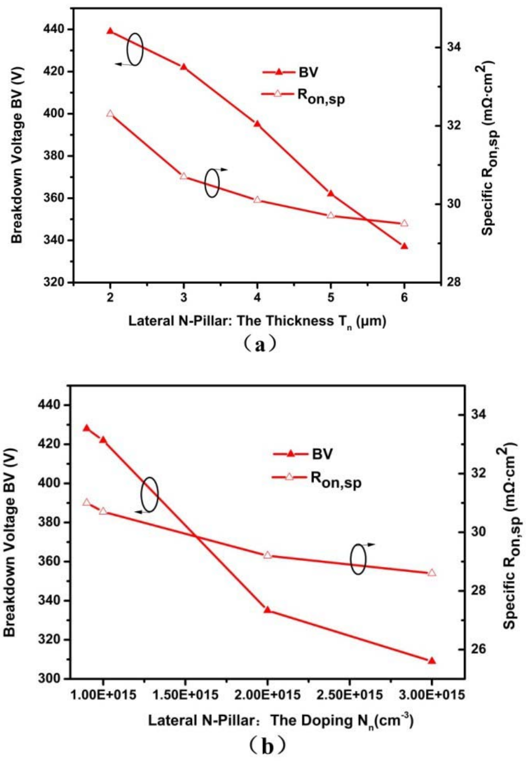

FIGURE 8. The BV and the $R_{on,sp}$ are functions of the Lateral Super Junction for the NEW-LDOMS (a) the thickness T_n of the N-Pillar (b) the doping N_n of the N-Pillar.

B. THE SPECIFIC ON RESISTANCE $R_{ON,SP}$

Fig. 6 shows the current voltage characteristics of the LDMOSs at forward conduction state. The source and the P-Substrate are shorted to the ground, the gate electrode V_g is 15V. The currents are increased linearly with the drain voltage for the both devices with the doping of the N_{drift} from 7e14 to 1e15. Moreover, at the same doping of the N_{drift}, the current density of the NEW-LDMOS with double electron channels is much higher than the TOL-LDMOS with single channel as shown in the inset pictures.

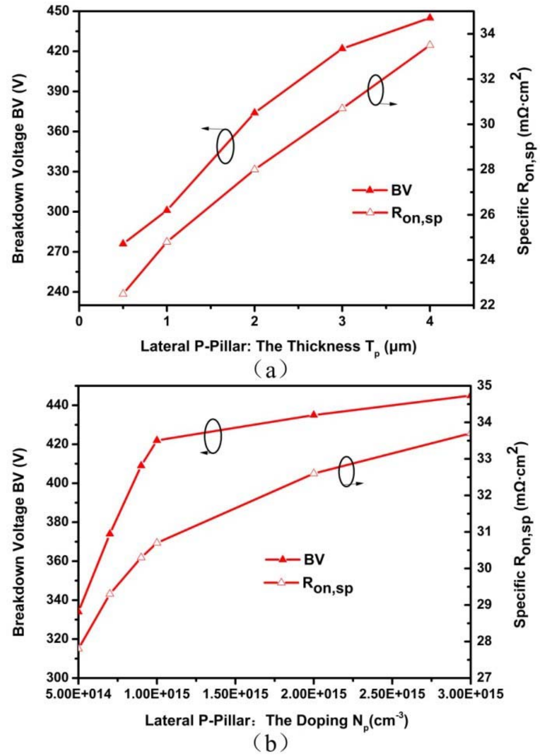

FIGURE 9. The BV and the $R_{on,sp}$ are functions of the Lateral Super Junction for the NEW-LDOMS (a) the thickness T_p of the P-Pillar (b) the doping N_p of the P-Pillar.

Fig. 7 shows the corresponding Specific On Resistance $R_{on,sp}$ of the LDMOSs at forward conduction state, it can be seen that the $R_{on,sp}$ of the NEW-LDMOS is much lower than the TOL-LDMOS at the same doping of the N_{drift} due to the double electron current channels.

C. THE LATERAL SUPER JUNCTION INFLUENCE ON THE BV AND $R_{ON,SP}$

The BV and the $R_{on,sp}$ are functions of the N-Pillar of the Lateral Super Junction as shown in the Fig. 8. The $R_{on,sp}$ decreases with the increase of the thickness T_n and the doping N_n of the N-Pillar because the conduction capability of the current channel is improved as illustrated in the inset picture of Fig. 6. Meanwhile, the BV is decreased due to the charge imbalance between the N-Pillar and the P-Pillar.

The BV and the $R_{on,sp}$ are functions of the P-Pillar of the Lateral Super Junction as shown in the Fig. 9. The $R_{on,sp}$ increases with the increase of the thickness T_p and doping N_p of the P-Pillar because the conduction capability is reduced, at the same time the BV is enhanced due to the charge balance between the N-Pillar and the P-Pillar.

D. THE THICKNESS OF TOL INFLUENCE ON THE BV AND $R_{ON,SP}$

The BV and the $R_{on,sp}$ are functions of the thickness T_{ox} of the Trench Oxide Layer as shown in the Fig. 10. The

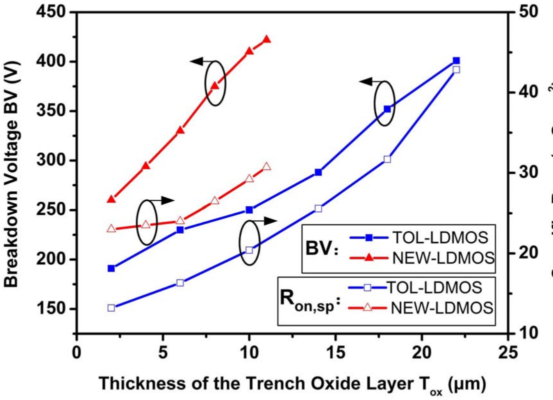

FIGURE 10. The BV and the $R_{on,sp}$ are functions of the thickness T_{ox} of the TOL for the LDMOSs (the T_{ox} is reduced from 22μm to 2μm for the TOL-LDMOS, the T_{ox} is reduced from 11μm to 2μm for the NEW-LDMOS).

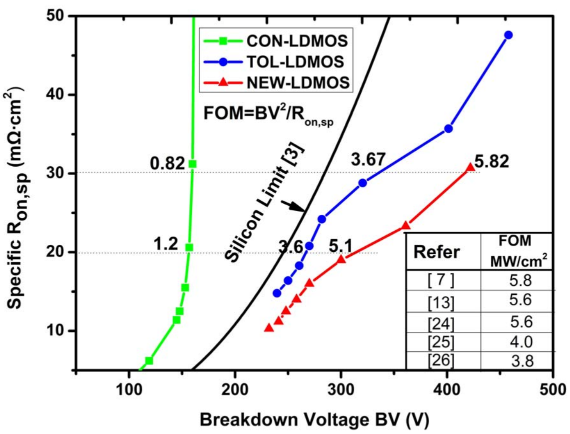

FIGURE 11. Specific $R_{on,sp}$ versus BV relationship for the LDMOS device with the experimental and simulated data reported previously.

T_{ox} is initially designed with 22 μm for the TOL-LDMOS and 11 μm for the NEW-LDMOS, when the T_{ox} is reduced to 2 μm, the $R_{on,sp}$ is improved for both LDMOSs due to the reduction of the resistance at the Source region and Drain region as shown in Fig. 1(b). At the same time, the BV is also reduced for both LDMOSs, but the BV of the NEW-LDMOS is much higher than the TOL-LDMOS with the same T_{ox} due to the lateral super junction as shown in Fig. 1 (a).

E. THE BALIGA'S FIGURE OF MERIT FOM

Fig. 11 shows the ideal silicon limit of the RESURF LDMOS given in [3], and the $R_{on,sp}$ versus the BV relationship of the devices with the experimental and simulated data reported previously [7], [13], [24]–[26]. It is apparent that the performance of the NEW-LDMOS breaks through the silicon limit. Moreover, the FOM (Baliga's Figure Of Merit) is defined as $BV^2/R_{on,sp}$ to describe the tradeoff performance of the devices. It shows that the FOM is obtained 5.82 MW/cm^{-2} with the BV of 422 V and $R_{on,sp}$ of 30.7 $m\Omega\cdot cm^2$ for the NEW-LDMOS, compared the conventional LDMOS with 0.82 MW/cm^2 and the TOL-LDMOS with 3.67 MW/cm^2, the FOM is improved almost 702% and 158% respectively.

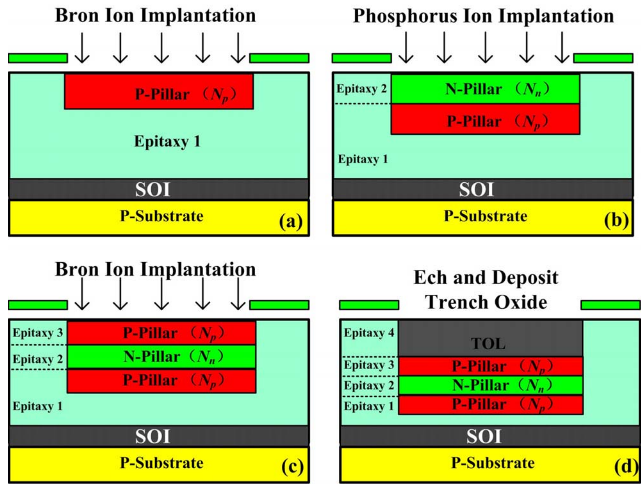

FIGURE 12. The key process of the NEW-LDMOS to prepare the lateral super junction and TOL (a) the bottom P-Pillar (b) the N-Pillar (c) the upper P-Pillar (d) the Trench Oxide Layer.

F. THE KEY PROCESS OF THE NEW-LDMOS

The key process of the NEW-LDMOS is compatible with the conventional TOL-DMOS as given in Fig. 12. However, extra three steps of epitaxies and ion implantation are needed to fabricate the P-Pillar and N-Pillar of the lateral super junction as illustrated in Fig. 12 (a-c). The process of Trench Oxide is given in Fig. 12 (d) for both NEW-LDMOS and TOL-LDMOS.

IV. CONCLUSION

A novel TOL-LDMOS with a Lateral Super Junction under the Trench Oxide is proposed, the multiple epitaxies and ion implantation are needed to prepare the P-Pillar and N-Pillar. The results show that the Lateral Super Junction combined with the TOL can improve the surface and bulk electric field in the N-drift, which significantly improves the BV. On the other hand, the N-Pillar of the Lateral Super Junction provides another electron current channel at the forward conduction state, which significantly decreases the Specific $R_{on,sp}$. Finally the tradeoff performance of the NEW-LDMOS breaks through the ideal silicon limit with superior FOM.

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