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# Cryogenic Temperature Characterization of a 28-nm FD-SOI Dedicated Structure for Advanced CMOS and Quantum Technologies Co-Integration

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**ABSTRACT** Silicon co-integration offers compelling scale-up opportunities for quantum computing. In this framework, cryogenic temperature is required for the coherence of solid-state quantum devices. This paper reports the characterization of an nMOS quantum-dot dedicated structure below 100 mK. The device under test is built in thin silicon film fabricated with 28 nm high-*k* metal gate ultra-thin body and ultra-thin buried oxide advanced CMOS technology. The MOS structure is functional with improved performances at cryogenic temperature. The results open new research avenues in CMOS co-integration for quantum computing applications within the FD-SOI platform.

**INDEX TERMS** FD-SOI, quantum computing, co-integration, cryogenic temperature.

## I. INTRODUCTION

Breakthoughs of the last 15 years, together with their potential for scalability, have made solid-state quantum bits (qubits) amongst the most promising contenders for the realization of a quantum computer [1]–[7]. Scaling solid-state qubits to a full fledge quantum computer requires the co-integration of qubits with their control blocks [8]. While particularly adapted to this approach, most solid-state qubits operate at cryogenic temperature to obtain sufficient quantum coherence, a stringent requirement for the co-integration of control electronics. Silicon qubits are particularly attractive for co-integration, due to their high coherence and direct compatibility with CMOS technology [6]–[16]. To address the development of co-integrated silicon qubits and control devices it is important to characterize MOS behavior for classical operation at cryogenic temperature. While MOS devices were proven successful for silicon qubit operations at temperatures of a few milli-kelvin [6], [7], [16], the development of next-generation cryogenic transistors is under evaluation [17]. Fully depleted silicon-on-insulator (FD-SOI) based architectures are promising candidates to fulfill the requirements of low-temperature co-integrated quantum processors (Fig. 1). This technology provides low power consumption capabilities [18], [19], demonstrated cryogenic temperature operation [17], [20]–[22] and reduced leakage current [18] that is detrimental to quantum devices. Moreover, back body biasing offers additional control for electrostatically defined quantum confinement. Here a first transistor characterization of STMicrolectronics 28nm FD-SOI technology is reported with a dedicated qubit structure operating at cryogenic temperature below 100 mK.

## II. SAMPLE STRUCTURE AND METHODS

The device is designed on ultra-thin body and ultra-thin buried oxide (UTBB) 28 nm high-k metal gate FD-SOI technology. The standard fabrication process comprehends an ultra-thin silicon channel of 7 nm and ultra-thin buried oxide (BOX) of 25 nm together with high-k metal gate stack and P/N-type backplane. The equivalent oxide thicknesses (EOT) are EOT=1.1 nm for standard gate voltage (1 V) and EOT=3.4 nm for extended front gate at high

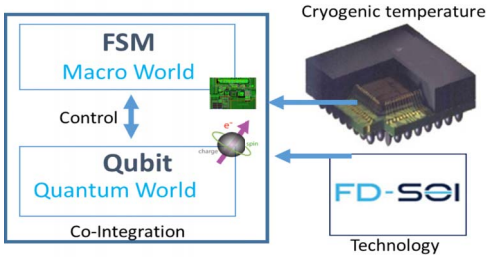


**FIGURE 1.** Co-integration based on 28 nm FD-SOI technology.

voltage drive (1.8 V). The back end of line is processed with eight copper layer interconnections and bonding pad connections made of aluminum/copper alloy.

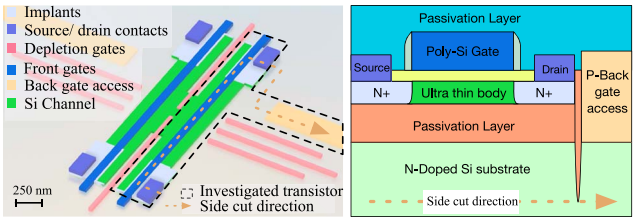


**FIGURE 2.** (left) Dedicated layout, terminals and device topography. (right) Not to scale side-cut schematic of the investigated transistor.

The dedicated structure consists of two distinct channels with isolated terminals (Fig. 2). The device is designed to host two independent quantum dots in the gated wire geometry [23], [24] that could serve as qubits. The two channels comprehend an accumulation gate overlapping an intrinsic active Si channel with N-type drain and source implants that are connected to metal terminals to drive the drain current $I_{ds}$. Both active can be considered as N-MOS structure with a 980 nm long and 200 nm wide channel with a narrow front gate of 54 nm. Three additional control gates are located close to the active to allow electrostatic control of the quantum dots in future work. In this study, the N-MOS electrical characteristics with front and back gate controls have been investigated on half of the structure. Front and back gate bias, $V_{fg}$ and $V_{bg}$, are used to change the carrier density and characterize the low temperature properties of the N-MOS transistor. The unpackaged samples are mounted at the die level and wire bonded to a chip carrier thermally anchored to the mixing chamber of a BlueFors 250 μW dilution refrigerator operating at a base temperature of 20 mK. The electronic temperature could not be directly measured for these samples. Previous measurements on quantum devices gave an electronic temperature of 50 mK for the same setup.

## III. FRONT GATE CHARACTERIZATION

The most important result of our study is that the N-MOS transistor is functional at 20 mK and shows improved performances compared to room temperature regarding: effective carrier mobility, power consumption and sub-threshold slopes.

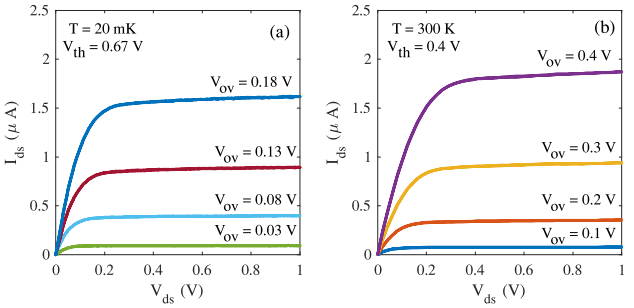


**FIGURE 3.** (a) $I_{ds}(V_{ds})$ for $V_{fg}$ varying from 0.65 V to 0.85 V by steps of 0.05 V and for $V_{bg} = 0$ V at 20 mK. (b) $I_{ds}(V_{ds})$ for $V_{fg}$ varying from 0.5 V to 0.8 V by increments of 0.1 V and for $V_{bg} = 0$ V at 300 K. The overdrive voltage ($V_{OV}$) is indicated for each curve.

The electric performance of the drain current $I_d$ ($V_{ds}$) response for different front gate bias is reported for unbiased back-gate $V_{bg} = 0$ V (Fig. 3). At cryogenic temperature, an increase in threshold voltage of 0.27 V highlights the reduced carrier density in the channel. Above threshold, with fixed overdrive voltage ($V_{OV}$), larger saturation current is observed. This effect is well understood with an increase of the effective carrier mobility ($\mu_{eff}$) at low temperature. In linear regime, the maximal effective mobility can be derived from the maximal transconductance extracted with $I_{ds}(V_g)$ curves and the Y-function method [25]. In FD-SOI, the maximal effective mobility then be extracted for front and back[1] interfaces following:

$$\mu_{\text{eff}}^{\max} = I_{\text{ds}} \left[ \frac{W}{L} \frac{C_{\text{ox}}}{(1+\alpha)} \left( V_{\text{g}}^{\max} - V_{\text{th}} \right) V_{\text{ds}} \right]^{-1}$$
$$\alpha = \frac{C_{\text{si}} C_{\text{ox}}}{C_{\text{ox}} (C_{\text{si}} + C_{\text{box}})} \quad (1)$$

where $W$ and $L$ are the width and length of the channel and $V_{\text{g}}^{\max}$ the gate voltage at maximal transconductance. The capacitance ratio $\alpha$ is calculated from the front and back interfaces oxide capacitance $C_{\text{ox}}$ and $C_{\text{Box}}$ and the silicon channel capacitance $C_{\text{si}}$. The capacitances are estimated from device material and geometry.

The extracted maximal effective mobilities are respectively $\mu_{\text{eff-FG}}^{\max} \sim 590$ cm$^2$/Vs and $\mu_{\text{eff-BG}}^{\max} \sim 890$ cm$^2$/Vs at 20 mK (Fig. 4). At high temperature, the back interface follows a power law dependence of $\mu_{\text{eff-BG}}^{\max} \sim T^{-3/2}$ in good agreement with bulk phonon scattering. In front gate operation, the high-$\kappa$ metal gate stack gives rise to an additional scattering mechanism due to soft-optical phonons [26], [27] which has been argued to account for the lower mobility compared to the back interface [28]. Although $\mu_{\text{eff-FG}}^{\max}$ remains lower than $\mu_{\text{eff-BG}}^{\max}$ throughout the whole temperature range, both mobilities reach a plateau between 1-10 K and decrease again at very low temperature. The decrease can indicate

1. In back-gate operation Cox and CBox are reversed in equation (1). In this regime most of the accumulated channel is not overlap by the top gate and $\alpha \sim 0$.

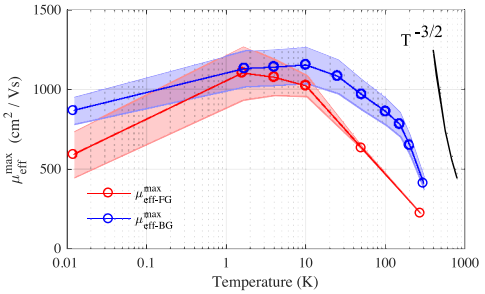


**FIGURE 4.** **Temperature dependence of the maximal effective mobility for front (blue) and back (red) gate operation. The mobilities are extracted from equation (2) and the Y-function method at $V_{ds}$ = 10 mV. Shaded areas represent error bars on the extracted mobilities.**

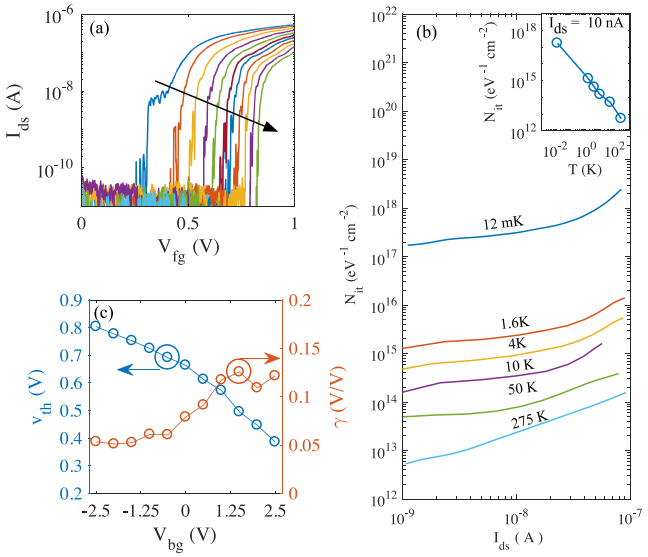


**FIGURE 5.** **(a) $I_{ds}$ as a function of $V_{fg}$ for $V_{bg}$ ranging from 2.5 V to −2.5 V by steps of 0.5 V at 20 mK & $V_{ds}$ = 10 mV. The arrow indicates decreasing back-gate bias. (b) Temperature dependence of the extracted charge trap density ($N_{it}$) in the weak inversion regime. The inset shows $N_{it}$ as a function of temperature extracted at $I_{ds}$ = 10 nA. (c) Threshold voltage ($V_{th}$) and back-body coefficient ($\gamma$) as a function of $V_{bg}$.**

coulomb scattering with substrate impurities in both channels which is expected to reduce the mobility with lowering temperature [26], [27], [29].

The lower $V_{ds}$ required to reach the saturation regime at low temperature leads to slightly lower power dissipation for the same dynamic range in $V_{ds}$. In static operation with $V_{OV}$ = 0.08 V and $V_{ds}$ = 0.2 V the power dissipation is ∼100 nW. In that regime, the co-integration of up to 10,000 transistors at 100 mK can be envisioned without impairing the operation temperature of the qubits. At milli-Kelvin temperature the transport behavior is very sensitive to disorder in the channel as seen from current peaks and valleys in subthreshold regime (Fig. 5a). Local traps cause position-dependent variations of the electronic density of states. Due to the small dimensions of the channel and front gate, it results in the formation of tunnel barriers and leads to quench or revival of the subthreshold current as the traps are being filled or emptied. The switching performances of the transistor should also be improved at low temperature as depicted by the reduction of the sub-threshold swing from S = 87 mV/decade at 300 K to S = 7 mV/decade at 20 mK. The subthreshold swing can be further enhanced by decreasing the back gate biasing (Fig. 5a). At $V_{bg} = -2.5$ V, a value of S = 2 mV/decade is measured. This is consistent with the displacement of the mean channel position toward the front interface which increases the front gate coupling capacitance ($C_{ox}$) [30]. However, even in these conditions, the subthreshold swing remains orders of magnitude larger than the expected value of S ∼ 0.006 mV/decade when considering the typical linear reduction of S with temperature for MOSFET devices [31]. A simplified model for subthreshold swing can be derived by reducing a standard equation for FD-SOI [32] to a single sheet conductivity model and equal trap state density at front and back interfaces:

$$S = \ln 10 \frac{kT}{q} \left( \frac{(C_{si} + C_{ox} + C_{it})}{C_{ox}} - \frac{C_{si}^2}{C_{ox}\,(C_{si} + C_{box} + C_{it})} \right) \quad (2)$$

where $C_{Si}$ is the inversion charge capacitance and $C_{it}$ the interface trap state capacitance.

In the context of bulk MOSFET transistors the deviation from theory was explained by an increase in the interface trap state density ($N_{it}$) at low temperature [33], [34]. The disordered potential at the Si-$SiO_2$ interface gives rise to a tail of localized states lying below the mobility edge ($E_c$) of the conduction band in the channel [35]. As the temperature is lowered, the Fermi level is shifted toward the mobility edge and stabilizes slightly below for typical doping levels [36], [37]. Together with the reduced energy window spanned by the Fermi function, this leads to a higher occupied trap state density which can be a significant fraction of the total charge density. As a result, the interface charge trap capacity, $C_{it} = qN_{it}$, and the subthreshold swing are also increased. For FD-SOI transistors at high temperature significant front and back interface charge state densities have been measured [32], [38], and a similar behavior of the subthreshold swing is expected at low temperature.

From equation (2) and $I_{ds}(V_{fg})$ in the weak inversion regime the interface trap state density can be extracted for various temperatures (Fig. 5b). Since the span of the Fermi function is significantly reduced at low temperature, the subthreshold regime corresponds to an energy scale very close to the mobility edge. Hence, measuring $N_{it}$ at different temperatures gives insight about the energy dependence of the trap state density. In the present case, $N_{it}$ is found to increase exponentially. This tendency pictures the exponentially increasing density of interface states as the energy approaches the mobility edge and was also observed in previous work [32]. Although the extraction of $N_{it}$ with

equation (2) has been successful down to 4 K [33], it's validity at milli-Kelvin temperature can be doubtful due to the usage of Maxwell-Boltzmann statistics. Therefore, the value of $N_{it} \sim 10^{17}$ eV$^{-1}$cm$^{-2}$ extracted at 12 mK should be taken as an indicator, while a deeper study of the interface trap state density will be part of a future work.

Back body biasing modifies the front gate operation of the transistor. At low temperature, the front-gate threshold voltage varies as a function of the back-gate bias with a back-body coefficient of $\gamma \sim$ 50-125 mV/V (Fig. 4c) comparable to room temperature operation [39]. The back-body coefficient is roughly constant with $\gamma \sim 50$ mV/V at negative $V_{bg}$ and increases above $V_{bg} = -1.25$ V. This is again reminiscent of the mean channel position displacement with varying back gate voltage. As the back-gate bias becomes more positive, the mean channel position is dragged toward the back interface, thus increasing the BOX capacitance. Back body biasing also presents two major effects on $I_{ds}(V_{ds})$ characteristics in front gate operation (Fig. 6). At negative bias, a hysteretic behavior is observed on most of the curves (Fig. 6a). The hysteresis presumably arises from the high resistance of the back plane at low temperature due to low donor concentration. At negative bias the back-plane resistance is further increased and give rise to very long settling time of the back-gate voltage.

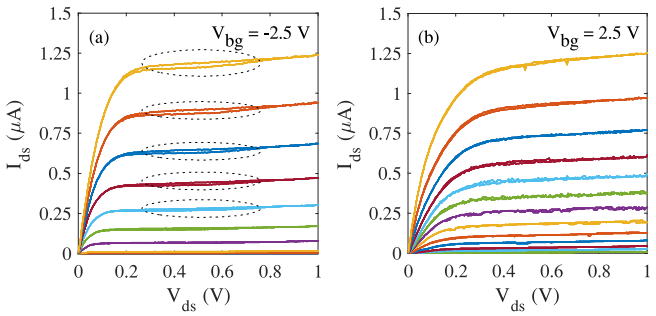


**FIGURE 6. (a) $I_{ds}$ ($V_{ds}$) for $V_{fg}$ from 0.7 V to 1 V by step of 25 mV with back-gate bias $V_{bg} = -2.5$ V Dotted circles indicate the hysteresis region. (b) $I_{ds}$ ($V_{ds}$) for $V_{fg}$ from 0.2 V to 0.5 V by step of 25 mV with back-gate bias $V_{bg} = 2.5$ V.**

In saturation regime at positive back-gate bias of $V_{bg} = 2.5$ V, pronounced random telegraphic noise is observed (Fig. 6b). For these parameters, the mean channel position is near the back interface, especially in the regions of the device without overlapping front gate (Fig. 2). Furthermore, the telegraphic noise is suppressed as front gate bias increases, thus pulling the mean channel position toward the front interface. This indicate the presence of active back interface charge traps and will be further discussed in Section IV. Typical transport measurements of quantum dots are performed with source-drain current in the pA range and below. Therefore, it is important to maintain gate leakage currents well below the quantum dot source-drain current to conserve a good signal to noise ratio. Moreover, leakage currents can induce electrical noise which has been found to perturb the electrostatic environment of quantum dots [40]. For the thin front-gate oxide, a maximum leakage current of 120 pA is measured at 1 V gate bias. This leakage current is four orders of magnitude lower than the source-drain current and therefore acceptable for transistor applications in co-integration but needs to be improved for quantum dot control. This large leakage is not observed with the back gate and will be explored on devices with thicker front-gate oxide.

## IV. BACK GATE CHARACTERIZATION

Deeper characterization of the telegraphic noise and hysteresis behavior with back gate biasing is now being addressed. The investigation is performed with bidirectional source-drain bias sweep and ramp up and down excursions of the back gate (Fig. 7). All $I_{ds}$ ($V_{ds}$) curves in back-gate operation exhibit random telegraphic noise in the saturation regime. In concordance with Fig. 6, this indicates the presence of active traps at the back interface.

Absent at room temperature, a strong hysteresis appears on all $I_{ds}(V_{ds})$ curves due to the high resistivity of the back plane. The different amplitude and current level of the hysteresis for same back-gate voltages highlight the slow time constant involved in back gate biasing. In Fig.7b, the slow time constant is exemplified by smaller hysteresis amplitude in $I_{ds}$ ($V_{ds}$) curve at 3.5 V compared to Fig. 6a due to five minutes waiting time between the two curves. The hysteretic behavior also persists in $I_{ds}$ ($V_{bg}$) characteristics for dynamic back gate biasing (Fig. 7a). It gives rise to an apparent voltage shift of $\sim$ 400 mV between sweep up and down traces. This shift can be reduced by decreasing the sweep rate (inset of Fig. 8a). Altogether with time-dependent measurements a settling time on the order of tens of minutes is estimated for the back-gate bias.

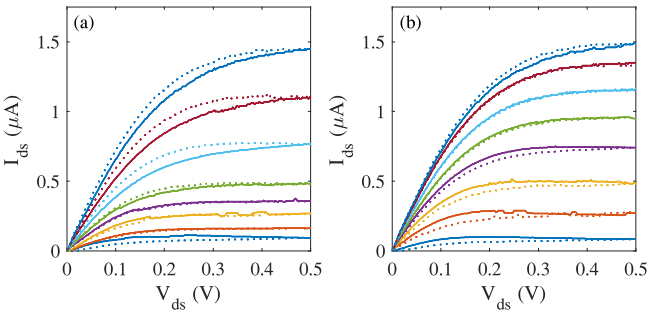


**FIGURE 7. $I_{ds}$ ($V_{ds}$) for $V_{fg=}$0 V and $V_{bg}$ ramping up (a) and down (b) between 2.8 V and 3.5 V by steps of 0.1 V at 20 mK and $V_{fg} = 0$ V. Forward $V_{ds}$ sweeps are represented in solid lines (0 to 0.5 V) and backward $V_{ds}$ sweeps in dotted lines. Five minutes separate the end of the acquisition of the ramp-up series and the beginning of the ramp down.**

Back-gate operation also present different plateaus in $I_{ds}$ ($V_{bg}$) traces (Fig. 8a). The non-monotonous behavior

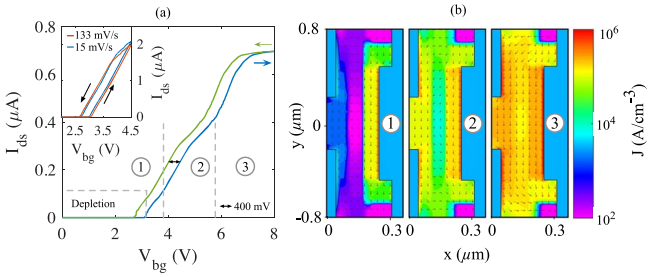


**FIGURE 8.** **(a) $I_{ds}(V_{bg})$ for $V_{ds}$ = 10 mV at 20 mK for rising (blue) and decreasing (green) $V_{bg}$. Dashed lines separate the three accumulation regimes for rising $V_{bg}$. Inset: $I_{ds}(V_{bg})$ for $V_{ds}$ = 100 mV for different sweep rates. (b) Simulated current density using Atlas 2D-Poisson solver at 300 K in the three different regimes.**

comes from the fact that the front gate does not fully overlap the channel accumulated by the back gate (Fig. 2). It results in different threshold voltages for the different regions of the channel due to additional screening underneath the front gate. The plateaus are trackable up to room temperature and their origin can thus be understood with the current density extracted from Atlas simulations at 300 K (Fig. 8b). Although the simulations are not quantitatively representing the current density at cryogenic temperature, the qualitative behavior of the three different regimes can be described as follows. 1) The front gate screening prevents the current from flowing on the left side of the device. 2) Increasing back-gate bias allows the current to overcome the barrier at the center of the device, but there is still low current underneath the front gate. At higher $V_{bg}$ the current start to saturate for non-overlapping regions. 3) Current amplitude underneath the front gate increases and saturation is met in all the regions of the device at $V_{bg} > 7$ V.

## V. CONCLUSION

A cryogenic temperature characterization of a N-MOS quantum dot structure built on 28 nm UTBB FD-SOI advanced CMOS technology is presented. The front gate MOS behavior is functional at 20 mK with improved maximal carrier mobility ($\mu_{\text{eff-FG}}^{\max} \sim 590$ cm$^2$/Vs), power dissipation and sub-threshold slope (S $\sim$ 2-7 mV/decade) compared to room temperature operation. The subthreshold slope is found to be limited by interface trap state density. In back gate biasing and back-gate operation, a large hysteresis is apparent due to low implantation in the back plane and leads to settling time of tens of minutes. Furthermore, biasing the back gate to positive voltages gives rise to telegraphic noise in the current characteristics. This is due to a displacement of the mean channel position toward the back interface and could be linked to the activation/relaxation processes on back interface trap states. A better understanding of this behavior requires further investigation, such as cryogenic C-V characterization, to pinpoint the process involved in this unstable behavior. Our results represent a first step toward co-integration of a qubit with its control block within the 28 nm FD-SOI technology.

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