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Scalability and Stability Enhancement in Self-Aligned Top-Gate Indium- Zinc-Oxide TFTs With Al Reacted Source/Drain

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ABSTRACT A self-aligned fabrication process for top-gate amorphous indium–zinc–oxide (a-IZO) thin-film transistors (TFTs) is demonstrated. Aluminum (Al) thermal treatment is employed to dope the a-IZO layer and thus form the self-aligned source/drain regions. The results show that the sheet resistance of the Al-treated a-IZO layer can be as low as 360 Ω/□. The fabricated top-gate TFTs typically have a mobility of 16.84 $cm^2/V \cdot s$, subthreshold swing of 0.14 V/dec and on/off current ratio of $> 10^9$. The Al-treated TFTs show a significant scalability and stability enhancement compared to the conventional Ar plasma-treated ones. This enhancement can be attributed to the thin Al_2O_3 layer formed on source-drain area that blocks the diffusion of hydrogen or H_2O from the passivation layer into the source-drain and channel regions.

INDEX TERMS Amorphous indium-zinc-oxide (a-IZO), self-aligned, top-gate, aluminum reaction.

I. INTRODUCTION

Amorphous oxide semiconductor (AOS) thin-film transistors (TFTs) represented by amorphous indium-gallium-zinc-oxide (a-IGZO) TFTs have attracted considerable attention in recent years for their potential applications in large area electronics because of their intriguing properties, such as high mobility, excellent large area uniformity, and low processing temperature [1]–[4].

The AOS TFTs have usually been fabricated in the bottom-gate structure, such as the back-channel-etch (BCE) or etch-stop-layer (ESL) structure [5], [6]. For bottom-gate structures, some issues are difficult to address, such as the large parasitic capacitance between the gate and source/drain electrodes and the weak channel length scalability [7].

In contrast, the top gate (TG) structure is free of the large parasitic capacitance if a self-aligned fabrication process is established. For the TG AOS TFTs, one major technical issue is the formation of the self-aligned source/drain (S/D) regions, which must be highly conductive and stable. To date, a number of methods of forming the self-aligned n+ S/D regions have been proposed, such as H doping [8], [9], ion implantation [10]–[13] and H_2, Ar, or NH_3 plasma treatments [14]–[17]. While these methods are usually able to help reduce the S/D resistance effectively, they are not well controlled [18]. Recently, Sony demonstrated a low resistive metallic S/D region formation technique with a-IGZO and a-ITZO TFTs using the Al reaction method [18], [19]. It was shown that the sheet resistance of the S/D regions with this method is low and remains stable, even after subsequent thermal processes. Therefore, the use of metal reaction is a promising method to form the self-aligned S/D regions of top-gage AOS TFTs.

In addition, amorphous indium-zinc-oxide (a-IZO) is potentially a high mobility AOS material, and a self-aligned top-gate (SATG) a-IZO TFT process has been demonstrated [4], in which the low resistance S/D region is formed by the conventional Ar plasma treatment. However, the availability of the metal reaction method with a-IZO TTFs has not been confirmed yet.

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In this work, the Al reaction method with a-IZO TFTs is experimentally studied. A low and stable sheet resistance in source/drain regions is obtained with this method. A new SATG a-IZO TFT process is thus developed. In particular, the metal reaction method allows a-IZO TFTs to achieve a significant improvement in scalability and stability.

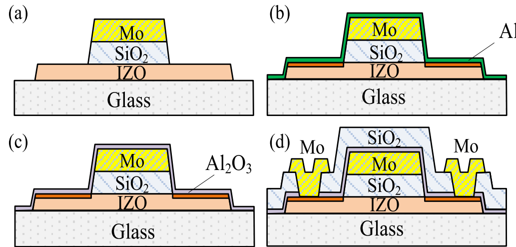

FIGURE 1. Fabrication process of the self-aligned top-gate a-IZO TFTs.

II. EXPERIMENT

Fig. 1 shows a cross-sectional view of the fabrication processes for our SATG a-IZO TFTs. The substrates used are two-inch glass wafers. First, a 40-nm-thick a-IZO film was deposited on the substrate by direct current (DC) sputtering using an IZO target (In: Zn = 1: 1 in mol %) at Ar/O_2 gas flow ratio of 40 sccm: 10 sccm. The IZO film is then patterned by wet etching to form the active islands. Following, a 200-nm-thick SiO_2 layer was deposited by plasma enhanced chemical vapor deposition (PECVD) as the gate insulator. Afterwards, a 150-nm-thick layer of molybdenum (Mo) was deposited by DC sputtering as the gate metal. The Mo gate and SiO_2 gate insulator layers were patterned by dry etching using one single photolithographic mask, as shown in Fig. 1(a). Next, a 3-nm-thick Al layer was deposited by sputtering on the exposed IZO layer in the S/D area, as shown in Fig. 1(b). Immediately after the deposition, thermal annealing was performed in an oxygen-contained atmosphere for 1.5 hour at 300 °C, as shown in Fig. 1(c). Afterwards, a 200-nm-thick layer of SiO_2 was deposited at 150 °C by PECVD to form an interlayer dielectric and then patterned to open contact holes for S/D metal electrodes by dry etching. Finally, a 100-nm-thick Mo was deposited by DC sputtering and patterned to form S/D electrodes, as shown in Fig. 1(d).

For comparison, a-IZO TFTs with S/D regions treated by Ar plasma instead of the Al reaction were also fabricated. The Ar plasma treatment was performed immediately after the dry etch of the gate metal and dielectric, as shown in Fig. 1(a), the treat time is 60 s in this fabrication.

The electrical characteristics of the TFTs were measured with an Agilent B1500 semiconductor parameter analyzer at room temperature in the dark.

III. RESULTS AND DISCUSSION

Fig. 2 shows the sheet resistances of the Al reaction- and Ar plasma-treated a-IZO films versus the post thermal treatment temperatures. The sheet resistances were obtained using

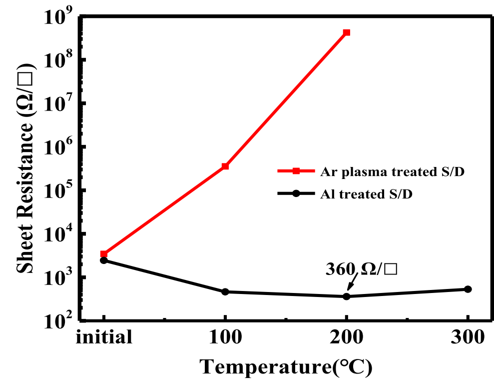

FIGURE 2. Dependence of the sheet resistance of the source/drain regions on the post thermal treatment temperature.

Hall Effect Measurement. Before the Al deposition or Ar plasma treatment, the sheet resistance of the a-IZO film is over $10^9 \Omega/\square$. As shown, both the Al and Ar plasma treatment enables the a-IZO films to have a low sheet resistance. However, the Al-treated film exhibits a noticeable reduction in the sheet resistance after the post-annealing from room temperature to 300 °C, whereas the Ar plasma-treated one exhibits a sharp increase with raising annealing temperature. This observation is similar to the earlier observation in a-IGZO films [18]. The minimal sheet resistance in this work of the Al-treated film at 200 °C is 360 Ω/□ , which is lower than that of the a-IGZO films of 995 Ω/□ [19]. Thus, the availability of the Al treatment for doping the a-IZO is well verified by the observation of a low sheet resistance.

It is worth pointing out that the initial sheet resistance of the source/drain region with the 3 nm Al coated is reduced to about 2.5 KΩ/□ from over $10^9 \Omega/\square$ before the thermal treatment. The low initial resistance is unlikely caused by the 3 nm Al film itself since the sheet resistance of the 3 nm Al film itself is too high to be measured in our experiments. It is believed the low initial resistance is caused by the Al atoms bombing on the IZO and generates oxygen vacancies at the IZO surface during the sputtering process. The generated oxygen vacancies lead to the initial low resistance.

Fig. 3 shows the transfer characteristics ($I_{DS} - V_{GS}$) of both the Al and Ar plasma-treated SATG a-IZO TFTs with the gate length $L = 10$ μm and channel width $W = 20$ μm. The inset plot shows the off- currents of TFTs at $V_{DS} = 10$ V. Table 1 lists the major performance parameters of the fabricated SATG TFTs. As shown, the Al-treated TFT shows better electrical performance than the Ar plasma-treated TFT. The saturation mobility (μ_{sat}), subthreshold swing (SS) and on/off current ratio (I_{on}/I_{off}) of the Al-treated device are 16.84 $cm^2/V \cdot s$, 0.14 V/dec and $> 10^9$, respectively, which are overall superior to those of the Ar plasma-treated device.

Fig. 4 shows the total device resistances R_{TOT} (V_{DS}/I_{DS}) of the a-IZO TFTs versus the gate length L at various V_{GS}, with (a) for the Al reacted and (b) the Ar plasma-treated. The channel width normalized $R_{SD}(R_{SD} \cdot W)$ and the shrinkage of

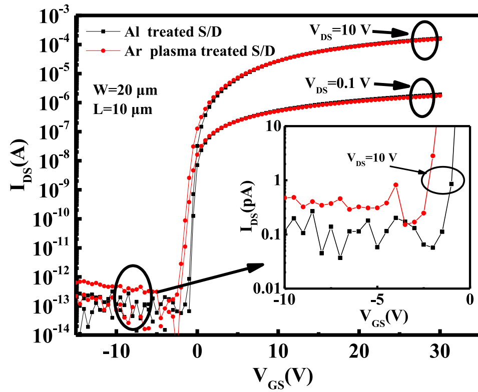

FIGURE 3. Transfer characteristics of the Al reaction and Ar plasma-treated SATG a-IZO TFTs with gate length $L = 10\ \mu$m and channel width $W = 20\ \mu$m. Inset plot shows the off- currents of TFTs at $V_{DS} = 10$ V.

TABLE 1. Electrical parameters of the self-aligned top-gate a-IZO TFTs with different S/D treatment methods.

S/D treatment	V_{TH} (V)	μ_{sat} ($cm^2/V\cdot s$)	SS (V/dec)	I_{on}/I_{off}	$R_{SD}\cdot W$ ($\Omega\cdot$ cm)	ΔL (μm)
Al metal	0.22	16.84	0.14	$> 10^9$	4	0.1
Ar plasma	-0.28	14.28	0.31	$> 10^8$	50	2.5

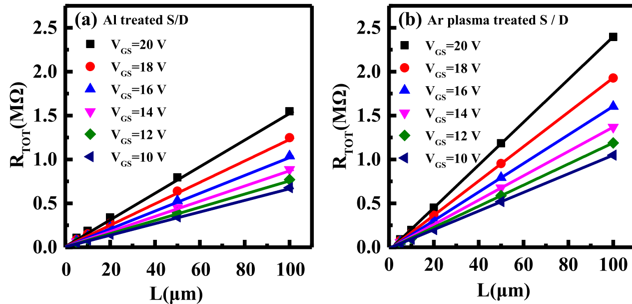

FIGURE 4. R_{TOT} of SATG a-IZO TFTs plotted as a function of L at various V_{GS} values for (a) Al-treated and (b) Ar plasma-treated devices.

the channel length (ΔL) were extracted by using transmission line method [20], where ΔL is the difference between the gate length and the effective channel length. The values of $R_{SD}\cdot W$ and ΔL of the Al-treated TFTs are approximately 4 $\Omega\cdot$ cm and 0.1 μm, respectively, and those of the Ar plasma-treated TFTs are approximately 50 $\Omega\cdot$ cm and 2.5 μm, respectively.

For the Al-treated device, the low resistance of the S/D region is attributed to the indium - oxygen coordination vacancies produced by the reaction of Al with IZO [20]. In addition, the negligibly small ΔL indicates that the source-drain region did not extend into channel region during the subsequent thermal process during the PECVD for passivation layer deposition.

Note that the S/D parasitic resistance of the Ar plasma-treated device is not as high as expected and the on-state characteristics are as good as those of the Al-treated device. In other words, the Ar plasma-treated S/D region still retains low resistance, even after the thermal deposition of PECVD SiO_2 passivation layer. The low resistance of S/D region is unlikely attributed to the Ar plasma treatment effect and is very likely caused by hydrogen diffusion during the PECVD processing of the SiO_2 layer. The large ΔL in the Ar plasma-treated device suggests a long S/D region extension generated under gate electrode caused by hydrogen further diffusion from the S/D region into the channel region, reducing the effective length of the channel region. In contrast, for the Al-treated device, the ΔL is small enough to be neglected, indicating that the source-drain region does not extend into the channel region. It is inferred that the thin Al_2O_3 layer generated on the source/drain region blocks the hydrogen diffusion into the S/D region during the PECVD processing of the SiO_2 layer.

Fig. 5 shows the transfer characteristics (I_{DS} - V_{GS}) of the fabricated SATG a-IZO TFTs with various L (1, 2, 5, 10 and 50 μm) (a) for the Al reaction-treated devices and (b) the Ar plasma-treated devices, respectively. The channel width W for all devices is 20 μm.

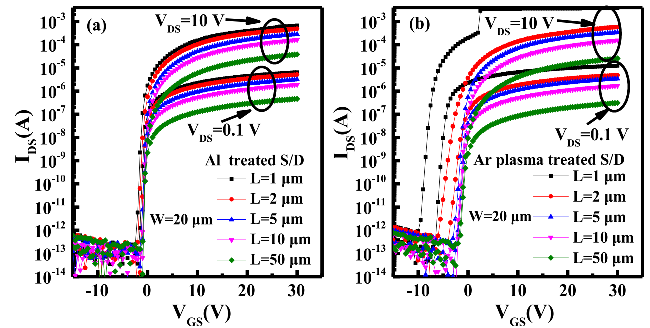

FIGURE 5. Transfer characteristics (I_{DS} - V_{GS}) of the fabricated SATG a-IZO TFTs at various gate lengths with (a) for the Al reaction-treated devices, and (b) for the Ar plasma-treated devices, respectively. The channel sizes: $W = 20\ \mu$m and $L = 1, 2, 5, 10$ and $50\ \mu$m.

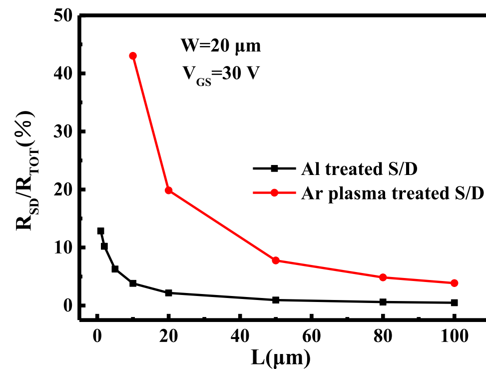

FIGURE 6. Ratio of R_{SD} to the R_{TOT} versus channel gate L for the Al reaction -treated and Ar plasma-treated TFTs.

As shown in Fig. 5 (a), the Al-treated TFTs retain superior electrical characteristics, even when the gate length L reduces to 1 μm, with no noticeable degradation of subthreshold

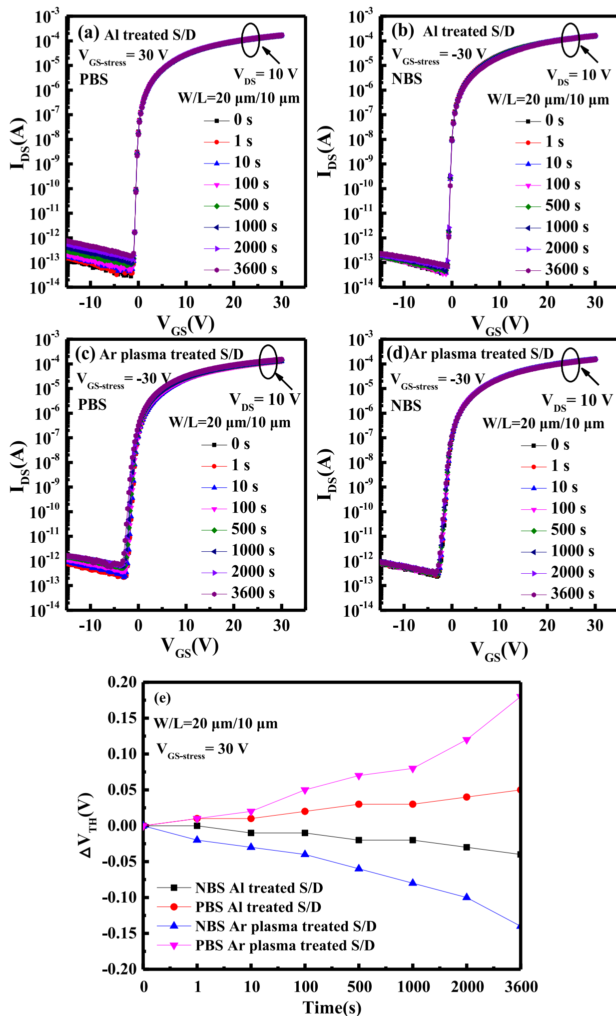

FIGURE 7. Evolutions of transfer characteristics of the fabricated IZO TFTs under positive gate bias stress (PBS) and negative gate bias stress (NBS), with (a) and (b) for Al treated ones, (c) and (d) for Ar plasma treated ones. The gate bias voltages ($V_{GS\text{-}stress}$) are 30 V and − 30 V for PBS and NBS, respectively, and (e) threshold voltage shift (ΔV_{TH}) versus stress time for both TFTs. The ΔV_{TH} under the PBS and NBS for one-hour are 0.05 V and − 0.04 V for the Al treated devices. They are 0.18 V and − 0.14 V for the Ar plasma treated ones.

swing (*SS*) and variation of threshold voltage observed. This finding suggests that the Al doping method allows the SATG a-IZO TFT an excellent scalability in addition to the formation of a self-aligned and low-resistance source-drain region. As shown in Fig. 5 (b), the Ar plasma-treated TFTs exhibit an obvious variation in electrical characteristics with the gate length reduction. In particular, the threshold voltage V_{TH} of devices shows a remarkable lowering with the gate length when it is shorter than 10 μm. The short channel effect should be caused by the diffusion of hydrogen into the channel region, thereby increasing the base electron concentration in the channel and reducing the effective channel length. The equivalent electron concentration increases with the gate length shortening.

Fig. 6 shows $R_{SD}/\ R_{TOT}$ ratio plotted as a function of gate length L at $V_{GS} = 30$ V for the Al reaction and Ar plasma-treated a-IZO TFTs. It is seen that the ratio for Al reaction-treated TFTs is much smaller than the Ar plasma treated ones when the L gets shorter and shorter. The ratio for the Al reaction-treated device with $L = 1\ \mu$m is calculated to be about 12.85%. In other words, the Al reaction method is good for short channel oxide TFTs.

Finally, we investigate the stability of the fabricated a-IZO TFTs under electrical bias stress. Fig. 7 shows the evolutions of transfer characteristics of the fabricated IZO TFTs under positive bias stress (PBS) and negative bias stress (NBS) stress, with (a) and (b) for the Al treated devices, (c) and (d) for the Ar plasma treated ones. The gate bias voltages, $V_{GS\text{-}stress}$ for the PBS and NBS were 30 V and − 30 V and the source and drain electrodes are grounded for both, and (e) threshold voltage shift (ΔV_{TH}) versus stress time for both TFTs. The Al treated TFTs exhibit a V_{TH} shift of 0.05 V under the one-hour PBS and − 0.04 V under the one-hour NBS, with nearly unchanged *SS* characteristics. On the other hand, the Ar plasma treated TFTs exhibit a V_{TH} shift of 0.18 V under the one-hour PBS and − 0.14 V under the one-hour NBS. It has been known well that the stability of oxide TFTs is usually affected by the hydrogen impurities in the channel region and the water molecules adsorption at the channel interface [21], [22]. The stability improvement in the Al-treated devices can also be attributed to the thin Al_2O_3 layer formed on source-drain area that blocks the diffusion of hydrogen or H_2O from the passivation layer into the source-drain and channel regions.

IV. CONCLUSION

To develop a self-aligned top-gate a-IZO TFT fabrication process, a technique featuring a thin Al layer deposition and subsequent annealing was applied to form low resistance S/D regions. A low sheet resistance of 360 Ω/□ was achieved in the Al-treated a-IZO layer. The availability of this technique was thus verified well. In addition, the Al-treated TFTs showed better electrical performances than the Ar plasma-treated ones, including the higher mobility, steeper subthreshold swing and larger on/off current ratio. One more important observation is the excellent scalability and stability with the Al-treated SATG device. This excellent scalability and stability were ascribed to the thin Al_2O_3 layer generated on the source/drain region, which blocks the hydrogen or H_2O diffusion into the source-drain or channel regions.

REFERENCES

[1] K. Nomura *et al.*, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488–492, Nov. 2004, doi: 10.1038/nature03090.

[2] J. S. Park, W.-J. Maeng, H.-S. Kim, and J.-S. Park, "Review of recent developments in amorphous oxide semiconductor thin-film transistor devices," *Thin Solid Films*, vol. 520, no. 6, pp. 1679–1693, Jan. 2012, doi: 10.1016/j.tsf.2011.07.018.

[3] T. Kamiya, K. Nomura, and H. Hosono, "Present status of amorphous In–Ga–Zn–O thin-film transistor," *Sci. Technol. Adv. Mater.*, vol. 11, no. 4, pp. 1–23, Aug. 2010, doi: 10.1088/1468-6996/11/4/044305

[4] Y. Song *et al.*, "Top-gated indium–zinc–oxide thin-filmtransistors with in situ Al_2O_3/HfO_2 gate oxide," *IEEE Electron Device Lett.*, vol. 35, no. 12, pp. 1251–1253, Dec. 2014, doi: 10.1109/LED.2014.2360922.

[5] M. Mativenga *et al.*, "Edge effects in bottom-gate inverted staggered thin-film transistors," *IEEE Trans. Electron Devices*, vol. 59, no. 9, pp. 2501–2506, Sep. 2012, doi: 10.1109/TED.2012.2205258.

[6] H.-C. Lin, M.-H. Wu, C.-W. Chan, R.-J. Lyu, and T.-Y. Huang, "Novel InGaZnO inverters utilizing film profile engineering," *Jpn. J. Appl. Phys.*, vol. 54, no. 8, pp. 1–4, Jul. 2015, doi: 10.7567/JJAP.54.081102.

[7] W.-J. Nam *et al.*, "55-inch OLED TV using InGaZnO TFTs with WRGB pixel design," in *SID Symp. Dig. Tech. Papers*, vol. 44, Jun. 2013, pp. 243–246, doi: 10.1002/j.2168-0159.2013.tb06190.x.

[8] D. H. Kang, I. Kang, S. H. Ryu, and J. Jang, "Self-aligned coplanar a-IGZO TFTs and application to high-speed circuits," *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1385–1387, Oct. 2011, doi: 10.1109/LED.2011.2161568.

[9] D. H. Kang, I. Kang, S. H. Ryu, Y. S. Ahn, and J. Jang, "Effect of SiO_2 and/or SiN_x passivation layer on thermal stability of self-aligned coplanar amorphous indium–gallium–zinc–oxide thin-film transistors," *J. Display Technol.*, vol. 9, no. 9, pp. 699–703, Sep. 2013, doi: 10.1109/JDT.2013.2244846.

[10] Z. Ye, L. Lu, and M. Wong, "Zinc-oxide thin-film transistor with self-aligned source/drain regions doped with implanted boron for enhanced thermal stability," *IEEE Trans. Electron Devices*, vol. 59, no. 2, pp. 393–399, Feb. 2012, doi: 10.1109/TED.2011.2175398.

[11] R. Chen, W. Zhou, M. Zhang, M. Wong, and H.-S. Kwok, "Self-aligned indium–gallium–zinc oxide thin-film transistor with phosphorus-doped source/drain regions," *IEEE Electron Device Lett.*, vol. 33, no. 8, pp. 1150–1152, Aug. 2012, doi: 10.1109/LED.2012.2201444.

[12] R. Chen, W. Zhou, M. Zhang, M. Wong, and H. S. Kwok, "Self-aligned indium–gallium–zinc oxide thin-film transistor with source/drain regions doped by implanted arsenic," *IEEE Electron Device Lett.*, vol. 34, no. 1, pp. 60–62, Jan. 2013, doi: 10.1109/LED.2012.2223192.

[13] M. Zhang *et al.*, "Self-aligned top-gate zinc oxide thin film transistors fabricated by reactive sputtering of metallic zinc target," in *SID Symp. Dig. Tech. Papers*, vol. 46, Jun. 2015, pp. 1173–1175, doi: 10.1002/sdtp.10045.

[14] J. Park *et al.*, "Self-aligned top-gate amorphous gallium indium zinc oxide thin film transistors," *Appl. Phys. Lett.*, vol. 93, no. 5, pp. 1–3, Aug. 2008, doi: 10.1063/1.2966145.

[15] S. Kim *et al.*, "Source/drain formation of self-aligned top-gate amorphous GaInZnO thin-film transistors by NH_3 plasma treatment," *IEEE Electron Device Lett.*, vol. 30, no. 4, pp. 374–376, Apr. 2009, doi: 10.1109/LED.2009.2014181.

[16] J. C. Park, H.-N. Lee, and S. Im, "Self-aligned top-gate amorphous indium zinc oxide thin-film transistors exceeding low-temperature poly-Si transistor performance," *ACS Appl. Mater. Interfaces*, vol. 5, no. 15, pp. 6990–6995, Aug. 2013, doi: 10.1021/am401128p.

[17] J. C. Park and H.-N. Lee, "Self-aligned coplanar amorphous indium zinc oxide thin-film transistors with high performance,"*Solid State Electron.*, vol. 103, pp. 195–198, Jan. 2015, doi: 10.1016/j.sse.2014.07.013.

[18] N. Morosawa, Y. Ohshima, M. Morooka, T. Arai, and T. Sasaoka, "Self-aligned top-gate oxide thin-film transistor formed by aluminum reaction method," *Jpn. J. Appl. Phys.*, vol. 50, no. 9R, pp. 1–4, Sep. 2011, doi: 10.1143/JJAP.50.096502.

[19] M. Narihiro *et al.*, "High mobility self-aligned top-gate oxide TFT for high-resolution AM-OLED," in *SID Symp. Dig. Tech. Papers*, vol. 44, Jun. 2013, pp. 85–88, doi: 10.1002/j.2168-0159.2013.tb06147.x.

[20] S. Lee and D.-C. Paine, "Identification of the native defect doping mechanism in amorphous indium zinc oxide thin films studied using ultra high pressure oxidation," *Appl. Phys. Lett.*, vol. 102, no. 5, pp. 1–2, Feb. 2013, doi: 10.1063/1.4790187.

[21] W.-T. Chen *et al.*, "Oxygen-dependent instability and annealing/passivation effects in amorphous In–Ga–Zn–O thin-film transistors," *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1552–1554, Nov. 2011, doi: 10.1109/LED.2011.2165694.

[22] J. K. Jeong, H. W. Yang, J. H. Jeong, Y.-G. Mo, and H. D. Kim, "Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistors," *Appl. Phys. Lett.*, vol. 93, no. 12, pp. 1–3, Sep. 2008, doi: 10.1063/1.2990657.

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