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Built-In Sheet Charge As an Alternative to Dopant Pockets in Tunnel Field-Effect Transistors

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ABSTRACT Dopant pockets in combination with a III–V heterostructure have become a staple in simulations of tunnel field-effect transistors (TFET) to achieve acceptable on-currents (I_{ON}) and to break the I_{ON}-subthreshold swing trade-off in pTFETs. Questions on the scalability and variability of these dopant pockets remain, however. We therefore propose an alternative concept using two opposite sheet charges at the tunnel junction that are realized by exploiting different bonding types. With fully quantum mechanical 30-band k.p-based simulations, we investigate two configurations that exhibit such sheet charges both at the device level and in a ring-oscillator: a lattice-matched GaAs-Ge-GaAs heterostructure TFET and a homostructure InGaAs TFET. By comparing to pocketed broken gap GaSb-InAs TFETs, we show that built-in sheet charge is a valid alternative for both nTFET and pTFET, with the prospect of lower variability and better scalability.

INDEX TERMS Heterostructures, tunnel transistors, TFET.

I. INTRODUCTION

The tunnel field-effect transistor (TFET) shows a path towards lower supply voltage operation (<0.5V) than a MOSFET, thanks to its potential for a sub-60mV/dec subthreshold swing (SS) [1], [2]. It achieves this through the use of band-to-band tunneling (BTBT), a quantum mechanical (QM) phenomenon that is activated by a large gate-induced electric field at the source-channel junction. In silicon, unfortunately, the large bandgap results in low ON-currents (I_{ON}), prompting research into different material systems such as III-V heterostructures [3]. These allow for a small or even zero effective bandgap at the tunnel junction in the case of respectively a staggered or a broken band alignment. Often, though, a heterostructure alone is not sufficient to obtain acceptable I_{ON}, and TFET simulations additionally rely on highly doped regions (called 'pockets') at the tunnel junction. These dopant pockets create a built-in field at the junction that enhances the tunneling probability and induces a steeper onset. Specific pocketed designs have also been proposed for III-V pTFETs to circumvent the I_{ON}-SS trade-off caused by the low density of states (DOS) in the conduction band of the source material [4]. Important questions remain, however, on the variability and scalability of dopant pockets, since in the small volume that they occupy, typically only a few nanometers wide, dopants become countable at scaled dimensions, and the required abruptness in the profiles becomes difficult to achieve.

Recently, a different approach was suggested based on III-nitrides, which consists of replacing the dopant pocket with a thin InN layer sandwiched between two GaN outer layers [5], [6]. The polarization mismatch of the inner InN layer with the outer GaN results in an opposite sheet charge at each of the interfaces, producing a built-in electric field like in the case of a dopant pocket. Preliminary simulations showed TFET performance similar to configurations with dopant pockets. The downside is that GaN-InN epitaxy is very difficult to realize because of an 11% lattice mismatch. Even if the growth itself would be possible, the resulting

strain would have a significant and complex impact on the magnitude of the sheet charges.

In this paper, we therefore propose an alternative to dopant pockets that relies on built-in sheet charge in material combinations without lattice mismatch. We propose two ways to realize these sheet charges: heterovalent interfaces and an antiphase domain (APD). We investigate an example of each using our full-zone k.p-based QM simulator Pharos [7]. Performance of the new device concept is analyzed at the device level for n- and pTFETs and at the circuit level in a ring-oscillator (RO), and compared to optimized broken gap TFETs with dopant pockets.

II. GENERAL CONCEPT

Our proposed concept relies on the realization of two opposite sheet charges at the tunnel junction by exploiting differences in bonding type. The charges result in a built-in electric field at the tunnel junction that enhances I_{ON}. At the same time, the fixed charges reduce the depletion length at both sides of the junction, resulting in relatively flat bands in these regions at tunneling onset and hence a steeper switching. Compared to dopant pockets, which depend on the dispersion of impurities in a small volume, built-in sheet charges have the advantage of being an areal density of charge, intrinsic to bonds at an interface. The magnitude of the charge and the resulting electric field are therefore not susceptible to discrete variations as device dimensions are scaled down. Furthermore, there is no risk of dopant tails, as the charges are confined to an interface and the region in between the charges can be left intrinsically doped.

A first way to realize these sheet charges is through a pair of heterovalent interfaces. These can be obtained by inserting a thin layer of a group IV material in between two III-V outer layers, grown in such a way that at one of the interfaces, there is a predominance of III-IV bonds, while at the other interface the majority of bonds is IV-V (see Fig. 1(a)). The deficiency, respectively excess of electrons at the interfaces results in two opposite sheet charges. As an example, we consider the GaAs-Ge-GaAs system, grown in the [111] crystal direction such that the GaAs consists of alternating Ga and As layers. Research based on density functional theory (DFT) has predicted that significant opposite sheet charges form at the Ga-Ge and Ge-As interfaces, giving rise to electric fields of up to 13MV/cm [8]. This material system has several other advantages for TFET implementation. First, it is lattice-matched, so no strain-induced defects are expected at the interfaces. Epitaxial growth of such structures has been shown in [10]. Second, with GaAs outer layers, there is a large bandgap material in the channel and drain regions, which is beneficial for the OFF-state as it reduces ambipolar current and direct source-drain tunneling. Third, with a Ge inner layer, the bandgap at the tunnel junction is relatively small. Other combinations, such as Si-GaP-Si, GaP-Si-GaP or Ge-GaAs-Ge also present heterovalent interfaces, but the large bandgap of the inner material would result in a low I_{ON}.

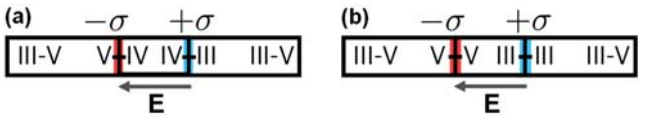


FIGURE 1. Schematic of ways to form built-in opposite sheet charges σ that create an electric field E: (a) heterovalent junctions, (b) an antiphase domain [8]. A third option, not discussed in this paper, is heteroatom epitaxy [9].

TABLE 1. Parameters of the simulated TFET configurations in Fig. 2.

	GaAs-Ge-GaAs		$In_{0.53}Ga_{0.47}As$	GaSb-InAs	
	nTFET	pTFET	nTFET	nTFET	pTFET
$L_{channel}$ [nm]	30	30	40	40	30
L_{gate} [nm]	30	30	20	20	26
T_{po} [nm]	1.66 (=5ML) 1 (=3ML)	1.66	0.68	2	2.5-2.5
N_{source} [cm^{-3}]	1x10^{20} (5ML) 5x10^{19} (3ML)	5x10^{18}	5x10^{19}	1x10^{20}	8x10^{18}
N_{po} [cm^{-3}]	undoped			1x10^{20}	1x10^{20}
σ_{po} [cm^{-2}]	9x10^{13} (5ML) 1.1x10^{14} (3ML)	9x10^{13}	1.2x10^{14}	/	
N_{drain} [cm^{-3}]	1x10^{19}	1x10^{19}	1x10^{19}	5x10^{18}	3x10^{19}

A second way to obtain sheet charges is by inserting an APD in a III-V material. The charge is then created due to "wrong bonds" (III-III and V-V) at the antiphase boundaries (see Fig. 1(b)). This requires the controlled formation of an APD. This is challenging, but impressive control of III-V crystal structure has been demonstrated [11], [12]. Here, we take the example of a [111]-grown homostructure $In_{0.53}Ga_{0.47}As$ TFET, but also heterostructures could be envisioned.

III. DEVICE LEVEL EVALUATION

We now investigate the GaAs-Ge-GaAs TFET and the $In_{0.53}Ga_{0.47}As$ TFET discussed in the previous section and compare them to pocketed broken gap GaSb-InAs TFETs (see Fig. 2 and Table 1). The simulated configurations correspond to wide nanosheets, but the sheet charge concept is applicable just as well to nanowires. $L_{channel}$ and L_{gate} of all configurations are chosen to keep direct source-drain tunneling and ambipolar current acceptable, while retaining well-behaved output characteristics. The broken gap pTFET in Fig. 2(b) has an improved source design to limit source degeneracy, while maintaining a strong electric field at the tunnel junction [4]. Transport is simulated with our ballistic QM simulator Pharos, which is based on a spectral full-zone 30-band k.p band structure model that takes into account the effects of size- and field- induced quantum confinement on the band structure [7]. The k.p parameters are fitted to bandgaps and effective masses from [13] and [14]. Electrostatics are calculated in Synopsys SDevice [15], with the sheet charges defined as fixed interface charge. The body thickness of the devices is chosen sufficiently wide

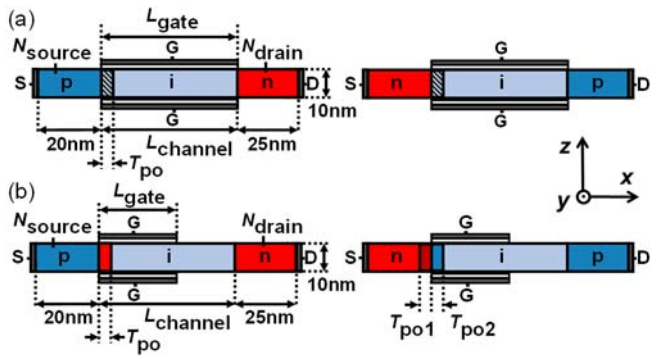


FIGURE 2. Simulated TFET configurations. EOT is 0.6nm with a work function of 4.55eV. The y-direction is considered to be translationally invariant, corresponding to a wide nanosheet. It has been checked that a gate-source overlap/underlap of +/- 1nm does not significantly affect the device characteristics. Other parameters are in Table 1. (a) Sheet charge enhanced nTFET and pTFET, where the hatched region denotes an intrinsic region bordered by two opposite sheet charges. (b) Broken gap nTFET and pTFET [4].

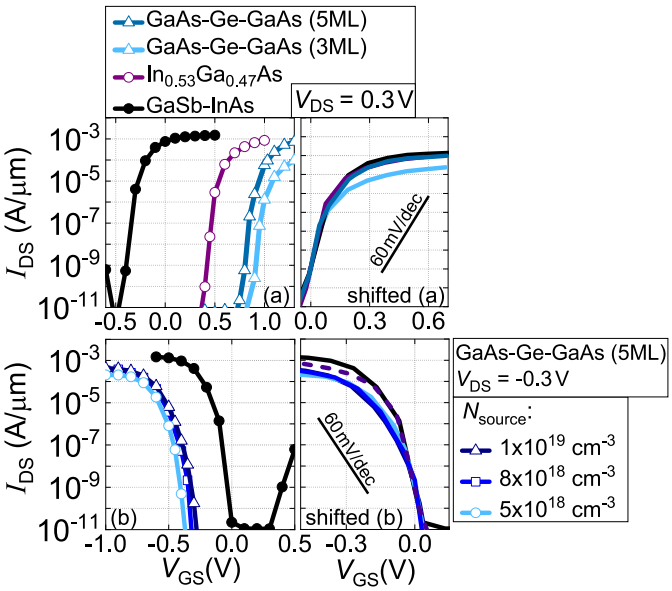


FIGURE 3. QM simulated transfer characteristics of sheet charge enhanced TFETs compared to pocketed broken gap TFETs. (a) nTFETs, for the GaAs-Ge-GaAs TFET illustrated with two values of T_{po} and N_{source}, and (b) pTFETs with the mirrored InGaAs nTFET curve as a dotted line. The shifted curves are such that I_{OFF} at 1nA/μm coincides.

such that the non-selfconsistent approach for the electrostatic potential is not expected to have a significant impact on the device characteristics. The sheet charge magnitudes and the dependence on layer thickness are calculated from electric field values extracted from DFT results in literature (see [8, Fig. 2(b)], and Table 1 for the sheet charge values). The distance between the sheet charges, T_{po}, is always taken as an integer number of monolayers (ML).

The transfer characteristics in Fig. 3(a) show that the nTFETs with the proposed sheet charge concept obtain comparable performance as a broken gap GaSb-InAs TFET with

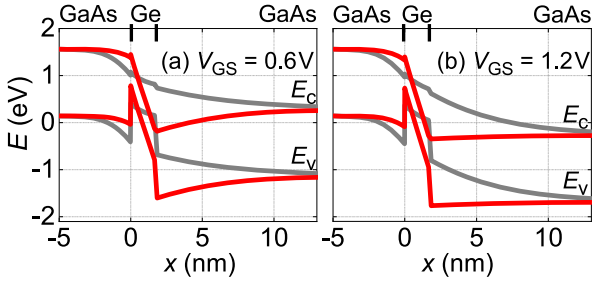


FIGURE 4. Band diagrams at the tunnel junction along a center cross-section of a GaAs-Ge-GaAs nTFET with a T_{po} of 5ML, comparing the bands with (red) and without (grey) sheet charge at the heterovalent junctions in the (a) OFF and (b) ON state. V_{DS} is 0.3V.

a 2nm dopant pocket. An I_{ON} is reached of 250μA/μm for the GaAs-Ge-GaAs and InGaAs TFETs and around 400μA/μm for the broken gap TFET (for a V_{DD} of 0.3V and I_{OFF} at 1nA/μm). I_{60}, the highest current for which the SS is sub-60mV/dec [16], is around 10μA/μm for all configurations. The band diagrams in Fig. 4 show that this performance is a result of the sheet charges at the interfaces, which enable relatively flat bands in the outer layers at tunneling onset and hence a sharp OFF-ON transition. Across the inner layer, a strong electric field is present, resulting in short tunnel paths in the ON-state. DFT results suggest that σ, and therefore E, decreases for larger T_{po} [8]. Since the band alignment of the two outer layers is determined by the product of σ and T_{po} [6], T_{po} should be optimized such that the bands at either side of the inner layer are almost flat at tunneling onset.

In the pTFET case, Fig. 3(b) shows for the GaAs-Ge-GaAs configuration that there is no severe I_{ON}-SS trade-off when varying source doping, contrary to typical III-V pTFETs. The sheet charges maintain the electric field at the tunnel junction, and the source doping only has a minor impact on it.

IV. CIRCUIT LEVEL EVALUATION

To capture the impact of the device-level performance differences between the various considered TFET configurations, we now also evaluate their performance in a representative RO circuit. This is a benchmark often employed in industry for a number of reasons [17], [18]. First, compared to a single inverter, an RO has no issues with the input slew rate definition because it is a self-driven system. This avoids having to make a choice of input signal and load, which also complicates the interpretation of the performance comparison. Second, if the fan-out and back end of line (BEOL) are chosen correctly, an RO is considered a good proxy for a system-on-a-chip (SoC) critical path. As we choose an inverter-based RO with a fan-out of 3 and BEOL wire length of around 50 times the contacted poly pitch (CPP), this corresponds to place-and-route results of an ARM core.

In particular, we consider a vertical nanosheet architecture, including device-internal, intra- and intercell parasitic

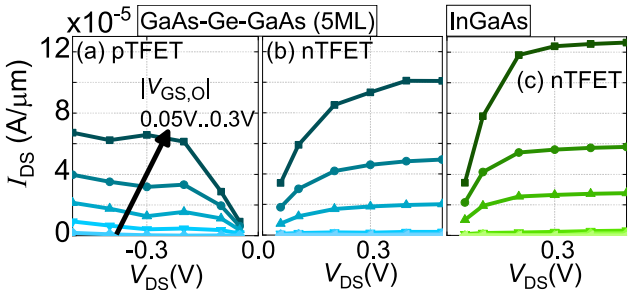


FIGURE 5. QM output characteristics of sheet charge TFETs for different V_{GS} beyond onset ($V_{GS,O}$). The kink in the current for $V_{DS}<-0.3V$ in (a) results from resonances in quantum wells near the tunnel junction. In the RO, however, operation is mainly below V_{DS}=0.3V.

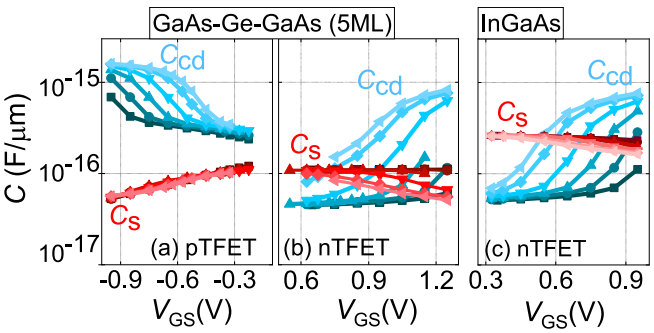
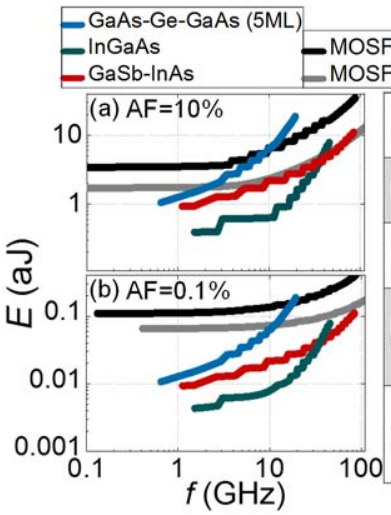


FIGURE 6. C-V characteristics, showing the gate-to-source capacitance (C_s) and gate-to-channel-drain capacitance (C_{cd}) for V_{DS} ranging from 0.05V to 0.5V (light to dark tones).

capacitances and resistances [19]. QM transfer and output characteristics (see Fig. 5) for a wide range of V_{GS} and V_{DS}, together with device-internal capacitance-voltage data extracted from SDevice (see Fig. 6), serve as input to calibrate a TFET compact model [20]. With this model, different application scenarios are explored by varying V_{DD} (0.1V to 0.5V) and I_{OFF} (1pA to 10nA). For each (V_{DD}, I_{OFF}) combination, we balance inverter noise margins (NM) with automatic adjustment of the work function depending on the relative strength of the n- and p-type device [21]. For (V_{DD}, I_{OFF}) combinations with NM > 30% of V_{DD}, a transient analysis is carried out, yielding energy-frequency (E-f) envelopes shown in Fig. 7 for two activity factors (AF) as in [21]. As a reference, (lateral) FinFET-based 7nm and projected 3nm node Si/SiGe MOSFET are also included [22], [23].

Overall, Fig. 7 shows that the sheet charge TFETs exhibit comparable energy consumption as the pocketed TFET. The slightly larger energy consumption of the GaAs-Ge-GaAs TFET can be explained by the lower I_{DS} over much of the V_{DD} range in the pTFET transfer characteristics (see Fig. 3(b)). Compared to the MOSFET, all investigated TFET configurations provide significantly lower energy consumption for 0.1% AF, especially at lower frequencies, thanks to their low leakage current and SS. The pocketed and InGaAs configurations also show energy gains compared to MOSFET for the higher AF of 10%.



	V_{DD} [V]	I_{OFF} [pA]
GaAs-Ge-GaAs	0.125	1.78
	0.5	31.6
InGaAs	0.1	10
	0.425	1
GaSb-InAs	0.15	1
	0.475	3.16
MOSFET 7nm	0.15	17.8
	0.275	10
	0.5	10^4
MOSFET 3nm	0.125	316
	0.325	17.8
	0.5	10^4

FIGURE 7. E-f envelopes of an inverter-based RO of three vertical TFET configurations and two lateral Si/SiGe MOSFET reference nodes for two AFs. For TFET, a 49x10nm vertical nanosheet per device is assumed. Interconnect load defaults to 50x the 32nm contacted gate pitch (C_{load}=0.4fF, R_{load}=~700Ω). Energy per switch for each (V_{DD}, I_{OFF}) is the sum of active power consumption and leakage during each delay [20]. An E-f envelope consists of the most energy-efficient (V_{DD}, I_{OFF}) pairs by Pareto optimization. The table contains (V_{DD}, I_{OFF}) for begin-and endpoints of the curves.

V. CONCLUSION

We presented built-in sheet charges at the TFET tunnel junction as an alternative to dopant pockets and showed comparable performance to pocketed broken gap TFETs, both at the device and circuit level. Sheet charge TFETs hold the prospect of better scalability and lower variability in advanced nodes. Comparison to Si/SiGe MOSFET 7nm and projected 3nm node indicates an energy gain window for TFET implementations, especially for low AF and low frequency applications.

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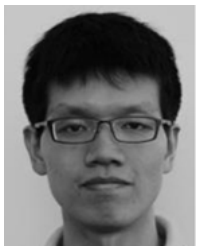

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