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SCR-Based ESD Protection Using a Penta-Well for 5 V Applications

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ABSTRACT This paper proposes a new structure of silicon controlled rectifier (SCR)-based ESD protection circuit using a penta-well for ESD protection in 5 V applications. The proposed circuit exhibits higher holding voltage and current-driving capability than low R_{on} SCR (LRSCR) ESD protection circuits. The existing LRSCR ESD protection circuit and the proposed ESD protection circuit were fabricated using the 0.18 μm BCD process. The electrical and latch-up characteristics were compared and analyzed using transmission line pulse measurement and a transient-induced latch-up test.

INDEX TERMS Silicon controlled rectifier (SCR), penta-well, holding voltage, current driving capability.

I. INTRODUCTION

Owing to the recent development of semiconductor processing technology, the miniaturization and high integration of integrated circuits has increased circuit speed, but the malfunction and destruction of circuits due to electrostatic discharge (ESD) is a serious problem. In cases of ESD destruction, metal electrodes, oxide insulation films, and junction surfaces are destroyed by the heat generated when ESD current is discharged due to thinning of the oxide insulation films [1]. ESD is therefore one of the most important issues in the safety and reliability of semiconductor integrated circuits [2], [3]. A typical ESD protection circuit, SCR, has excellent tolerance characteristics because it discharges ESD current into the silicon substrate. Low R_{on} SCR (LRSCR) improve upon the weaknesses of SCRs by introducing a high trigger and low holding voltage, and possess a low ON resistance and high tolerance characteristics [4]. However, their design parameters need to be optimized for use in 5 V applications, which increases the circuit size [5], [6]. Therefore, this paper proposes an SCR-based ESD protection circuit with a low ON resistance, and high holding voltage characteristics by using the 0.18 μm BCD layout minimum rule, without having to increase the circuit size.

II. PROPOSED ESD PROTECTION CIRCUIT

A cross-sectional view and a circuit diagram of the proposed ESD protection circuit are shown in Fig. 1. Its structural characteristics are as follows. Penta well and N+ drift are inserted to have higher holding voltage characteristics than LRSCR ESD protection circuit. The operation of the proposed ESD protection circuit is as follows. The anode voltage is increased by the ESD current flowing from the anode terminal. Electron–hole pairs are generated by an avalanche breakdown caused by the electric field having a high N + drift/P-well (cathode) junction. The electrons pass through the N + drift region and the N-well to the anode terminal, and the holes move to the cathode terminal to increase the potential of the cathode P-well. When this potential increases beyond the internal electric field of the P-well/N + cathode junction, the two junctions become forward biased and the parasitic NPN bipolar junction transistor (BJT) is turned on. In the proposed structure, the N-well/N + drift junction, which is the base of the PNP BJT PNP1, is also the base of the PNP BJT PNP2. The R_{NW} voltage drop of the collector current of the NPN transistor supplies the base current to PNP1 and PNP2, and both the PNP transistors and one NPN transistor are turned on. In the case of the LRSCR, the electron current then flows through the P + cathode, P-well, N +, N-well, and P + anode while

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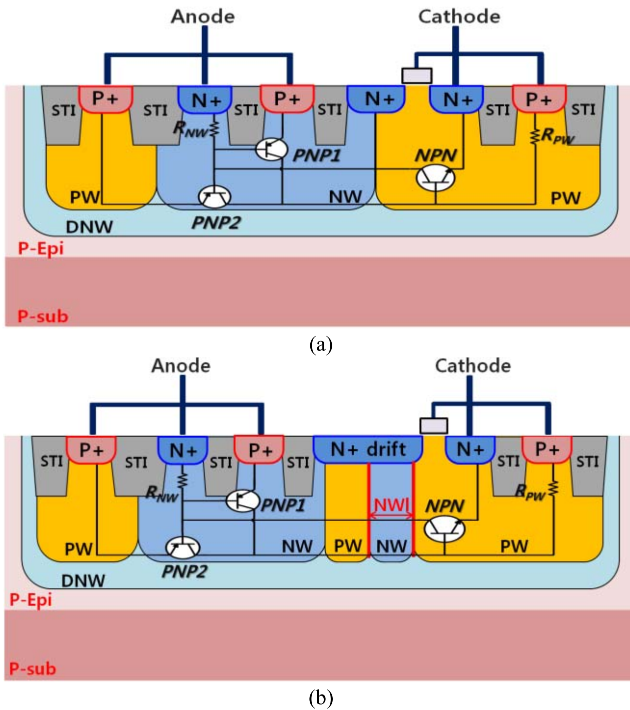

FIGURE 1. Cross-sectional view of (a) LRSCR (b) and proposed ESD protection circuit.

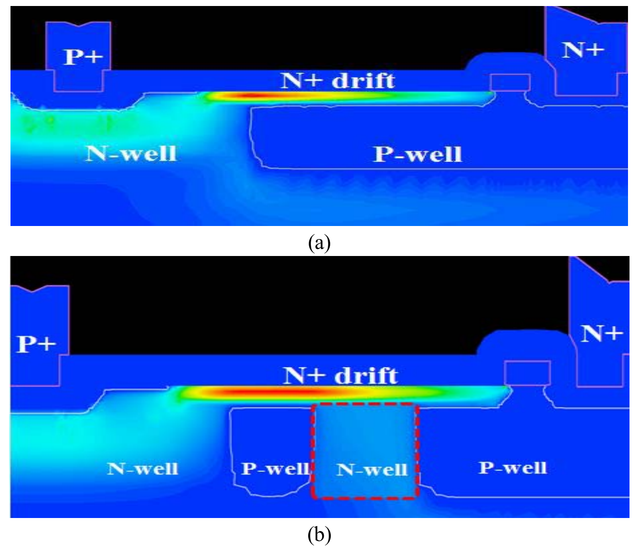

FIGURE 2. TCAD-simulated electron current flow (a) LRSCR (b) and proposed ESD protection circuit.

flowing from the cathode to the anode. Conversely, in the proposed ESD protection circuit, a long path of P + cathode, P-well, N-well, N + drift, N-well, and P + anode is formed because of an additional well of the red region shown in Fig. 1. Further, a longer effective base length of the parasitic PNP BJTs (PNP1 and PNP2) decreases the current gain. As a result, the proposed circuit has a high holding voltage due to a low positive feedback current gain when compared to an LRSCR. Fig. 2 shows a comparison of the electron current flow generated by a TCAD simulation in the LRSCR and the proposed ESD protection circuit. Fig. 2(b) shows the additional path flow of the electrons in the proposed circuit. At this time, the length of the N + drift region is the same in Fig. 2(a) and 2(b). The proposed circuit layout uses the minimum design rule and has a 4 µm longer total length dimension of 40 µm (total size : 40 µm ∗ 70 µm = 2800 µm^2) than the LRSCR dimension of 36 µm (total size : 36 µm ∗ 70µm = 2520µm^2). However, the LRSCR has a larger total length dimension of 43 μm (total size : 43µm∗70µm = 3010µm^2) than the proposed ESD protection circuit, in order to optimize the 5 V design windows. Therefore, the proposed circuit possesses the characteristics of latch-up immunity in addition to the advantages of reduced size and high holding voltage.

Fig. 3 shows the total current flow of the proposed ESD protection circuit. Fig. 3(a) shows the state of the proposed device before the trigger. As shown in the figure, in most currents, there is a weak avalanche breakdown current between the cathodes P- well and the N+ drift region. Fig. 3(b) shows the current flow in the trigger state of the proposed protection circuit. In this case, most of the current flows from the N+ drift region to the N+ cathode diffusion region through the operation of the parasitic NPN BJT. A voltage drop of the N- well occurs when electrons are injected into the N+ diffusion region. Fig. 3(c) shows the current flow at the moment when the ESD current is discharged after the full turn-on of the protection circuit and the turn-on to left parallel parasitic PNP bipolar. From this point, all of the SCRs in the proposed protection circuit are activated discharge the ESD current.

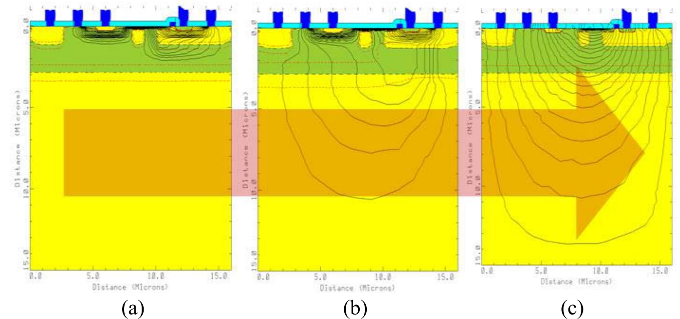

FIGURE 3. Total current flow of the proposed ESD protection circuit.

III. RESULTS AND DISCUSSION

The transmission line pulse (TLP) method is used to measure the electrical and endurance characteristics of both the proposed ESD protection circuit and the LRSCR, using 10 ns rising time and 100 ns pulse width [7]. Fig. 4 shows a TLP *I–V* curve comparing the proposed ESD protection circuit and the LRSCR through a 0.18 µm BCD layout. It displays a low trigger voltage of 9.5 V and a high holding voltage of 5.2 V, effective robustness of 6.2A and 6.8A (current limit

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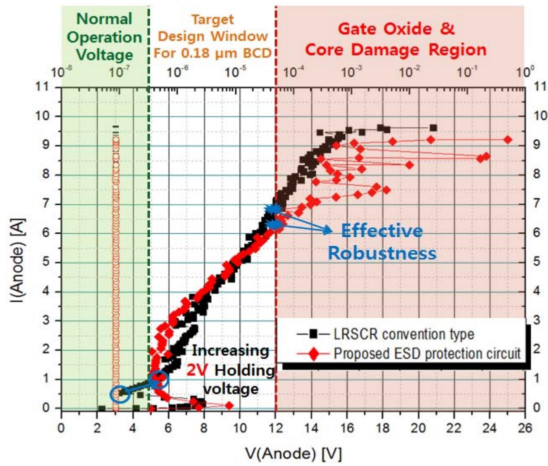


FIGURE 4. TLP I–V characteristic curves of LRSCR and proposed ESD protection.

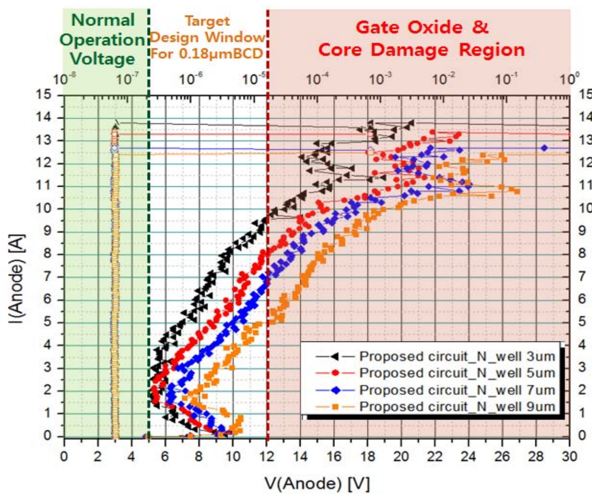
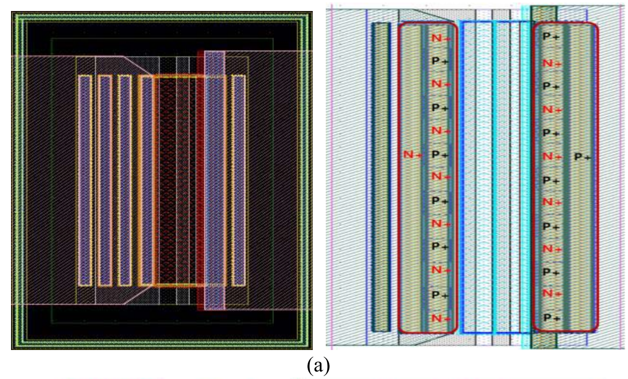


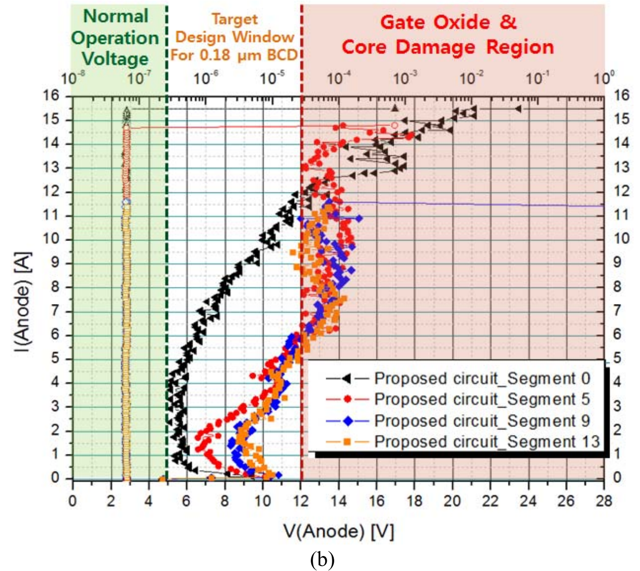
FIGURE 5. TLP I–V characteristic curves of the proposed ESD protection circuit for N-well parameter variation.

in the core damage region for 5V applications) as a result of the additional well and N + drift path. Furthermore, it has a low ON resistance of 1.35 Ω, similar to that of the LRSCR, due to the operation of PNP2. Fig. 5 shows a TLP *I–V* curve of the proposed ESD protection circuit for N-well design variables, which are varied in the range of 3–9 μm. As result, for a larger N-well, the base length of PNP1 and PNP2 and the length of the NPN current path formed through the N-well increase, decreasing the current gain and increasing the holding voltage from 5.3 to 7.11 V.

Fig. 6(a) shows the layout of the proposed circuit using a segmented emitter based on the 0.18 μm BCD process. This paper focuses only on a 1:1 segment ratio (one well tie-down region versus one emitter region). Fig. 6(b) shows a TLP curve of the proposed circuit with the number of emitter segments varying from 0 to 13. The measurement results show that the holding voltage increases from 5.11 to 8.73 V. Given that the number of segments in the segmented



(a)



(b)

FIGURE 6. (a) Proposed ESD protection circuit layout with 13 segments and (b) TLP I–V characteristic curves with varying segment number.

emitter affects the holding voltage, and therefore, reduces the effective emitter region of the parasitic PNP BJT and NPN BJT, the segmented emitter is implemented as shown in Fig. 6(a), with the segmented N+ and P+ diffusion regions separated by an n-well and a p-well, respectively. The proposed ESD protection circuit with the segmented emitter exhibits higher holding voltagethan that shown in Fig. 6. However, the second breakdown current (*It2*) decreases with an increasing number of segments in the emitter region, because of the current crowding phenomenon in the emitter region, which is caused by the smaller emitter region. Therefore, an increased holding voltage leads to a lower *It2*.

The thermal reliability of the proposed ESD protection circuit at high temperatures (300–500 K) is also measured, as shown in Fig. 7. The high temperature characteristics are important because they affect the electrical characteristics and It2 of the circuit [8]. In the thermal reliability test, the TLP system is used for the measurement, while the wafer is heated by a hot chuck system and a controller. The ESD protection circuit used for this measurement has an N-well length of 2 μm and 0 segments. When the temperature increases, the holding voltage decreases from 5.2 to 5.03 V

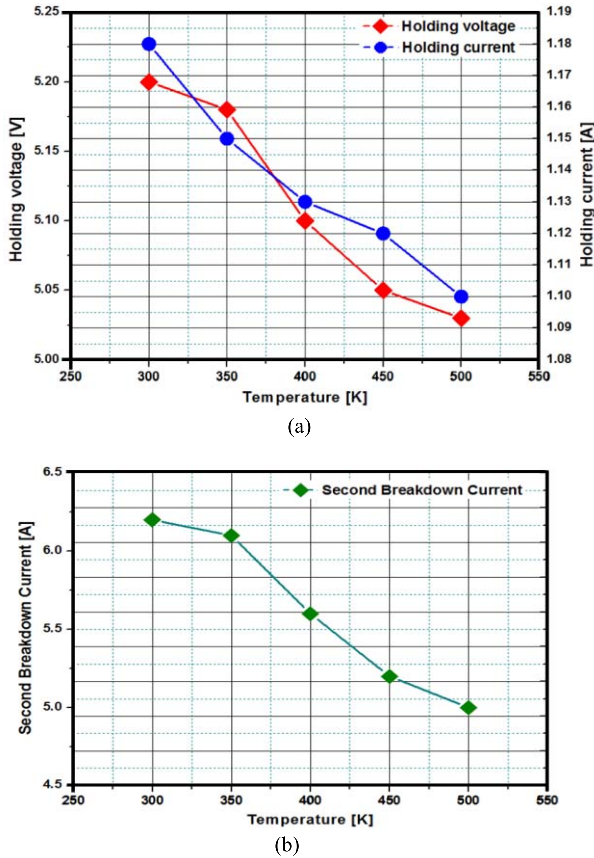


FIGURE 7. Electrical characteristic at high temperature (300 to 500 K): (a) holding voltage and current, (b) second breakdown current.

and the holding current decreases from 1.18 to 1.10 A, as a result of the increase in the current flowing through the diode. Thus, a decrease in the base-emitter voltage (VBE) of the parasitic NPN/PNP BJTs is observed, and therefore, the holding voltage decreases, as shown in (2). Further, the well and substrate resistances increase because of a decrease in carrier mobility at high temperature, causing a decrease in the holding current, as shown in (3).

$$V_h = V_{EBQ1} + V_{BCQ1} + V_{EBQ2} \quad (1)$$

$$V_h = V_{BEon} + V_{BCQ1} \quad (2)$$

$$I_h = \frac{V_{BEon}}{\beta_{NPN}\beta_{PNP} - 1}\left[\frac{1}{R_n}(\beta_{PNP}+1)\beta_{NPN} + \frac{1}{R_p}(\beta_{NPN}+1)\beta_{PNP}\right] \quad (3)$$

As the temperature increases, It2 decreases from 6.2 to 5.0 A because of thermal damage. Thus, the proposed ESD protection circuit exhibits outstanding thermal reliability.

Fig. 8 compares the results of the LRSCR and the proposed ESD protection circuit in a transient latch-up test [9], [10]. The ESD pulse is reproduced using a capacitor charged at the anode of the device under test, and the power supply is connected to a 5 V DC voltage, which corresponds to the supply voltage of the internal circuit on the same node. The holding voltage of the LRSCR is confirmed as shown in Fig. 8(a), in which the hold-up occurs due to a low holding voltage of 3.5 V. However, in the case of the proposed ESD protection circuit, the holding voltage is 5.2 V and the DC supply voltage is 5 V or more. After the operation of the ESD protection circuit, latch-up immunity is confirmed, as shown in Fig. 8(b), as the supply voltage returns to 5 V.

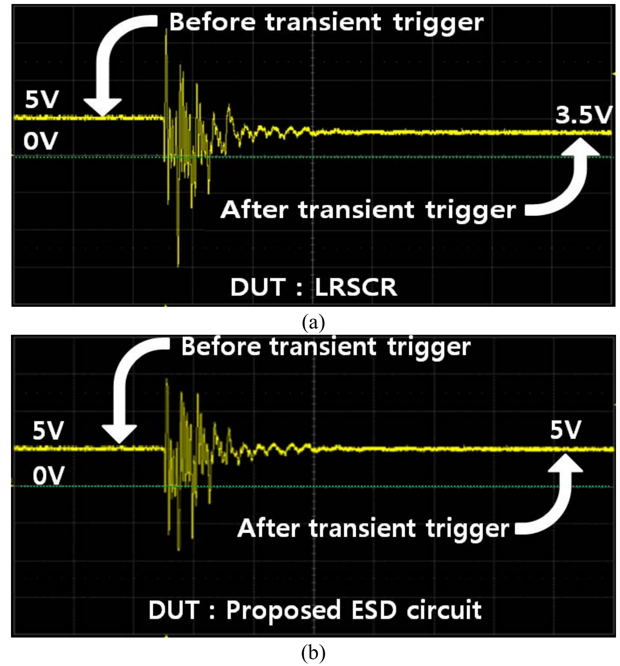


FIGURE 8. TLU measured voltage waveform (a) LRSCR (b) and Proposed ESD protection circuit.

IV. CONCLUSION

In this paper, we propose an ESD protection circuit with higher holding voltage characteristics as compared to those of an LRSCR. The LRSCR was designed to conform to a 5 V ESD design window through the optimization of the design variables. This led to an increase in the total cell area. The proposed ESD protection circuit was suitable for 5 V ESD design window applications with 5.2 V holding voltage, and had a smaller total cell size than the LRSCR. The electrical characteristics of the LRSCR and the proposed ESD protection circuit were verified through TLP measurements. As the N-well design variables were variable from 3 to 9 μm, the holding voltage increased from 5.3 to 7.11 V, and using the segment emitter layout, the holding voltage increased from 5.11 to 8.73 V. Furthermore, we also confirmed that TLU immunity is achieved. The proposed ESD protection circuit had an ON resistance of 1.35 Ω and an *It2* value of 6 A. It is expected that the application of the proposed circuit to 5 V power supplies will lead to increased area efficiency, which will lead to improved reliability and price competitiveness in these applications.

REFERENCES

[1] M.-D. Ker and C.-C. Yen, "Investigation and design of on-chip power-rail ESD clamp circuits without suffering latchup-like failure during system-level ESD test," *IEEE J. Solid-State Circuits*, vol. 43, no. 11, pp. 2533–2345, Nov. 2008, doi: 10.1109/JSSC.2008.2005451.

[2] O. Semenov, H. Sarbishaei, and M. Sachdev, "ESD protection design for advanced CMOS," in *Proc. SPIE*, 2001, pp. 123–131.

[3] Y. Koo, K. Lee, K. Kim, and J. Kwon, "Design of SCR-based ESD protection device for power clamp using deep-submicron CMOS technology," *Microelectron. J.*, vol. 40, no. 6, pp. 1007–1012, Jun. 2009, doi: 10.1016/j.mejo.2009.01.001.

[4] B. B. Song and Y. S. Koo, "Low Ron and high robustness ESD protection design for low-voltage power clamp application," *Electron. Lett.*, vol. 52, no. 18, pp. 1554–1555, Sep. 2016, doi: 10.1049/el.2016.2391.

[5] C.-Y. Lin and R.-K. Chang, "Design of ESD protection device for K/Ka-band applications in nanoscale CMOS process," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 2824–2829, Sep. 2015, doi: 10.1109/TED.2015.2450225.

[6] Q. Cui *et al.*, "High-robustness and low-capacitance silicon-controlled rectifier for high-speed I/O ESD protection," *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 178–180, Feb. 2013, doi: 10.1109/LED.2012.2233708.

[7] E. Grund and M. Hernandez, "Obtaining TLP-like information from an HBM simulator," presented at the EOS/ESD Symp., Anaheim, CA, USA, Sep. 2007, pp. 2A.3-1–2A.3-7, doi: 10.1109/EOSESD.2007.4401737.

[8] Q. Cui *et al.*, "High-robustness and low-capacitance silicon-controlled rectifier for high-speed I/O ESD protection," *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 178–180, Feb. 2013, doi: 10.1109/LED.2012.2233708.

[9] M. Kelly *et al.*, "Developing a transient induced latch-up standard for testing integrated circuits," in *Proc. EOS/ESD Symp.*, Orlando, FL, USA, 1999, pp. 178–189, doi: 10.1109/EOSESD.1999.819004.

[10] M.-D. Ker and S.-F. Hsu, "Evaluation on efficient measurement setup for transient-induced latchup with bi-polar trigger [CMOS IC reliability]," in *Proc. IRPS*, San Jose, CA, USA, 2005, pp. 121–128.

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