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Built-In Bias Generation in Anti-Ferroelectric Stacks: Methods and Device Applications

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ABSTRACT The discovery of ferroelectric (FE) properties in binary oxides has enabled CMOS compatible and scalable FE memories. Recently, we reported a simple approach to introduce non-volatility into state-of-the-art dynamic random-access memory stacks that show anti-FE (AFE) behavior. By employing a pair of electrodes with different work functions, a built-in bias is generated. Consequently, this bias modulates the energy potential of the AFE and enables two stable non-volatile states. Using this approach, a significant endurance improvement compared to hafnia-based FE memories can be obtained. In this paper, we investigate the possibility to bypass the usage of asymmetric workfunction electrodes. Using the interface-engineering approach, based on fixed charge or dipole formation, we show two additional methods for built-in bias generation within AFE layer stacks. By characterizing the film properties and performance of AFE capacitors, we compare and investigate retention and endurance of both work function-difference-based and interface-based AFE non-volatile memory. Finally, for the first time we present the concept of a binary oxide-based AFE tunnel junction that leverages both an interface and work function engineered AFE stack.

INDEX TERMS Anti-ferroelectric, tunnel-junction, non-volatile memory, DRAM.

I. INTRODUCTION

With the growth of the Internet-of-Things (IoT) and the rise of smart cities, the generation of data increases at a tremendous pace [1]. This so-called big data calls for a shift towards memory- or data-centric computing and increases the need for low-power low-latency non-volatile (NV) information storage. Currently, different concepts such as phase change [2], conductive bridge [3], magnetic [4] and ferroelectric (FE) [5]–[7] memories are considered as potential solutions that would guarantee low power, low latency and nonvolatility. Among the listed, FE memories are characterized with unmatchable low writing energy (which is in order of fJ) needed for storing one bit of information [8] accompanied by dynamic random-access memory (DRAM)-like endurance ($\sim 10^{15}$ stress cycles; see Fig. 1a). State-of-the-art FE memories are perovskite based and their scaling has saturated at the 90 nm technology node, limiting them to niche markets [9], [10]. The discovery of ferroelectric properties within the CMOS compatible hafnia-zirconia (HZO) mixtures [11], [12] enabled further scaling of FE memories to 2X nm nodes [6], [13] and beyond. Even though this discovery bridged the scaling gap between state-of-the-art technology nodes and FE memories, the reliability issues in binary oxide based FE memories still need to be fully solved. Due to the high coercive field close to the breakdown field strength, hafnia based FE memories suffer from dielectric breakdown and fatigue, i.e., closure of the memory window (MW). Consequently, the endurance of binary-oxide based FEs is significantly lower compared to state-of-the-art fully-optimized perovskite based FE materials [14]–[16].

Depending on the ratio of hafnia and zirconia in the HZO mixture, a monoclinic, orthorhombic or tetragonal

phase can be stabilized leading to paraelectric, ferroelectric or anti-ferroelectric (AFE) behavior, respectively [12]. Pure ZrO_2 thin films show AFE characteristics. Moreover, this AFE behavior is observed in state-of-the-art ZrO_2 based DRAM capacitor stacks [17], [18]. Analogous to perovskite based FEs [19], [20], ZrO_2 based AFE are characterized with higher endurance strength compared to their FE counterparts [18]. However, in contrast to FEs, AFEs have no remanent polarization at zero field and therefore cannot be used for nonvolatile storage. Recently, Pešić *et al.* demonstrated that non-volatility can be introduced in AFEs using asymmetric electrodes with different work functions (WF) [17], [18]. Details will be discussed in Section II-B. Using this approach, a significant improvement in the endurance compared to HfO_2 based FEs was achieved.

This paper is organized as follows: In the first part, interface and work function based built-in bias generation methods are presented. Afterwards, the device fabrication is described and the physics of the memory effect in biased AFE materials is revisited. Subsequently, the device performance of interface (IF) based and WF based AFE non-volatile memory are compared. Finally, the concept of an anti-ferroelectric tunnel junction, which is characterized by non-destructive read-out (in contrast to 1T-1C AFE-RAM) is presented.

II. BUILT-IN BIAS GENERATION

A. FREE ENERGY ENGINEERING: THEORETICAL ASSESSMENT

In this section, two methods for generation of the built-in bias required for the modification of the energy landscape of the material will be addressed. Before discussing details about the built-in bias generation, basic properties of AFE materials are discussed. Upon the application of an external electric field (higher than the critical field), AFEs exhibit field-induced ferroelectricity (FFE) manifested in the constricted polarization-voltage (P-V) hysteresis shown in Fig. 1b) (blue dashed line). With the removal of the electric field excitation, the energy potential (see inset of Fig. 1b) restores its stationary state at P = 0, thus losing its FFE properties. Furthermore, compared to non-volatile FEs, AFEs do not possess a non-zero remanent polarization and hence are cannot be used for non-volatile storage. To enable non-volatility, an introduction of a built-in bias is needed [17], [18]. In the following, two methods for the generation of the built-in bias, required for the modification of the energy landscape of the material, will be discussed.

B. FREE ENERGY ENGINEERING: WORKFUNCTION APPROACH

The first approach of built-in bias generation is based on asymmetric work function electrodes. Pešić *et al.* [18] reported that sandwiching of the AFE film with different workfunction electrodes generates the desired built-in bias field that can be employed to modify the energy landscape of an AFE capacitor and to enable non-volatile storage in state-of-the-art DRAM stacks (Fig. 1b inset). Consequently, the generated built-in bias field is sufficient to induce a hysteresis shift, and center the left branch of the AFE P-V loop (see Fig. 1b) towards zero-field. Centering of the left branch of the constricted hysteresis loop enables non-volatile switching between the polarized (binary "0") and non-polarized (binary "1") memory state.

The built-in bias field $E_{built-in}$ generated by using electrodes with different WF values is described by the following equation:

$$E_{built-in} = \frac{1}{t \cdot q} \cdot (WF_{TE} - WF_{BE}), \tag{1}$$

where t represents the thickness of the AFE, q is the elementary charge, WF_{TE} and WF_{BE} are the workfunction values for the top and bottom electrode, respectively.

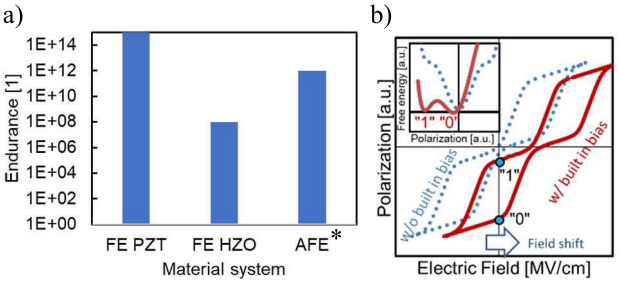

FIGURE 1. a) Field cycling endurance of a state-of-the-art perovskite capacitor (FE PZT) [8], ferroelectric 1:1 mixture of ZrO_2 and HfO_2 based capacitor (FE HZO) [12] and anti-ferroelectric ZrO_2 based capcaitor (AFE)* [18]. b) Model of polarization hysteresis of AFE materials at zero external fields with (solid) and without (dotted) built-in bias field. The shift in the polarization characteristics along the field axis results in a P_r at zero bias and therefore enables non-volatile data storage. Inset denotes corresponding free energy potential (solid) with and (dottet) without built-in bias at zero external field. *Extrapolated value.

C. FREE ENERGY ENGINEERING: INTERFACE APPROACH

In addition to the asymmetric electrode work function method [17], two additional, interface-based methods were proposed [21]. Here, we suggest that the required built-in bias field can be generated by either introduction of an interfacial dipole [22] (Fig. 2) or fixed charges between two dielectric layers [23]. A surface density difference of oxygen atoms at the interface between two oxide materials can be used as an intrinsic origin for dipole formation [22]. Alternatively, the composition change from one material to another can induce positive or negative fixed charge at the interface [23]. Both effects can be used for introduction of an internal bias field. It should be noted that the direction of the built-in bias field, generated by the asymmetric WFs, can be altered by combining the top electrode (TE) with a higher or lower workfunction material with respect to the bottom electrode (BE). On the other hand, interface charge effects or the dipole orientation can be controlled by the sequence of the deposited layers.

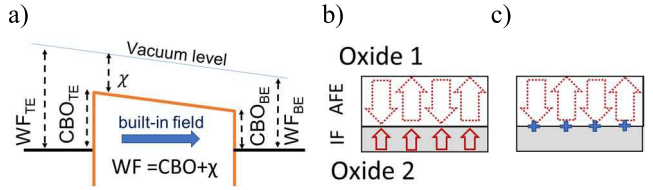

FIGURE 2. **Built-in bias field generation by a) asymmetric stack comprising electrodes with different work function values and by combining a heterostructure of two oxide materials with different surface density of oxygen which result in either b) dipole formation or c) introduction of fixed charges. CBO and χ denote conduction band offset and electron affinity respectively.**

III. FABRICATION STEPS AND CHARACTERIZATION METHODS

A. METAL-INSULATOR-METAL-STRUCTURES: FABRICATION

TiN/ZrO_2/RuO_x and TiN/ZrO_2/Al_2O_3/TiN metal-insulator-metal (MIM) test structures were deposited on Silicon substrates. The process flow of the TiN/ZrO_2/Al_2O_3/TiN capacitor stack fabrication is given in Fig. 3, whereas the details of the TiN/ZrO_2/RuO_x stack fabrication can be found in [18] and [24].

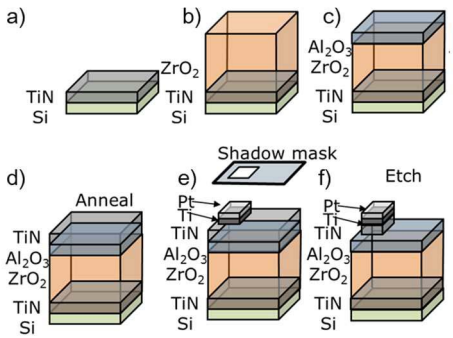

FIGURE 3. **Process flow used for fabrication of the capacitor stacks under test. a) PVD deposited TIN BE on Si substrate, b) ALD deposited ZrO_2 dielectric, c) ALD deposited Al_2O_3, d) PVD deposited TiN top electrode and crystallization anneal, e) PVD deposition of the Ti adhesion layer and Pt hard mask and f) etching of TiN and formation of discrete capacitor structures.**

First, a 12-nm thick TiN bottom electrode was deposited by physical vapor deposition (PVD) sputtering at room temperature. After the deposition of the BE, a ZrO_2/Al_2O_3 dielectric stack, with combined thickness of 12 nm, was grown by atomic layer deposition at 230 and 250°C, respectively. Al_2O_3 and ZrO_2 stacks were processed in H_2O process using trimethylaluminum (TMA), and Zr based metal organic precursor (TEMAZr) as reactants, respectively. To investigate the influence of the thickness of the interfacial Al_2O_3, the thickness ratio between Al_2O_3 and ZrO_2 was varied, while preserving the total thickness of 12 nm. The dielectric stack was capped by a reactively sputtered 12-nm thick TiN TE. In the following step, the dielectric was crystalized in nitrogen atmosphere by a 20 s rapid thermal anneal at 800 °C. The annealing step of the ZrO_2 film, confined in between two TiN electrodes, results in stabilization of the tetragonal phase (t-phase) which is responsible for the AFE behavior [6], [17], [25]. To prepare the stack for further structuring, circular hard masks consisting of 10 nm Ti (adhesion layer) and 50 nm Pt were deposited in an electron beam evaporator using a shadow mask. Finally, discrete capacitor structures were patterned by wet etching of the TiN in a standard-clean one (SC1) step, thus defining a device area of 9100 μm^2.

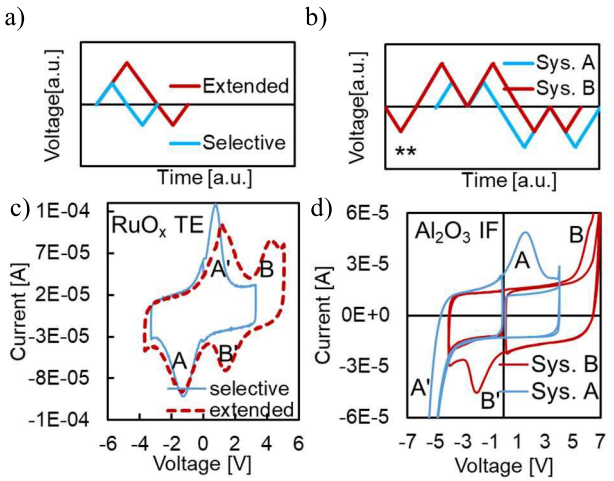

FIGURE 4. **Pulse waveform used to obtain the dynamic current of a) WF-engineered AFE capacitor (with indicated extended and selective sweep) and b) IF-engineered equivalent (with indicated left (A) and right (B) system). Comparison of AFE c) TiN/ZrO_2/RuO_x and d) TiN/ZrO_2/Al_2O_3/TiN stacks with extended range and selective read-out. Current peak pairs A-A′ and B-B′ denote left and right system of AFE film, respectively. *I-V characteristics are measured at 1 kHz. **PUND like waveform (b and d) is used to discriminate switching from leakage current.**

The above discussed approach should preserve the tetragonal nature and consequent anti-ferroelectric properties of the ZrO_2 based film and generate a built-in bias required for the centering of the left system (switching peak A and A'; see Fig. 4c) of the current-voltage (I-V) curve. Extension of the sweep towards more positive values proves that the TiN/ZrO_2/RuO_x stack is still anti-ferroelectric (Fig. 4c dashed trace) but shifted along the voltage axis. Analogous to the WF-engineered case, the IF-based approach results in biasing and centering of the A-A' peak pair around the origin. Introduction of the Al_2O_3 interfacial layer causes an additional voltage drop and requires the application of a higher voltage that consequently results in a high dynamic leakage current that is comparable to current component originating from switching (see Fig. 4d). On the other side, static current decreases with the increase of the interfacial thickness (see Fig. 5a) indicating the persistence of the interfacial layer. However, a possibility that a portion of the deposited Al_2O_3 diffuses during anneal cannot be totally excluded. Additional parasitics arising due to the interfacial Al_2O_3-based dead layer (and its persistence) will be discussed in detail in Section IV-B when addressing the retention of the device.

B. CHARACTERIZATION METHODS

To record the P-V response of the capacitors, an aixACCT TF Analyzer 3000 and Keithley 4200 SCS parameter analyzer were used. Retention and imprint experiments were performed using a semi-automatic probe station from Cascade Microtech and Keithley 4200 SCS parameter analyzer.

IV. COMPARISON OF IF AND WF BASED AFE-RAM

This section is devoted to the performance investigations of WF and IF engineered AFE memories reflected through the two most important reliability features, i.e., retention and endurance. In addition to benchmarking of these two solutions, engineering guidelines for improvements of these stack are suggested.

A. ENDURANCE

In Fig. 5b), a comparison of the endurance characteristics of WF-engineered and IF-engineered AFE non-volatile memory is shown. WF-engineered AFE memory exhibits a wake-up-free, [16], [26] stable endurance characteristic (see Figure 5) with slight operation induced imprint. It is assumed that the higher-phase uniformity of the film is responsible for the wake-up free behavior [24], [27], while the imprint is caused by asymmetry of electron injection into the device [28]. Compared to the WF-engineered case, the IF-engineered solution requires an increase of the operation voltage due to the voltage drop in the parasitically formed voltage divider comprising active ZrO_2 and dead Al_2O_3-based layer to achieve polarization values comparable to the WF-based counterparts. In addition, the charging of the ZrO_2/Al_2O_3 interface leads to biasing of the hysteresis and a drop of the remanent polarization. Increased stressing conditions lead to significant leakage, stress induced degradation and premature hard breakdown of the device.

B. RETENTION

Not only is the endurance of the device based on the IF-solution significantly deteriorated, but retention issues could arise as well. In addition to the voltage drop and subsequent increase of the operation voltage, the Al_2O_3 interface acts as a dead, non-switching layer that will cause a depolarization field [29], [30]. This depolarization field tends to flip the stored memory state and has detrimental impact on the retention of the device. A complete retention test is described by Rodriguez *et al.* [31] and was applied on AFE RAM in a previous study [27]. In the comprehensive retention study (reported in [27]) we pointed out that the non-polar (positive) state cannot be imprinted or disturbed due to the natural P=0 free energy minimum of the AFE. Hence, here we focus only on the retention of the polar state. The measurement principle is depicted in the inset of Fig. 5c) and it can be understood as follows: After the setting of the negative state, a read-out of the state was performed with sequentially increasing delay; Upon application of the negative set pulse, the current response comprises dielectric (permittivity related) component and switching current components; Subsequently, a control pulse of the same polarity should contain only a dielectric non-switching component if the polarization state is retained.

As expected with an increase of the thickness of IF layer, retention of the IF-engineered devices is reduced tremendously. Compared to the stable retention performance of the WF-engineered AFE RAM reported in [27], IF-based AFE RAM loses its retention within the first ms already at room temperature. This fast loss of the state can be explained by the increased depolarization field (the values given in Fig. 5d are calculated based on [29] and [30]) and non-significant built-in bias strength of the generated dipole/fixed charge magnitude. In addition to the desired shift of the I-V peaks by formation of the dipole/fixed charges, the IF depolarizes the film and results in higher fields needed for switching of the state. As a result, the distance between the switching peak B and the back-switching peak B' (see Fig. 4d)) increases to such an extent that the peak B' ends up occurring in the negative electric field polarity compared to WF-based solution where all peaks are biased in the same direction. An overview of these dependencies is given in Fig. 5d). Based on these assessments it can be concluded that the WF-based approach would be preferential for the implementation of the AFE non-volatile memory. Nonetheless, engineering of the interface by thinning and the choice of the material that has a higher surface oxygen concentration difference compared to Al_2O_3 would possibly ensure a dipole large enough to overcome the depolarization fields and modulate the energy potential, thus providing stable retention.

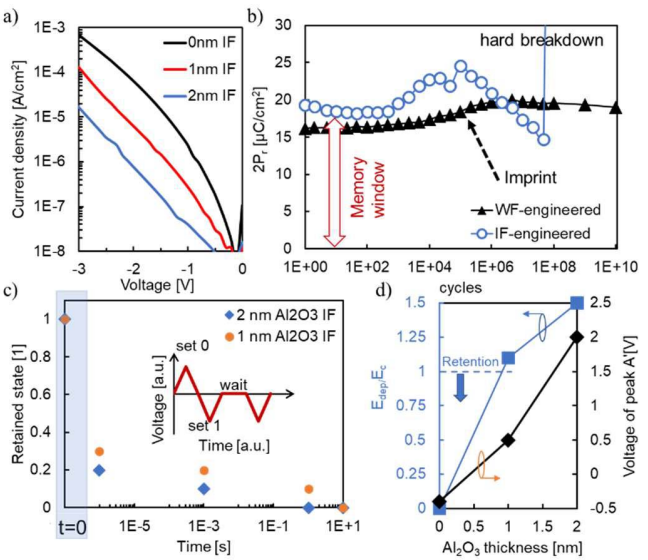

FIGURE 5. Reliability assessment of an AFE memory capacitor stack. a) Static I-V characteristics measured on MIMs with different interface thickness. b) Comparison of endurance of TiN/ZrO_2/RuO_x-(black triangles) and TiN/ZrO_2/Al_2O_3/TiN- (empty circles) based AFE RAM. c) Retention of the negative (polar) state measured on IF-engineered (TiN/ZrO_2/Al_2O_3/TiN) AFE capacitor test structures at room temperature. (inset) Waveform used for the assessment of the stored polar state. d) Depolarization field evolution and peak position of current peak A' as function of the thickness of the Al_2O_3 IF layer.

V. ANTI-FERROELECTRIC TUNNEL JUNCTION

In this last section a combination of the WF-engineered and IF-engineered stack will be discussed for potential memory applications. Similar to the FE counterparts, capacitor based AFE memories can be realized in two flavors, i.e.: a) AFE-RAM characterized with destructive read-out (DRO) and b) AFE tunnel junction (AFTJ) that exhibits non-destructive read-out (NDRO). The concept of the ferroelectric TJ (FTJ) was previously reported in [32]–[35]. Analogous to the FTJ here we suggest that the polarization state of the AFE can be exploited to modulate the band bending and thus the barrier height seen by tunneling electrons, obtaining either a high or a low resistance state (Fig. 6a)). To increase the ON/OFF ratio, a thin interfacial layer equivalent to that discussed in Section III-A can be used [35]. In contrast to FTJ, AFTJ requires a combination of the IF-engineered and WF-engineered device is required. The latter guarantees the non-volatility of the concept while the former assures a respectable magnitude of the tunneling probability and sufficiently high "ON/OFF" margin.

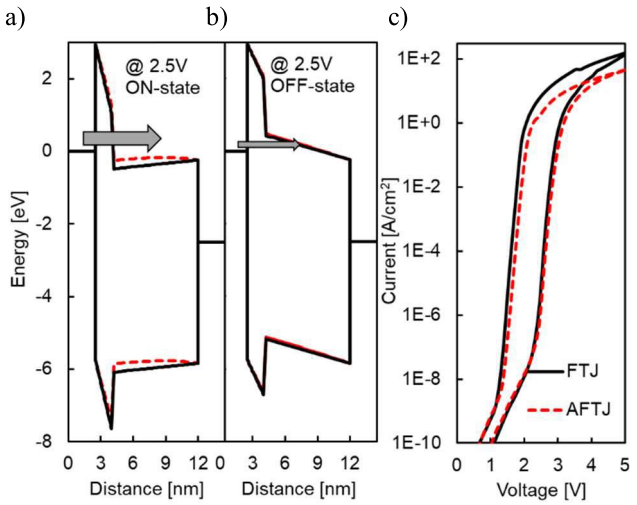

FIGURE 6. Band diagram of a simulated ZrO_2-based AFTJ (solid) compared to HfO_2-based FTJ (dashed) (with a 1.5-nm substoichiometric Al_2O_3 interfacial layer) showing the switching mechanism triggered by the polarization reversal in the a) ON (polar) and b) OFF (non-polar) state. c) Simulated I-V curves for 200 × 200 nm² (A)FTJ devices. Trap-assisted-tunneling based leakage current is enhanced only at low voltages (<3V), while the switching occurs at higher voltages, where Fowler-Nordheim tunneling dominates. *It should be noted that simulated structures differ in E_c, P_r and P_s as in the case of FTJ a positive and negative polarization is available compared to only one polar state in AFTJ.

To demonstrate the feasibility of the proposed concept using simulations, a $RuO_x/ZrO_2/Al_2O_3/TiN$ stack was implemented in commercially available MDLab software. For comparison a FTJ with the same properties and complete $2P_r$ (double to AFTJ) was simulated. (A)FTJ stack parameters are listed in Table 1 as reported in [24]. To investigate the influence of the AFE material solely on the characteristic of the TJ only P_r (P_s) and E_c were varied, whereas all remaining parameters of the band diagram were kept constant. Similarly to the interface-engineered AFE-RAM, a thinning of the Al_2O_3 layer is required for the reduction of the depolarization field and to provide long term retention of the AFTJ. ON and OFF state band diagrams and corresponding I-V characteristics are shown in Fig. 6a-b) and c), respectively.

TABLE 1. (A)FE tunnel junction simulation parameters.

Symbol	Quantity	Value
$2P_r$	Remanent polarization	23.5 (47) μC/cm²
$2P_s$	Saturation polarization	24 (48) μC/cm²
E_c	Coercive field of AFE (FE)	0.8 (1.2) MV/cm
Eg_{ZrO2}	Band gap of ZrO_2 (HfO_2)	5.6 eV
k_{ZrO2}	k-value of ZrO_2 (HfO_2)	30
Eg_{Al2O3}	Band gap of Al_2O_3	8.7 eV
k_{Al2O3}	k-value of Al_2O_3	9
N_t	Defect concentration	$6{\cdot}10^{19}$ cm^{-3}
WF_{TiN}	TiN workfunction	4.4 eV
WF_{RuOx}	RuO_x workfunction	5.2 eV

*values in parenthesis denote the simulation parameters of the FTJ

Independent on the realization of the active region (AFE vs. FE) OFF state is determined with the defect concentration and trap-assisted-tunneling (TAT) current component and hence stays constant. On the other side, ON state (and its onset) depends on the available polarization that modulates the band diagram in combination with the WF of the electrodes used. Consequently, a slightly higher ON/OFF ratio is observable for the FTJ compared to its AFTJ equivalent. Furthermore, the reduction of the WF of the TE (FTJ case) would results in earlier onset of the Fowler-Northeim and direct tunneling transport component.

VI. CONCLUSION

After our recent report of an AFE non-volatile memory concept, where asymmetric electrode materials induce a built-in bias field, thus enabling non-volatility in state-of-the art DRAM capacitors, we extend our study and focus on the possibility to bypass the usage of asymmetric work functions. Using the interface-engineering approach, based on fixed charge or dipole formation, we show two additional methods for built-in bias generation within the AFE stack. Based on its endurance and retention performance together with low operation voltages we conclude that the work function approach is more favorable.

Finally, we suggest the concept of a binary-oxide based anti-ferroelectric tunnel junction that combines work function asymmetry, which ensures non-volatility, and interface-engineering for an increase of the ON/OFF ratio of the memory device. By simulation we investigate the feasibility of the concept that would beside the decrease of the operation voltage enable non-destructive read-out operation.

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