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Direct Measurement of Active Near-Interface Traps in the Strong-Accumulation Region of 4H-SiC MOS Capacitors

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ABSTRACT This brief presents direct electrical measurement of active defects in the strong-accumulation region of N-type 4H-SiC MOS capacitors, which corresponds to the strong-inversion region of N-channel MOSFETs. The results demonstrate the existence of an active defect in the gate oxide, located very close to the SiC surface, with localized energy levels between 0.13 eV and 0.23 eV above the bottom of the conduction band. The observed spatial and energy localizations indicates that this is a well-defined defect.

INDEX TERMS 4H-SiC MOSFET, N-type SiC MOS capacitor, gate oxide, near-interface traps, trap measurement.

I. INTRODUCTION

Silicon carbide MOSFETs on 4H-SiC are now commercially available, performing beyond the theoretical limits of Si-based MOSFETs in terms of *on* resistance and blocking voltage. However, SiC MOSFETs are yet to reach the theoretical limits of SiC, the key problem being low channel-carrier mobility due to a high density of defects at or near the interface between SiC and the gate oxide [1]–[3]. The characterization of the interface between SiC and the gate oxide is typically based on capacitance and conductance measurements of N-type SiC MOS capacitors. These measurements are particularly sensitive in the depletion region, which has been adequate for the analysis of interface traps that are the dominant active defects in the case of Si-based MOS capacitors. Consequently, most of the characterization work for SiC-based capacitors has been focused on the depletion region [4], [5]. However, it has been shown recently that the active defects—the defects responsible for the low channel-carrier mobility in SiC MOSFETs—are in the strong-inversion of SiC MOSFETs [6]–[15], which corresponds to the strong-accumulation region of N-type SiC MOS capacitors [9]. These defects are identified as near-interface traps (NITs) [6]–[11], [14]–[21]. Three different techniques have been used to measure these defects: 1) conductance-based measurement in accumulation [9], [10], 2) measurements of current transients [8], and 3) thermal dielectric relaxation current (TDRC) technique [20]–[23]. There are possible issues with the conductance measurements in accumulation, due to the potential impact of the contact resistance and also due to high sensitivity to the specific calibration of the measurement equipment. With regards to the transient-current measurements, they can only measure traps with response times longer than tens of milliseconds. The TDRC technique fills traps by biasing MOS capacitors in accumulation, but this technique is limited to detecting traps with energy levels below the bottom of the conduction band because thermal emission—as distinct from tunneling—creates the thermal dielectric relaxation current. Therefore, there is a need for an alternative method of measuring the effects of defects in the strong-accumulation region of N-type 4H-SiC MOS capacitors.

In this brief, we present a direct experimental demonstration of active defects in the strong-accumulation region of N-type 4H-SiC MOS capacitors, which corresponds to the strong-inversion region in the case of N-channel 4H-SiC

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MOSFETs. The difference between measured alternating current through an MOS capacitor and the alternating current that corresponds to a trap-free MOS capacitor with a constant capacitance value is used to calculate the density of NITs as the active defects.

II. THE DIRECT MEASUREMENT METHOD

The voltage across a capacitor, v_C, is related to the current through the capacitor, i_C, by the following fundamental equation:

$$i_C = C\frac{dv_C}{dt} \tag{1}$$

The assumption of constant capacitance, C, in (1) is justified for the case of an ideal MOS capacitor in the accumulation region, especially for the case of small changes in the voltage v_C. If NITs impact the charging and discharging of the MOS capacitor due to a changing voltage v_C, then the measured current through the MOS capacitor, $i_{C\text{-}meas}$, will differ from the current given by (1). The difference between these two currents, $\Delta i_C = i_C - i_{C\text{-}meas}$, can be used to determine the density of NITs by the following equation:

$$D_{NIT} = \frac{1}{2kTqA}\int_{t_1}^{t_2} \Delta i_C(t)dt \tag{2}$$

In (2), the numerical integration of the current difference corresponds to captured/released charge from the NITs, which is divided by the capacitor area A and the electron charge q to obtain the density of NITs per unit area. Denoting the period of the sinusoidal signal by T, the integration limits are $t_1 = 0$ and $t_2 = T/2$ for the case of active NITs during capacitor charging, and $t_1 = T/2$ and $t_2 = T$ for the case of active NITs during capacitor discharging. Assuming that the energy width of NITs that are capturing and releasing electrons is $2kT$ [24], centered at the Fermi level, the density of NITs per unit area is divided by $2kT$ to obtain the density of NITs per unit area and per unit energy, labeled by D_{NIT}.

The direct measurement of current through a MOS capacitor can be performed by the RC circuit shown in Fig. 1.

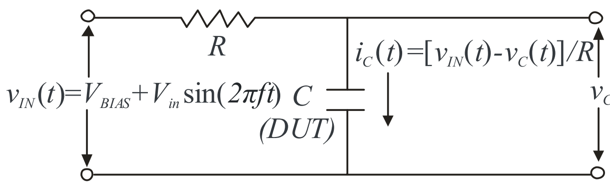

FIGURE 1. Configuration of the measurement circuit with *R* as an external resistor and *C* as the device under test (DUT).

The relationship between an arbitrary input voltage, v_{IN}, and the measured voltage across the capacitor, v_C, is

$$v_C = v_{IN} - Ri_C \tag{3}$$

From (1) and (3), the following differential equation is obtained:

$$\frac{dv_C}{dt} + \frac{1}{RC}v_C = \frac{1}{RC}v_{IN} \tag{4}$$

The solution of differential equation (4) is

$$v_C(t) = \exp\left(-\frac{t}{RC}\right)\left[A_0 + \frac{1}{RC}\int_0^t v_{IN}(t_S)\exp\left(\frac{t_S}{RC}\right)dt_S\right] \tag{5}$$

where A_0 is the integration constant and t_S is the variable time within the integration interval ($0 \le t_S \le t$). The measured input voltage $v_{IN}(t)$ is numerically integrated according to (5) to obtain the value of the voltage across the capacitor, $v_C(t)$, for the case of $D_{NIT} = 0$. The current through the MOS capacitor for the case of $D_{NIT} = 0$ is obtained by the following equation:

$$i_C(t) = \frac{v_{IN}(t) - v_C(t)}{R} \tag{6}$$

The condition that the DC component of the capacitor current has to be zero is used to set the correct value of the integration constant A_0.

The described procedure can be used to obtain the current $i_C(t)$ for arbitrary input voltages. However, high frequency sinusoidal signals are the most suitable because they minimize the signal distortion. In this work we have used sinusoidal input voltages, offset by a bias voltage V_{BIAS}:

$$v_{IN}(t) = V_{BIAS} + V_{in}\sin(2\pi f) \tag{7}$$

where f is the frequency of the applied sinusoidal voltage and V_{in} is the amplitude.

III. EXPERIMENTAL DETAILS

Measurements were performed on N-type 4H-SiC MOS capacitors, used as the device under test (DUT) in the RC circuit shown in Fig. 1. The MOS capacitors were fabricated on N-type, silicon faced, 4H-SiC wafers with nitrogen doped epitaxial layer at the concentration of 10^{16}cm^{-3}. Prior to the oxidation, the sample was cleaned by standard Radio Corporation of America (RCA) procedure. The oxidation was performed at 1250°C in dry O_2 for 60 min and then annealed in nitric oxide for 60 min, also at 1250°C. The resulting oxide thickness was 45 nm. The thickness of the oxide was determined from the accumulation capacitance, which was measured by Agilent B1505A LCR meter. Following the oxidation, aluminum was sputtered and patterned by photolithography to form square MOS capacitors with the area of 500x500 μm^2 and surrounding area of more than ten times the area of square MOS capacitors, to enable top-to-top measurements. Sinusoidal input voltages were applied to the smaller area through the external resistor R by a Tektronix AFG1022 arbitrary function generator and MP 3086 DC power supply, whereas the larger surrounding area was connected to the electrical ground. To measure the voltage across the capacitor, a Tektronix DPO7104 oscilloscope with Tektronix P6139A oscilloscope probes was used. The use of unshielded wires was minimized to avoid the impact of parasitic inductances, which was possible up to the frequency of $f = 8$ MHz (confirmed by the use of a constant-value

ceramic capacitor as the DUT). The lowest measurement frequency was 10 kHz. The measurements were performed with continuous sinusoids, therefore the presented results are the repetitive currents at given frequency. The parasitic capacitance is taken into account by matching the i_C waveform to $i_{C\text{-}meas}$, measured with constant-value ceramic capacitor as the DUT. The bias voltage was changed from $V_{BIAS} = 5$ V to 20 V whereas the amplitude of the input voltage was kept constant at $V_{in} = 500$ mV. Different resistor values were used to maintain similar output voltages at all measurement frequencies: $R = 180\ \Omega$ for 5 MHz, $R = 120\ \Omega$ for 6 and 7 MHz, and $R = 82\ \Omega$ for 8 MHz. It should be noted that a large leakage current would appear as a conductance in parallel with the capacitor and would impact the measured current. We measured the DC leakage through the capacitor (DUT) and confirmed that it was insignificant in comparison to the measured signal current. All the measurements were performed at room temperature.

IV. RESULTS AND DISCUSSION

The typical measured current, $i_{C\text{-}meas}$, is shown by the black lines in Figs. 2 and 3 for $f = 6$ MHz and $f = 7$ MHz, respectively, along with the current i_C that corresponds to the constant-capacitance value C (the gray lines). The difference between $i_{C\text{-}meas}$ and i_C is much larger at 7 MHz in comparison to 6 MHz. For the case of 7 MHz, the difference between these currents is the largest at $V_{BIAS} = 11$ V, which can also be seen from the plots of Δi_C shown in Fig. 4. For the case of $V_{BIAS} = 11$ V, it is clear that $i_{C\text{-}meas}$ is smaller than i_C during charging of the capacitor, which indicates that the charging current is reduced by delayed emission of electrons from the NITs. The difference during discharging of the capacitor is much smaller, indicating that there is almost no delayed electron capturing to reduce the charging current. Multiple devices were measured to confirm the repeatability of the results. We have not observed larger measured current in comparison to the ideal current.

The observed impact of the bias voltage can be related to the surface position of the Fermi level, E_F, and the energy location of the active NITs, E_{NIT}. Because of the quantum confinement effect, the Fermi level is above the bottom of the conduction band, E_C, in the case of strong inversion of P-type SiC and accumulation of N-type SiC [9]. As a consequence, the energy levels of the active defects—centered around the Fermi level—are also above E_C, which means that these defects have to be NITs positioned near the SiC surface that trap and release electrons by tunneling. In [12], the quantum confinement effect is considered to calculate the areal density of electrons in strong-inversion (N_{inv}) as a function of the position of the Fermi level E_F-E_C. Taking into account that the energy bands of P-type SiC in strong-inversion are very similar to the energy bands of N-type SiC in accumulation [9], we used the results from [12] for N_{inv} versus E_F-E_C to determine the positions of the Fermi levels for different applied bias voltages in our samples. To do so, we replaced N_{inv} by N_{acc}, which was calculated by

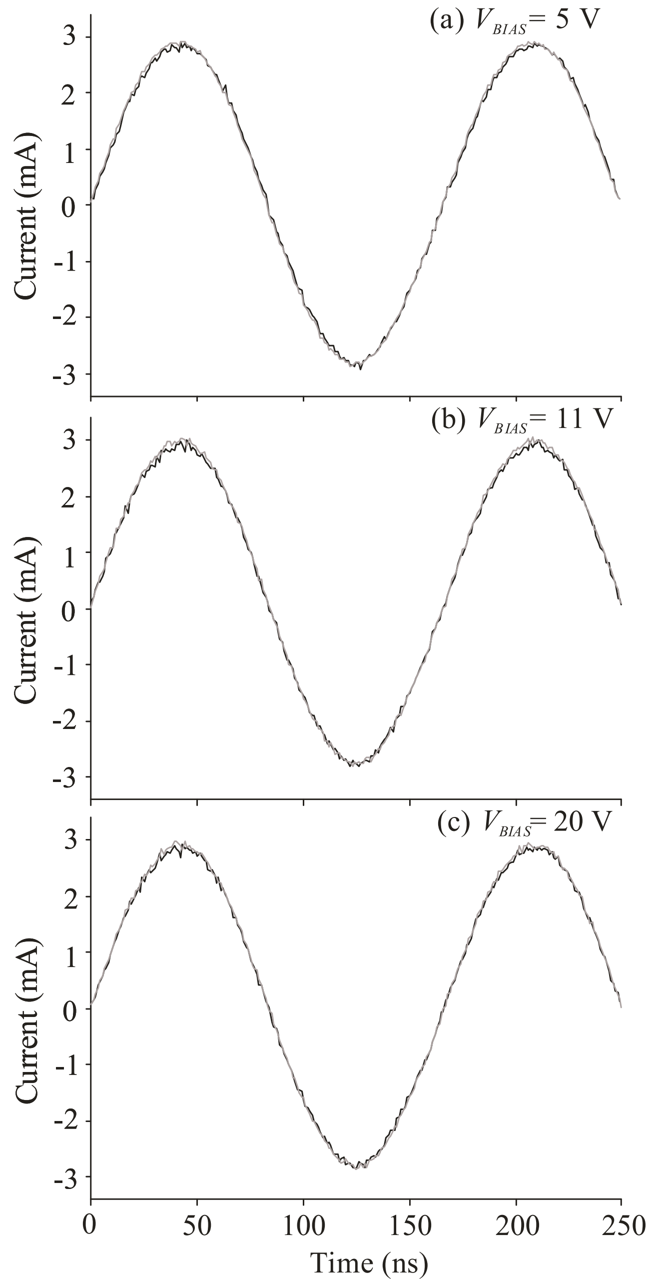

FIGURE 2. The measured current (black lines) and the current corresponding to constant capacitance C (gray lines) at 6 MHz for (a) 5 V bias voltage, (b) 11 V bias voltage and (c) 20 V bias voltage.

the following equation:

$$N_{acc} = \frac{(V_{BIAS} - V_{FB})\, C_{ox}}{q} \tag{8}$$

where V_{FB} is flat-band voltage and C_{ox} is oxide capacitance in accumulation per unit area. The value of the flat-band voltage was $V_{FB} = 0$ V, as determined concurrently with the gate oxide thickness by fitting the theoretical to the measured C–V curve. This relationship between V_{BIAS} and $N_{acc} \approx N_{inv}$, combined with Pennington and Goldsman's

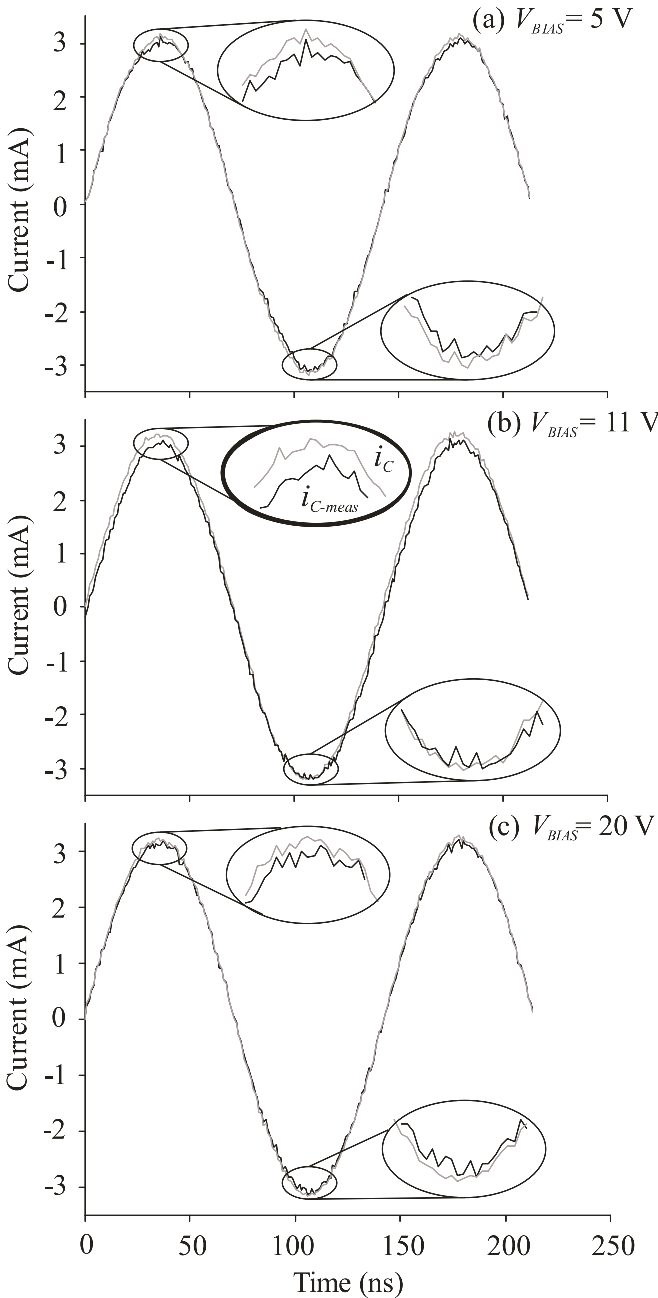

FIGURE 3. The measured current (black lines) and the current corresponding to constant capacitance *C* (gray lines) at 7 MHz for (a) 5 V bias voltage, (b) 11 V bias voltage and (c) 20 V bias voltage. The difference between these currents is the largest for 11 V bias voltage, indicating NITs with localized energy levels.

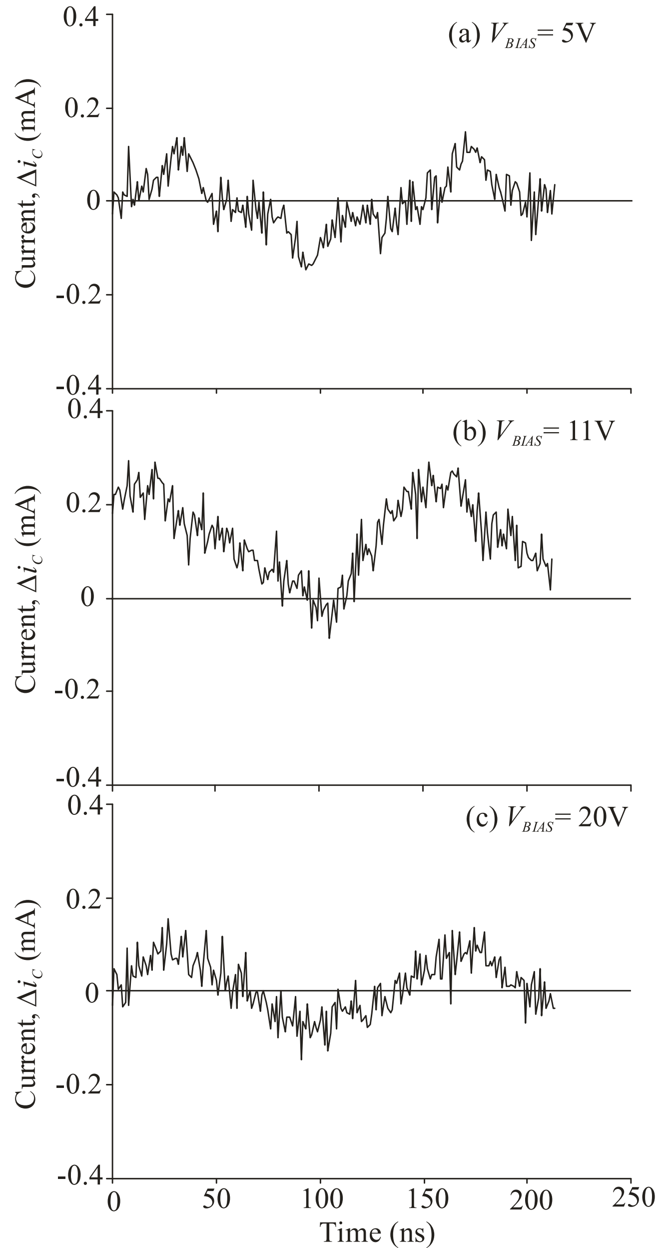

FIGURE 4. Current difference $\Delta i_C = i_C - i_{C\text{-}meas}$ at 7 MHz for (a) 5 V bias voltage, (b) 11 V bias voltage and (c) 20 V bias voltage.

relationship between N_{inv} and E_F-E_C $\approx$ E_{NIT}-E_C, enabled us to convert V_{BIAS} into E_{NIT}-E_C, as shown in Fig. 5.

The energy distributions of D_{NIT}, calculated by (2) for the case of charging currents, are shown in Fig. 6. The first implication from the results shown in Fig. 6 is that the energy levels of the dominant NITs are localized between 0.13 eV to 0.23 eV above E_C indicating a well-defined defect. The results in Fig. 6 also show that the localized defect is spatially localized as well, appearing very close to the SiC surface. We conclude this from the fact that there is a sharp increase in the D_{NIT} from about 2x10^{11} cm^{-2}eV^{-1} to 8x10^{11} cm^{-2}eV^{-1} when the frequency is increased from 6 MHz to 7 MHz. As mentioned previously, the delay of electron emission from the NITs is observed at 7 MHz, indicating that the emission time constant is approximately equal to the quarter of the signal period: $1/4f = 36$ ns. The emission of these electrons at around the quarter of the period opposes the charging current, causing the smaller $i_{C\text{-}meas}$ in comparison to the ideal case of $D_{NIT} = 0$. The quarter of the period in the case of the 6 MHz signal is $1/4f = 42$ ns, which is a sufficiently long time for the NITs

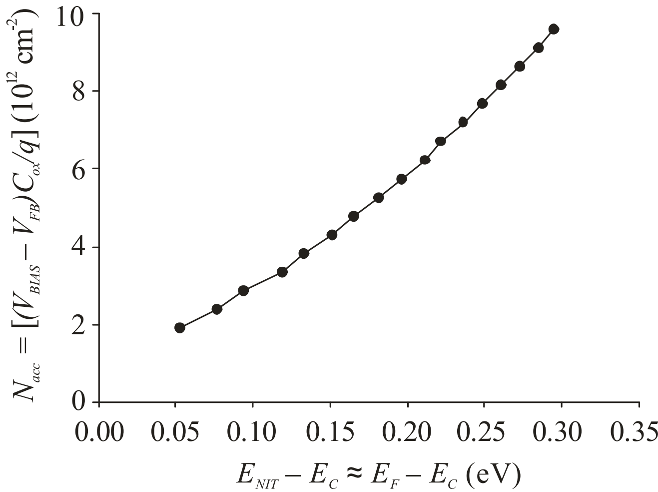

FIGURE 5. **Conversion of V_{BIAS} to E_{NIT}-E_C, based on the data from [12] for the relationship between the electron density, $N_{inv} \approx N_{acc}$, and the position of the Fermi level, E_F-E_C.**

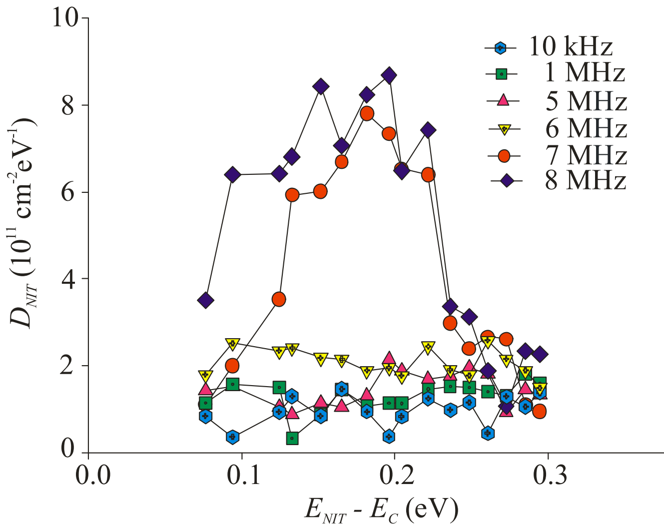

FIGURE 6. **Measured density of near-interface traps.**

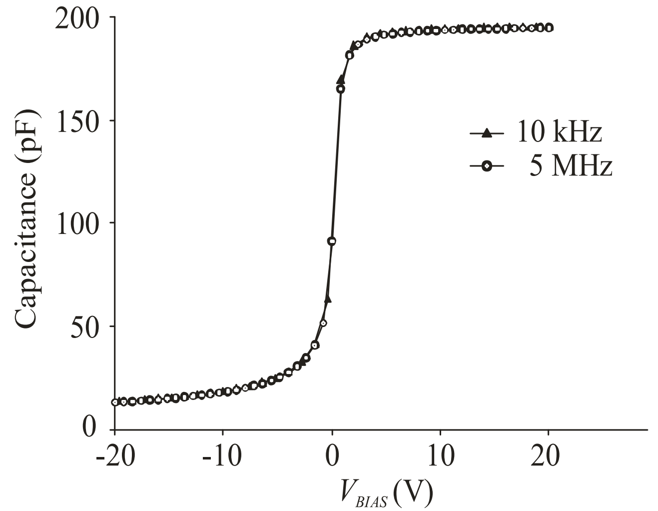

FIGURE 7. **Capacitance–voltage curves of the measured MOS capacitors. For clarity the lowest and highest frequency C–V curves are shown. There was no difference observed in the C–V measurement at the following measurement frequencies: 10 kHz, 100 kHz, 1 MHz, 2 MHz, 3 MHz, 4 MHz, and 5 MHz.**

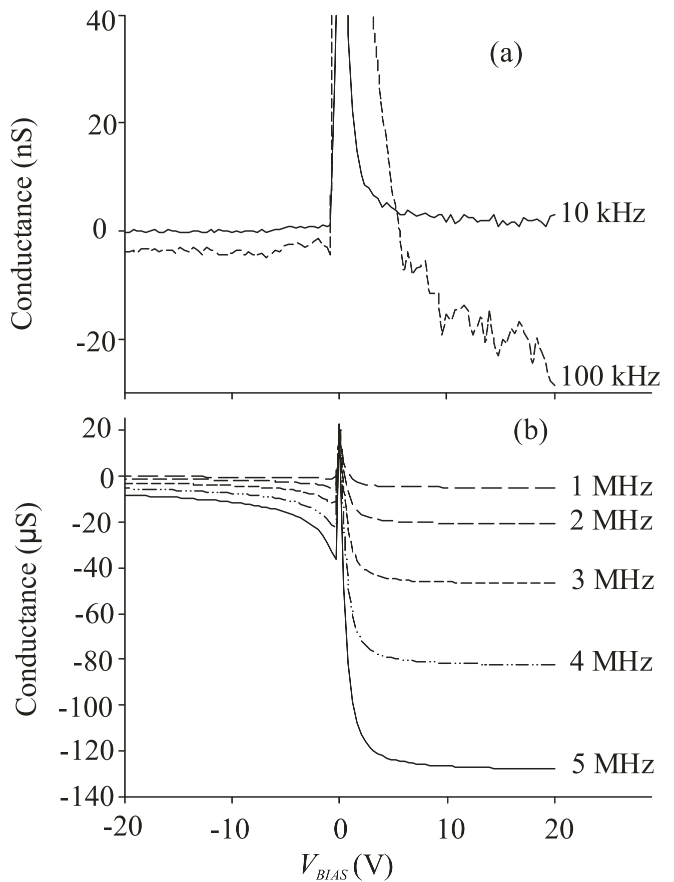

FIGURE 8. **Conductance–voltage curves of the measured MOS capacitors: (a) 10 kHz and 100 kHz, (b) 1–5 MHz.**

to emit the captured electrons, as evidenced by the absence of significant reduction in $i_{C\text{-}meas}$. This sharp increase of D_{NIT} with emission time shorter than 42 ns corresponds to a sharp localization of NITs near the interface.

Although the result about the localisation of NITs is new, the range of D_{NIT} values obtained by the measurement technique presented in this paper are in a good agreement with the values of 1x10^{11} cm^{-2}eV^{-1}, 9x10^{11} cm^{-2}eV^{-1} and 1x10^{11} cm^{-2}eV^{-1} published in [14], [16], and [18], respectively.

The results of our direct measurements of the current through the DUT, $i_{C\text{-}meas}$, in response to sinusoidal voltage, v_{IN}, have an important implication for the capacitance and conductance measurements by commercial LCR meters. The LCR meters model the DUT by an equivalent capacitance and an equivalent conductance (or resistance). An implicit assumption in this approach is that the current through the DUT is sinusoidal with amplitude and phase shift corresponding to the values of the capacitance and conductance

in the equivalent circuit. Our direct measurement of the current through the DUT shows a distortion from the sinusoidal shape, which cannot be adequately represented by a simple phase shift due to a conductance in parallel with the capacitance C. A consequence is that the distorted sinusoid cannot be properly fitted by the LCR models to result in physically meaningful capacitance and conductance. We measured the MOS capacitors by Agilent B1505A LCR meter, and with careful calibration, we were able to obtain constant capacitance in accumulation up to 5 MHz (the Agilent frequency limit), as shown in Fig. 7. However, the corresponding conductance in accumulation appears as positive only at 10 kHz and then becomes negative at higher frequencies, as shown in Fig. 8. Although this does correlate with the fact that there is a small discrepancy between i_C and $i_{C\text{-}meas}$, the physical meaning of the conductance is lost. We assume that the fitting problem (impossibility to fit ideal sinusoid with a phase shift to measured distorted sinusoids) results in conductance calculations that are highly sensitive to small differences between i_C and $i_{C\text{-}meas}$.

V. CONCLUSION

In this brief, N-type 4H-SiC MOS capacitors are used to perform direct measurements of near-interface traps that capture channel electrons in SiC MOSFETs, reducing the average channel-carrier mobility. The measurement technique utilizes the difference between measured alternating current through an MOS capacitor and alternating current that corresponds to a trap-free MOS capacitor with a constant capacitance value. The measurements performed on nitrided gate oxides identified a defect with energy levels localized between 0.13 eV and 0.23 eV above the bottom of the conduction band, which is also spatially localized very close to the SiC surface.

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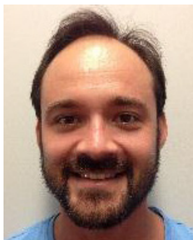

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