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Impact of Atomic Layer Deposition High k Films on Slow Trap Density in Ge MOS Interfaces With GeO_x Interfacial Layers Formed by Plasma Pre-Oxidation

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ABSTRACT For realizing of Ge complementary metal–oxide–semiconductor with a Ge gate stack with thin equivalent oxide thickness, low interface state density (D_{it}) and high reliability. In this paper, we examine the slow trap behaviors in the ALD high-k materials including Al_2O_3, Y_2O_3, HfO_2, and La_2O_3 on GeO_x/Ge interfaces, where the GeO_x interfacial layers are formed by plasma pre-oxidation. The C–V curves, D_{it} and slow trap density of the high-k/GeO_x/n- and p- Ge MOS capacitors are evaluated and compared. The Ge 3d spectra in X-ray photoemission spectroscopy are also compared among the Al_2O_3, Y_2O_3, HfO_2, and La_2O_3 on GeO_x/Ge structures. It is found that Al_2O_3 provides the lowest slow trap density for both electrons and holes in comparison with Y_2O_3, HfO_2, and La_2O_3 high-k films, while similar D_{it} values are observed among the MOS interfaces with Al_2O_3, Y_2O_3, HfO_2, and La_2O_3. The additional slow traps in the MOS capacitors with Y_2O_3, HfO_2, and La_2O_3 are attributable to any defects in the high-k films and/or the interfaces with GeO_x.

INDEX TERMS Slow trap density, Ge, MOS interfaces, plasma oxidation, ALD high-k films.

I. INTRODUCTION

Since the scaling of Si complementary metal–oxide–semiconductor (CMOS) has been approaching the physical limit year by year, a Ge channel with higher electron and hole mobility than Si can be a replacement suitable for enhancement of higher performance CMOS with low power supply voltage [1]. Here, one of the critical challenges for fabrication Ge-MOSFETs is to satisfy the requirements on Ge gate stacks such as thin equivalent oxide thickness (EOT), low interface state density (D_{it}), high channel mobility and superior long term reliability [2]–[11].

Al_2O_3/GeO_x/Ge and $HfO_2/Al_2O_3/GeO_x$/Ge structures fabricated by plasma post oxidation (PPO) have been reported as one of the realistic gate stacks with very thin EOT [12]–[15]. Here, electron cyclotron resonance (ECR) oxygen plasma has been employed to form the GeO_x/Ge interfacial layers through oxidizing the Ge interfaces through the Al_2O_3/Ge and HfO_2/Al_2O_3/Ge structures. The MOS gate stacks with 1-nm-thick or thinner EOT and low D_{it} of $\sim 10^{11}$ $eV^{-1}cm^{-2}$ have been obtained. However, a large amount of slow traps existing at the Ge MOS interfaces and resulting poor bias-temperature instability (BTI) characteristics have been becoming one of the most critical remaining issues for Ge CMOS realization [16]–[18].

In order to reduce the slow trap density, understanding of the physical origins of slow traps is indispensable. Recent studies have reported that the defects in Al_2O_3 [17]–[20] and Ge oxides [21]–[23] could be the physical origins of slow traps in Al_2O_3/GeO_x/Ge MOS structure. We recently examined the slow trap behaviors of ALD Al_2O_3/GeO_x/n- and p-Ge MOS interfaces with changing the thicknesses of Al_2O_3 and GeO_x [21], [23]. It has been found that the main slow traps of electrons, responsible for the hysteresis in the Al_2O_3/GeO_x/n-Ge interfaces, can locate near the GeO_x/Ge interfaces [21], while the main slow traps for holes, responsible for the hysteresis in the Al_2O_3/GeO_x/p-Ge interfaces, can locate near the Al_2O_3/GeO_x interfaces [23].

Also, we compared the slow trap density (ΔN_{st}) of ALD Al_2O_3/GeO_x/n- and p-Ge MOS formed by pre-oxidation of Ge and PPO. It has been found, as a result, that some amount of slow traps are additionally generated during the PPO process near conduction band side, suggesting that any reaction of Al_2O_3 and GeO_x and/or inter-diffusion of Al atoms in GeO_x interfacial layers can create slow traps during PPO [23]. These results mean that the formation of the GeO_x interfacial layers by pre-oxidation is more suitable with a same level D_{it} for high reliability Ge gate stacks than those formed by PPO. However, post Al_2O_3 ALD on GeO_x/Ge formed by plasma pre-oxidation is hard to continue the EOT scaling [24]–[28]. Thus, higher-k materials are needed to further scale the Al_2O_3/GeO_x/Ge gate stacks. However, the impact of different high-k materials on ΔN_{st} in the high-k/GeO_x/Ge MOS interfaces has not been examined yet.

In this study, we compare D_{it} and ΔN_{st} of the Y_2O_3, HfO_2 and La_2O_3/GeO_x/Ge interfaces prepared by high-k film post ALD on the plasma pre-oxidation GeO_x/Ge structures with those of the Al_2O_3/GeO_x/Ge ones, in order to evaluate the influence of the post ALD high-k films on interface traps of the GeO_x/Ge MOS structures with pre-oxidation. The process and structural parameters of the MOS structures with post ALD Al_2O_3, Y_2O_3, HfO_2 and La_2O_3 are systematically varied. Here, we focus on the location of slow traps in the high-k/GeO_x/Ge structures, as studied in Al_2O_3/GeO_x/Ge structures [23]. Also, we investigate the difference in the properties of interface traps and slow traps between n- and p-Ge MOS interfaces. In addition, the high k/GeO_x/Ge structures are analyzed by X-ray photoemission spectroscopy (XPS) in order to obtain the understanding of the physical origin of slow traps in the high-k/GeO_x/Ge gate stacks.

II. EXPERIMENTAL

Figure 1 shows the structure of fabricated Au/Al_2O_3, Y_2O_3, HfO_2 and La_2O_3/GeO_x/Ge gate stacks by plasma pre-oxidation, used in this study. Here, the amount of slow traps in these MOS interfaces is evaluated by changing post ALD high-k materials in order to study the effects of the different high-k materials on the slow trap properties. The thickness of Al_2O_3, Y_2O_3, HfO_2 or La_2O_3 was 10 nm. The thickness of GeO_x formed by plasma pre-oxidation, evaluated by ellipsometry, was 1.4 nm. The device fabrication flow is also shown in Fig. 1. First, n- and p-type (100) Ge wafers with a donor and acceptor concentration, respectively, of 10^{16} cm^{-3} were cleaned by de-ionized water, acetone and HF. After the pre-cleaning, plasma pre-oxidation was performed by using ECR plasma of Ar (9 sccm) and O_2 (3 sccm) at 300 °C under microwave power of 650 W. Here, the oxidation time was 10 s in order to form 1.4-nm-thick GeO_x. Subsequently, 10-nm-thick Al_2O_3, Y_2O_3, HfO_2, or La_2O_3 was deposited at 300 °C by a same ALD system. The precursors for ALD Al_2O_3, Y_2O_3, HfO_2, and La_2O_3 are $(CH_3)_3Al$, $(CpMe)_3Y$, $Hf(NEtMe)_4$ and $(C_3H_7C_5H_4)_3La$, respectively. Water was used as the oxidant. Post deposition annealing (PDA) was performed for 30 min at 400 °C in N_2 ambient, which is the same as the conditions verified by the previous works [29], [30], followed by the formation of 100-nm-thick Au gate electrodes and 100-nm-thick Al back contacts by thermal evaporation.

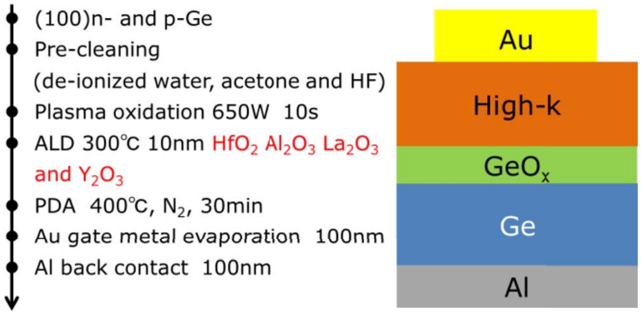

FIGURE 1. Process flow and structure of 10-nm-thick high-k/1.4-nm-thick GeO_x/Ge MOS interfaces.

D_{it} was evaluated by the conductance method. The slow trap density (ΔN_{st}) was evaluated from the hysteresis in the C-V sweep as a function of the effective oxide field (E_{ox}). Here, E_{ox} and ΔN_{st} were determined [18] by

$$E_{ox} = (V_G - V_{FB})/CET$$
$$q\Delta N_{st} = C_{ox}\Delta V_{hys}.$$

III. RESULTS AND DISCUSSION

Figure 2 shows the C-V curves of the 10-nm-thick Al_2O_3, Y_2O_3, HfO_2 and La_2O_3/1.4-nm-thick GeO_x/n- and p-Ge MOS capacitors with ECR plasma oxidation prior to ALD high-k films deposition. The C-V curve of Al_2O_3/GeO_x/n-Ge has larger flat band voltage (V_{fb}) shift than those of the other high-k materials, meaning that more negative charges are included in ALD Al_2O_3 films or the interfaces. It is observed, however, that the hysteresis of the Al_2O_3/GeO_x/n- or p-Ge MOS interfaces is significantly smaller than the HfO_2 and Y_2O_3 ones. Also, the La_2O_3/GeO_x/Ge MOS capacitors have the largest capacitance value among all of the capacitors, while also shows a very small hysteresis. This result suggests that La_2O_3 can be a good choice for the Ge gate stacks with low defect densities.

Here, accurate evaluation of D_{it} from C-V curves is not easy for Ge MOS interfaces at room temperature, because of the strong minority carrier response due to the narrow band gap of Ge [31]. So, we used the low temperature conductance method. Here, temperature was varied from 180 K to 250 K. Also, surface potential fluctuation (σ_s) was taken into account by the equation, $D_{it}=\left(\frac{G_p}{\omega}\right)_{f_p} f_D(\sigma_s)$ for evaluating D_{it}. [32] Figure 3 shows the energy

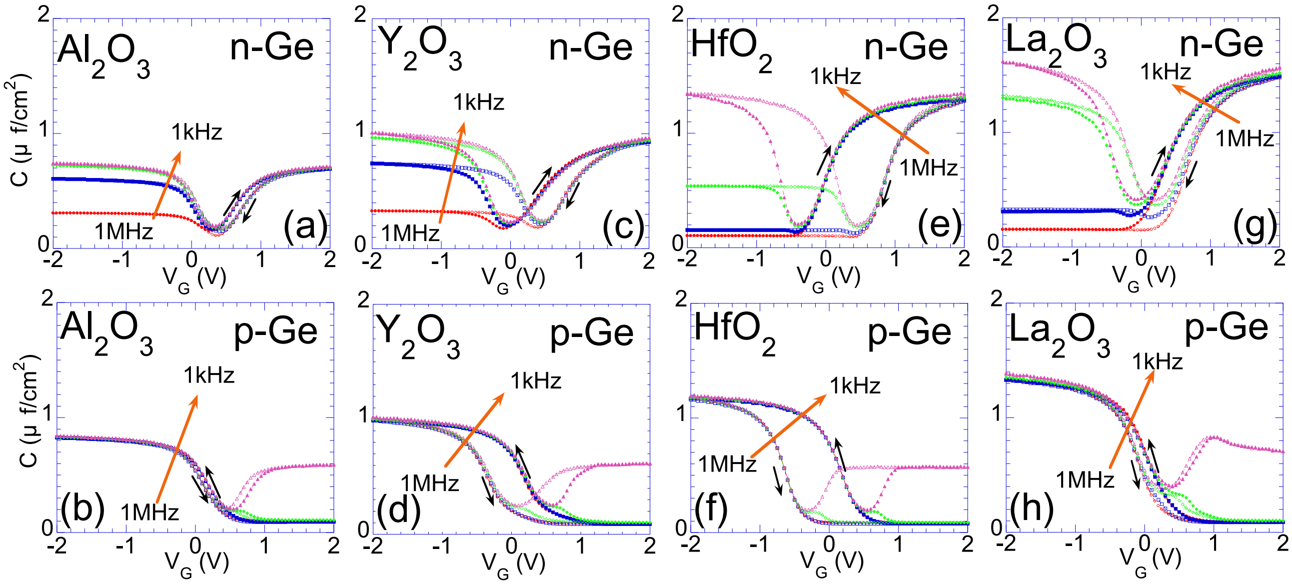

FIGURE 2. C-V curses of 10-nm-thick Al_2O_3, Y_2O_3, HfO_2 and La_2O_3/1.4-nm-thick GeO_x/Ge gate stacks with plasma pre-oxidation.

distributions of D_{it} of (a) the 10-nm-thick Al_2O_3, Y_2O_3, HfO_2 and La_2O_3/1.4-nm-thick GeO_x/n-Ge MOS interfaces and (b) p-Ge MOS interfaces with plasma pre-oxidation. The variation of D_{it} with changing the ALD high-k materials is very small. It is found that $D_{it}$is almost in a similar range from 1×10^{11} to 1×10^{12} $eV^{-1}cm^{-2}$ for both the n- and p- Ge MOS interfaces, though HfO_2 has slightly higher D_{it}. This result indicates the effectiveness of 1.4-nm-thick GeO_x/Ge interfaces formed by plasma pre-oxidation against the D_{it} increase associated with the high-k films ALD.

Figure 4 shows ΔN_{st} of the 10-nm-thick Al_2O_3, Y_2O_3, HfO_2 and La_2O_3 /1.4-nm-thick GeO_x/Ge MOS interfaces with plasma pre-oxidation as a function of E_{ox}. Here, the values of the voltage acceleration factor (γ), determined by equation $\Delta N_{st} \sim kE_{ox}^{\gamma}$ [18], are also show in Fig. 4. It is found that ΔN_{st} of the Al_2O_3/GeO_x/n- or p-Ge MOS interfaces is significantly lower than those of the MOS interfaces with the other high-k films. These results clearly show that the ALD Y_2O_3, HfO_2 and La_2O_3 films introduce additional slow traps in the high-k/GeO_x/Ge gate stacks in comparison with Al_2O_3. There can be three possible physical origins of the additional slow traps; (1) slow traps inside high-k films (2) high-k/GeO_x interface traps and (3) trap generation inside GeO_x. Actually, high-k/GeO_x interface traps and new traps inside GeO_x can be created by any chemical reaction at the high-k/GeO_x interfaces, and intermixing or diffusion of high-k species. It can be concluded, as a result, that the Al_2O_3/GeO_x/Ge interfaces have the weaker reaction and inter-diffusion at the Al_2O_3/GeO_x interfaces as well as the lower slow trap density inside Al_2O_3 than the interfaces with the other high-k materials.

On the other hand, ΔN_{st} of the La_2O_3/GeO_x/Ge structure has the different E_{ox} dependence from the other structures. Here, ΔN_{st} does not increase or even decreases with increasing E_{ox}, resulting in the smaller hysteresis in higher E_{ox}.

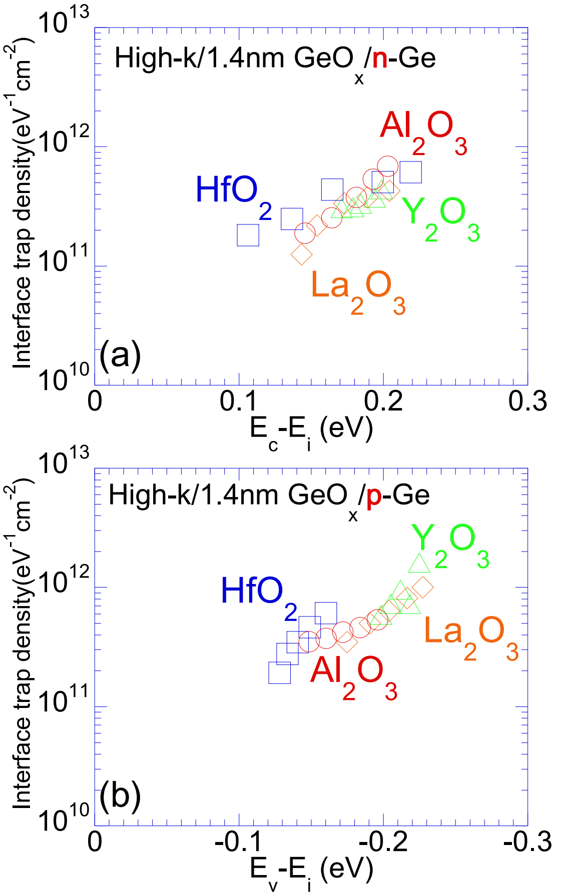

FIGURE 3. Relationship between energy and D_{it} of (a) 10-nm-thick Al_2O_3, Y_2O_3, HfO_2 and La_2O_3/1.4-nm-thick GeO_x/n-Ge and (b) p-Ge with plasma pre-oxidation.

This behavior is attributable to the decrease in V_{fb} with increasing the positive gate bias, suggesting the existence of the ferroelectric nature or any positive ion drift. The similar

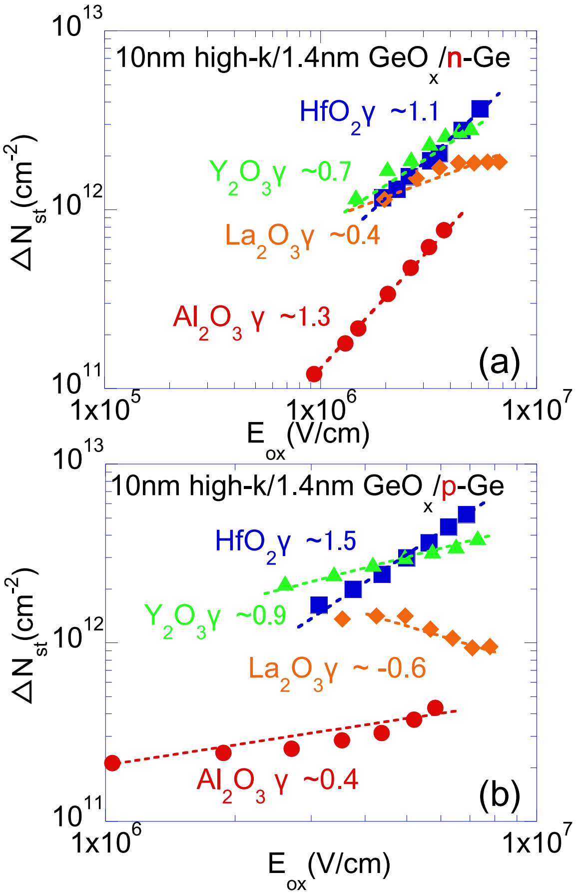

FIGURE 4. Relationship between E_{ox} and ΔN_{st} of (a) 10-nm-thick Al_2O_3, Y_2O_3, HfO_2 and La_2O_3/1.4-nm-thick GeO_x/n-Ge and (b) p-Ge with plasma pre-oxidation.

properties have already been reported in La_2O_3/InGaAs gate stacks [33], [34].

In order to examine the physical origins of the increase in the slow trap density in high-k/GeO_x/Ge interfaces, we measured the Ge 3d XPS spectra for the 1-nm-thick Al_2O_3, Y_2O_3, HfO_2 and La_2O_3/1.4-nm-thick GeO_x/Ge structures with plasma pre-oxidation. The results are shown in Fig. 5. We can observe peaks around a binding energy higher by ~3 eV from that of the Ge^0 peak, attributed to Ge oxides, for all the ALD high-k films. These peak energies and the peak shape are quite similar to that of the Al_2O_3/GeO_x/Ge structure, suggesting that ALD Y_2O_3, HfO_2 and La_2O_3 films have no significant influence on the structures of the GeO_x interfacial layers through the diffusion and/or reactions of Y, Hf and La atoms incorporated in the high-k films. In addition, it might be unlikely to consider that diffused high-k atoms newly create slow traps near the GeO_x/Ge interfaces, because the D_{it} values has almost no change among the Al_2O_3, Y_2O_3, HfO_2 and La_2O_3/GeO_x/Ge MOS interfaces, as shown in Fig. 3.

As a result, the additional increase in ΔN_{st} in the Y_2O_3, HfO_2 and La_2O_3/GeO_x/Ge MOS interfaces are attributable to the contribution of slow traps included in the ALD high-k materials and/or high-k/GeO_x interfaces.

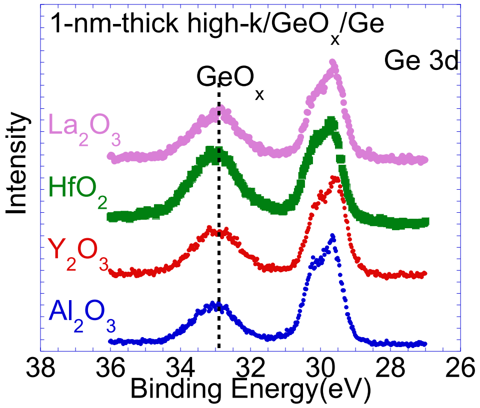

FIGURE 5. Ge 3d XPS spectra of 1-nm-thick Al_2O_3, Y_2O_3, HfO_2 and La_2O_3/1.4-nm-thick GeO_x/Ge interfaces with plasma pre-oxidation.

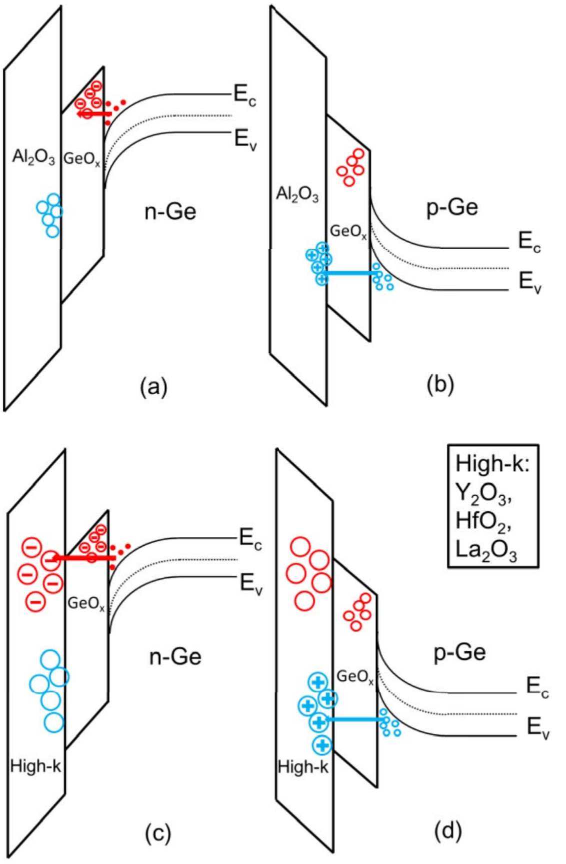

FIGURE 6. Schematic diagram of possible positions of slow traps of (a) Al_2O_3/GeO_x/n-Ge and (b) p-Ge (c) Y_2O_3, HfO_2 or La_2O_3/GeO_x/n-Ge and (d) p-Ge MOS interfaces by plasma pre-oxidation. The positions of slow traps of (a) Al_2O_3/GeO_x/n-Ge and (b) p-Ge have been reported in reference [23].

Finally, we summarize a schematic diagram of possible locations of slow traps in the Al_2O_3/GeO_x/n- and p-Ge MOS interfaces and Y_2O_3, HfO_2 and La_2O_3/GeO_x/n- and p-Ge MOS interfaces with plasma pre-oxidation, as shown in Fig. 6. The slow traps for electrons can locate near the GeO_x/Ge MOS interfaces, which has been previously clarified by evaluating ΔN_{st} in the Al_2O_3/GeO_x/n-Ge MOS capacitors and n-MOSFETs with the different thickness of Al_2O_3 and GeO_x [21], as shown in Fig. 6(a). On the other hand, the slow traps for holes in Al_2O_3/GeO_x/Ge MOS interfaces can locate around the Al_2O_3/GeO_x interface, shown in Fig. 6(b) [23]. In addition, the experimental findings of the larger slow trap density in Y_2O_3, HfO_2 and La_2O_3/GeO_x/n- and p-Ge MOS interfaces and no change in the Ge 3d XPS signal suggest that much larger amounts of additional slow traps for both electrons and holes can locate near the interfaces of GeO_x with ALD Y_2O_3, HfO_2 and La_2O_3, probably inside the high-k films, as shown in Fig. 6(c) and (d). As a result, particularly in the high-k/GeO_x/n-Ge MOS interfaces, the main slow trap position for electrons can change from the GeO_x/Ge interfaces to the high-k/GeO_x interfaces or inside the high-k films by replacing the high-k materials from Al_2O_3 to Y_2O_3, HfO_2 and La_2O_3. It has not been clear yet, however, whether the physical origins of the additional slow traps can be due to any defects in high-k films or defect states specific to the high-k/GeO_x interfaces. Further studies are needed to identify the detailed picture of the responsible trap states.

IV. CONCLUSION

We have investigated the slow trap density in ALD Al_2O_3, Y_2O_3, HfO_2 and La_2O_3/GeO_x/n- and p-Ge MOS interfaces with pre-oxidation by ECR plasma. It was found, as a consequence, that the Y_2O_3, HfO_2 and La_2O_3/GeO_x/n- and p-Ge MOS interfaces include much larger amounts of slow traps for both electrons and holes than the Al_2O_3/GeO_x/n- and p-Ge MOS interfaces, while D_{it} has almost similar values of as low as 1×10^{11} to 1×10^{12} $eV^{-1}cm^{-2}$ among the four interfaces. The XPS results have also shown no significant difference in the GeO_x interfacial layer structures among the Y_2O_3, HfO_2 and La_2O_3/GeO_x/Ge MOS interfaces. As a result, the higher density of slow trap for electrons and holes in the Y_2O_3, HfO_2 and La_2O_3/GeO_x/Ge MOS interfaces is attributable to any defects in the ALD Y_2O_3, HfO_2 and La_2O_3 films and/or at the interfaces with GeO_x near the conduction and valence band edge of Ge.

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