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Suppression of Punch-Through Current in 3 kV 4H-SiC Reverse-Blocking MOSFET by Using Highly Doped Drift Layer

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ABSTRACT Low on-resistance 4H-SiC reverse-blocking (RB) metal–oxide–semiconductor field-effect transistors (MOSFETs) have been developed by adopting a non-punch-through (NPT) drift layer in order to suppress the punch-through (PT) current under the reverse-blocking condition. The n-type NPT drift layer was 40-μm thick doped to 3.7×10^{15} cm^{-3}. The forward and reverse breakdown voltages of the fabricated NPT RB MOSFET were 3.6 kV and −3.0 kV, respectively. The differential specific on-resistance was 13.5 mΩ·cm^2 at room temperature, which was 33% lower than that of a 3 kV PT RB MOSFET, demonstrating superiority of the developed NPT RB MOSFET as a high-performance bidirectional switch.

INDEX TERMS Silicon carbide (SiC), reverse-blocking capability, non-punch-through (NPT) design, Schottky contact, metal-oxide-semiconductor field-effect transistor (MOSFET).

I. INTRODUCTION

Bidirectional switches are attractive building blocks, adopted in a lot of power-conversion circuits such as matrix converters, neutral-point-clamped multilevel inverters, and current-source inverters [1], [2]. In medium- or high-voltage applications over 600 V, the configurations by silicon (Si) insulated-gate bipolar transistors (IGBTs) and reverse-blocking (RB) IGBTs are usually employed [3]–[5]. On the other hand, silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) are promising as high-performance switching devices thanks to the superior material properties [6]–[8], and have been also used as a high-performance bidirectional switch by the anti-series connection of the two devices [9].

The authors have fabricated a 4H-SiC RB MOSFETs by embedding a Schottky barrier diode (SBD) on the backside and demonstrated superior performance as a 3-kV-class bidirectional switch [10], [11]. The bidirectional switch configured by the anti-parallel connection with the RB MOSFETs exhibited lower on-state loss than the standard MOSFETs configuration. This developed RB MOSFET had a punch-through (PT) drift layer, which is widely adopted in the standard SiC MOSFET. However, the performance of the PT RB MOSFET was degraded by the PT current because high voltage is applied to not only forward but also reverse directions. In this paper, the authors newly developed a 4H-SiC RB MOSFET adopted a non-punch-through (NPT) drift layer to suppress the PT current under reverse-blocking condition and achieved lower on-resistance than the PT RB MOSFET, keeping almost the same reverse-blocking voltage.

II. DEVICE DESIGN AND FABRICATION

The schematic cross section of the developed NPT RB MOSFET is shown in Fig. 1. The structural difference between the NPT RB MOSFET and the comparative PT RB MOSFET [11] are summarized in Table 1. These RB MOSFETs have almost the same thickness of the drift layer, about 40 μm. The doping concentration of the n$^-$-drift layer in the NPT RB MOSFET was 3.7×10^{15} cm^{-3}, which was 1.8-times higher than that of the PT RB MOSFET. The MOSFET cell designs were exactly the same in both the devices. Fig. 2 shows electric-field profiles calculated for the NPT and PT RB MOSFETs under ideal reverse-breakdown

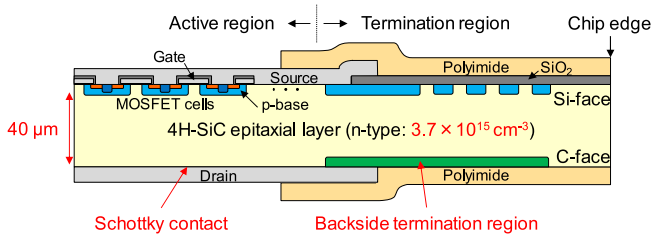

FIGURE 1. **Schematic cross section of the 4H-SiC non-punch-through reverse-blocking (RB) MOSFET.**

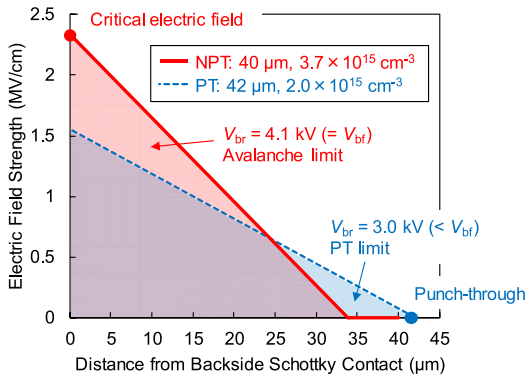

FIGURE 2. **Electric-field profiles in the NPT and PT RB MOSFETs at ideal reverse breakdown condition. Calculated ideal reverse breakdown voltages (V_{br}) are also shown, compared with the ideal forward breakdown voltage (V_{bf}).**

condition. In the case of the PT RB MOSFET, the space-charge region extends from the backside Schottky contact to the top MOSFET cells. When the space-charge region reaches the p-base regions, the built-in potential between the p-base and n^--drift regions drops, causing poor breakdown by the PT current. In this case, maximum electric field in the SiC is lower than the theoretical critical electric field determining avalanche breakdown, and the reverse breakdown voltage of the PT RB MOSFET (3.0 kV) becomes lower than the ideal avalanche breakdown voltage (5.8 kV). On the other hand, the NPT RB MOSFET shows avalanche-limited breakdown, keeping high blocking voltage, because the space charge region does not reach the p-base regions under avalanche-breakdown condition. The ideal reverse breakdown voltage of the NPT RB MOSFET is 4.1 kV, which is higher than 3.0 kV in the PT RB MOSFET. Therefore, the NPT RB MOSFET can improve the trade-off relationship between the breakdown voltage and the on-state resistance, owing to higher doping concentration than that of the PT RB MOSFET. In the NPT RB MOSFET, electric field strength near the backside Schottky contact becomes higher than that in the PT RB MOSFET under reverse bias condition. Thus, nickel (Ni) was adopted as a backside Schottky metal for the NPT RB MOSFET, which has higher barrier height for n-type SiC than titanium (Ti) adopted in the PT RB MOSFET [12], in order to suppress reverse leakage current caused by the higher electric field.

TABLE 1. **Structural difference between the SiC non-punch-through (NPT) and punch-through (PT) RB MOSFETs.**

Parameter	NPT (this work)	PT [11]
SiC thickness	40 µm	42 µm
drift doping	3.7×10^{15} cm^{-3}	2.0×10^{15} cm^{-3}
Schottky metal	Ni	Ti

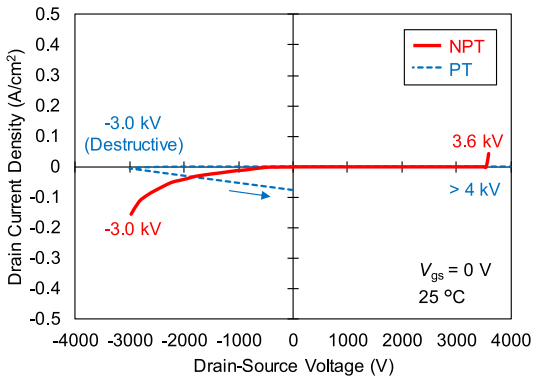

FIGURE 3. **Bidirectional blocking characteristics of the SiC NPT and PT RB MOSFETs.**

The fabrication process of a SiC NPT RB MOSFET is as follows. First, a conventional SiC double-implanted MOSFET (DMOSFET) was fabricated on the Si-face of the 50-µm-thick n^--epitaxial layer grown on a n^+-substrate. The entire region of the n^+-substrate was removed by mechanical grinding and chemo-mechanical polishing from the C-face. During the back-grinding process, the fabricated SiC DMOSFET wafer was fixed on a thick supporting wafer to prevent any cracks. The best SiC thickness in the NPT RB MOSFET is 34 µm to maximize the trade-off performance between on-resistance and reverse-blocking voltage (Fig. 2). In this work, the target SiC thickness was set to 40 µm to minimize the influence of the inevitable thickness fluctuation to breakdown voltage by the back-grind process. On the polished surface, a termination structure was formed by acceptor-type ion implantation through the photoresist patterns and a Schottky electrode was deposited, and activation annealing after the implantation was performed. However, the activation rate was not so high, because the annealing temperature was lower than the standard temperature (> 1500 °C) to protect the front-side structures. Finally, polyimide was coated around the drain-metal periphery to prevent discharge at the chip edge. All the backside patterns were formed by photolithography from the back surface, aligned to the front-side patterns through the SiC n^--epitaxial layer. The chip size and the active area of the fabricated NPT RB MOSFET were 1.8 mm × 1.8 mm and 1.15 mm^2, respectively. The fabricated RB MOSFET chips were assembled in TO-247 packages.

III. RESULTS AND DISCUSSION

Fig. 3 shows the bidirectional blocking characteristics of the fabricated NPT RB MOSFET and the comparative PT RB

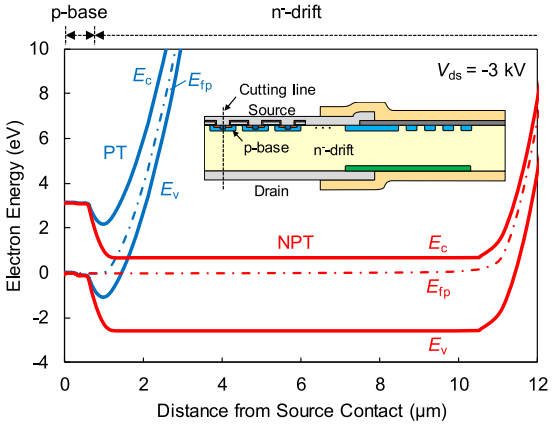

FIGURE 4. Band diagrams of the NPT and PT RB MOSFETs near the p-base region at $V_{ds} = -3$ kV (E_c/E_v: the conduction/valence bands, E_{fp}: the quasi-Fermi level for holes). The zero level of energy means the Fermi level under the equilibrium condition.

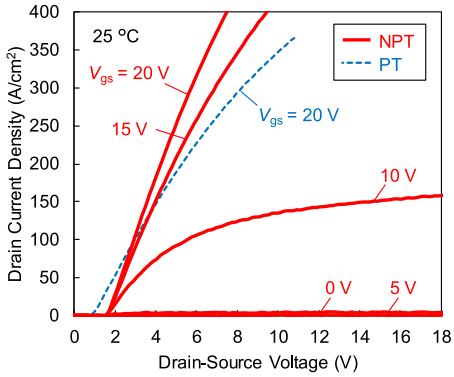

FIGURE 5. Forward $I_d - V_{ds}$ characteristics of the NPT RB MOSFET. Those of the PT RB MOSFET ($V_{gs} = 20$ V) are shown for comparison (dashed line).

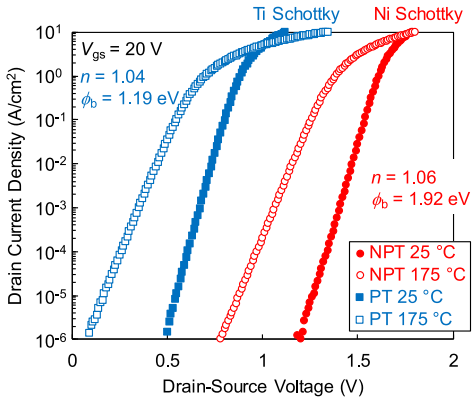

FIGURE 6. Forward Schottky characteristics of the NPT (Ni) and PT (Ti) RB MOSFETs ($V_{gs} = 20$ V).

MOSFET when gate-source voltage (V_{gs}) equals 0 V. The applied maximum drain-source voltage was set to ±4 kV in order to eliminate the influence of discharge in the package or the measurement system. Both the RB MOSFETs exhibited the same reverse-blocking voltage of −3.0 kV. However, destructive breakdown was observed only in the PT RB MOSFET, while the NPT RB MOSFET was not destructed in repetitive sweeps. To confirm the difference of the reverse-breakdown mechanism, band diagrams along the vertical direction near the p-base regions in these RB MOSFETs at −3.0 kV were simulated by TCAD (Fig. 4). In the PT RB MOSFET, the potential barrier for holes is degraded by the PT and holes are injected to the n^--drift layer, triggering the PT current. This PT current causes a drastic change of the electric field distribution and destructive breakdown. In the NPT RB MOSFET, the potential barrier near the pn junction between the p-base and n-drift regions remains unchanged under high reverse-bias condition, suppressing the PT current. The measured reverse breakdown voltage of the NPT RB MOSFET (3.0 kV) was 73% of the ideal value (4.1 kV), limited by the high reverse leakage current. The higher reverse leakage current in the NPT RB MOSFET than that in the PT RB MOSFET was due to the higher electric field applied to the reverse-blocking Schottky diode embedded on the backside (2.0 MV/cm at −3 kV). This leakage current can be suppressed by the introduction of a junction barrier Schottky structure onto the backside in the next step. In the case of the forward-blocking condition, the blocking voltages of the NPT and PT RB MOSFETs were 3.6 kV and more than 4 kV, respectively, and no PT current (no hole injection) was observed in both the NPT and PT RB MOSFETs, because the pn junction in the DMOSFET cells efficiently blocks carrier transport even if the backside Schottky barrier disappears by the extension of the space-charge region from the top cell structure. Therefore, the forward blocking in the PT RB MOSFET is also determined by avalanche, and the forward blocking voltage of the PT RB MOSFET becomes higher than that of the NPT RB MOSFET.

Fig. 5 depicts the forward output characteristics of the NPT RB MOSFET at room temperature. The threshold voltage was 2.6 V defined at the drain current density of 0.04 A/cm^2 and the junction voltage drop caused by the backside Schottky barrier was 1.8 V. For comparison, the on-state characteristics of the PT RB MOSFET are also plotted in Fig. 5 as dashed lines. In the low current region, the PT RB MOSFET has advantage because of the lower junction voltage drop than that of the NPT RB MOSFET as discussed in the following section. On the other hand, the differential on-resistance of the NPT RB MOSFET was obviously lower thanks to the higher doping concentration.

To investigate the detail of the junction voltage drop in these RB MOSFETs, low-current Schottky characteristics of the NPT and PT RB MOSFETs at 25 and 175 °C were compared in Fig. 6. The calculated ideality factor and the Schottky barrier height of the NPT RB MOSFET were 1.06 and 1.92 eV, respectively, which were almost the same as the values reported in Ni/4H-SiC SBD fabricated on a C-face [12]. The Schottky barrier height of the NPT RB MOSFET was higher than that of the PT RB MOSFET (Ti: 1.19 eV), which caused higher junction voltage drop and the

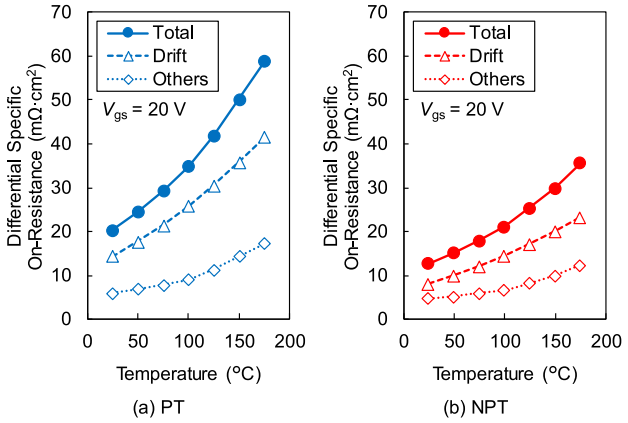

FIGURE 7. Temperature dependence of the differential specific on-resistance in the (a) PT and (b) NPT RB MOSFETs.

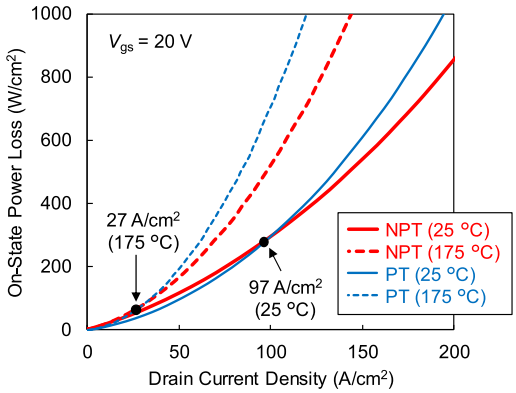

FIGURE 8. On-state power losses of the NPT and PT RB MOSFETs versus drain current density at 25 and 175 °C.

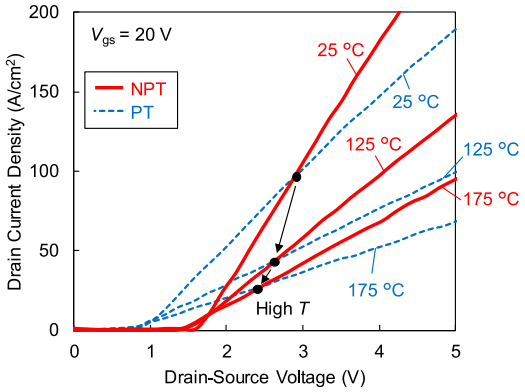

FIGURE 9. Temperature dependence of the on-state output characteristics in the NPT and PT RB MOSFET.

higher on-state loss in the NPT RB MOSFET at low current operation.

The temperature dependence (25–175 °C) of the differential specific on-resistance in the NPT and PT RB MOSFETs measured at V_{gs} = 20 V (electric field in the gate oxide: 3.8 MV/cm) is shown in Fig. 7. The drift-layer resistance was calculated by the doping concentration and the thickness of the n^--drift layer [13]. This drift-layer resistance of the NPT RB MOSFET was lower in the measured temperature range than that of the PT RB MOSFET, directly reflecting the 1.8-times higher doping concentration. The other resistances were mostly occupied by the junction field-effect transistor (JFET) resistance. Although the DMOSFET cell structures were the same in both the RB MOSFET, the JFET resistance of the NPT RB MOSFET was also lower than that of the PT RB MOSFET thanks to the highly doped n-type layer. Therefore, the total differential on-resistance of the NPT RB MOSFET was 33–39% lower than that of the PT RB MOSFET in the commonly used temperature (25–175 °C). The drift-layer resistance indicated the strong temperature dependence due to the degradation of phonon-limited mobility, dominating the total on-resistance. While the JFET resistance is affected by not only the mobility degradation but also the change of the JFET width by the temperature dependence of the built-in potential between p-base and n-type JFET regions, positive temperature coefficient was also shown in measured temperature range. As a result, the total resistance of the NPT RB MOSFET at 175 °C (35.7 mΩ·cm^2) was about 2.6-times higher than that at 25 °C (13.5 mΩ·cm^2).

Finally, the on-state power losses of the NPT and PT RB MOSFETs were estimated from the forward output characteristics, as shown in Fig. 8. The off-state power loss of the NPT RB MOSFET at room temperature was 33 W/cm^2 at 1.5 kV calculated from Fig. 3 and can be ignored in a useful operation as a 3-kV-class bidirectional switch, compared with the on-state loss. In high current operation ($>$ 97 A/cm^2 at 25 °C), the on-state loss of the NPT RB MOSFET was lower than that of the PT RB MOSFET, because of the lower differential on-resistance. On the other hand, in low current operation ($<$ 97 A/cm^2 at 25 °C), the junction voltage drop dominantly affects the on-state power loss and the NPT RB MOSFET with higher junction voltage drop indicated higher on-state loss. Fig. 9 shows the temperature dependence of the on-state output characteristics of the NPT and PT RB MOSFETs. At higher temperature, the cross point of the drain current-voltage characteristics between the two devices was shifted to lower voltage and lower current direction due to the reduction of junction voltage drop. At 175 °C, the operation area, in which the NPT RB MOSFET has advantage, expands to the region over 27 A/cm^2. Therefore, the developed NPT RB MOSFET can efficiently reduce on-state loss in high-current or high-temperature operation, compared with the PT RB MOSFET.

IV. CONCLUSION

The authors have developed a low on-resistance 4H-SiC RB MOSFET and evaluated the electric characteristics. To suppress punch-through current and reduce on-resistance, a NPT-type drift layer was adopted, which possessed 1.8-times higher doping concentration than that of the previously developed PT RB MOSFET. The forward- and reverse-blocking voltages of the fabricated

NPT RB MOSFET were 3.6 kV and −3.0 kV, indicating the 3-kV-class bidirectional blocking capability. The differential on-resistances were 33–39% lower than those of the comparative PT RB MOSFET, demonstrating that the NPT RB MOSFET is suitable for the component of a highly efficient bidirectional switch.

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