

Received 18 December 2017; revised 3 March 2018; accepted 3 March 2018. Date of publication 14 March 2018;
date of current version 26 March 2018. The review of this paper was arranged by Editor M. Chan.

Digital Object Identifier 10.1109/JEDS.2018.2815703

Compensated Synaptic Device for Improved Recognition Accuracy of Neuromorphic System

CHULJUN LEE, SANG-MO KOO, JONG-MIN OH, AND DAESEOK LEE[✉]

Department of Electronic Materials Engineering, Kwangwoon University, Seoul 01897, South Korea

CORRESPONDING AUTHOR: D. LEE (e-mail: leeds@kw.ac.kr)

This work was supported in part by the National Research Foundation of Korea grant funded by the Korea Government (Ministry of Science, ICT and Future Planning) under Grant 2017R1C1B5075540, in part by the Research Grant of Kwangwoon University in 2018, and in part by the High Level Track of Power Semiconductor Technology for Renewable Energy and Electrical Vehicle of the Korea Institute of Energy Technology Evaluation and Planning under Grant 20174010201290.

ABSTRACT To improve a pattern recognition accuracy of synaptic device-based neuromorphic system, we tried to obtain symmetric conductance changes between conductance increase process (potentiation) and conductance decrease process (depression). By utilizing compensational voltage division, we achieved more gradual conductance changes during the depression, which led to the symmetric conductance changes between the potentiation and depression. On the basis of the achieved symmetric conductance changes, obviously improved pattern recognition accuracy was obtained on a multilayer perceptron structural simulation.

INDEX TERMS Synaptic device, pattern recognition, neuromorphic system, resistive random access memory.

I. INTRODUCTION

Recently, huge amount of imprecise data such as videos, sounds, and pictures has been generated. Because of its undefined structural data, it is hard to analyze by a typical von-Neumann architectural computing system. Therefore, a brain-inspired computing system (neuromorphic system) which can lead to energy efficient and error tolerant computations has been intensely investigated [1]–[3]. To realize the neuromorphic system, various approaches: von-Neumann architecture based neuromorphic system, CMOS based neuromorphic chip, and synaptic device based neuromorphic system (S-neuromorphic system) have been proposed. Among those approaches, the S-neuromorphic system is the most promising candidate on the basis of its various advantages in power, area, and time respects [4]–[10]. Although several types of the synaptic device such as resistive switching random access memory, phase change memory, ferroelectric switches, and field-effect-transistor based devices have been proposed for the S-neuromorphic system, a more practical synaptic devices are still necessary [4], [11]. Thus, in this research, we developed a $\text{Pr}_{0.7}\text{Ca}_{0.3}\text{MnO}_3$ (PCMO) based synaptic device (PCMO-synapse) to satisfy the requirements of synaptic device: low power consumption, bidirectional and symmetric weight changes, multi-level

states, scalability, endurance, and data retention. Among these requirements, especially, we focused on the symmetric weight changes that can lead to degradation of the S-neuromorphic accuracy [10], [11], [14].

II. EXPERIMENTAL PROCEDURE

To evaluate the influence of device characteristic on the pattern recognition accuracy, we firstly fabricated the PCMO-synapse, then its synaptic characteristics were simulated by the self-constructed S-neuromorphic system. For a pattern recognition test, we utilized the MNIST handwritten number data set [12]. As the PCMO-synapse, we fabricated a Pt/PCMO/N:TiN/Pt structural two-terminal synaptic device on a Si wafer including a thermally-grown SiO_2 layer, as shown in Figure 1(a). For the first step, we patterned and deposited Pt layer on the SiO_2 layer as bottom electrodes. Subsequently, we sputtered the PCMO layer at 620°C for better crystallization, then Si_3N_4 side wall was deposited and etched to form a via-hole structure with 500 nm diameter. We employed nitrogen doped TiN electrode (N:TiN) as a top electrode. To optimize conductance range of the PCMO-synapse, nitrogen concentration was controlled [13]–[15]. Finally, Pt layer was deposited on the N:TiN layer as a capping layer. Electrical measurements were conducted

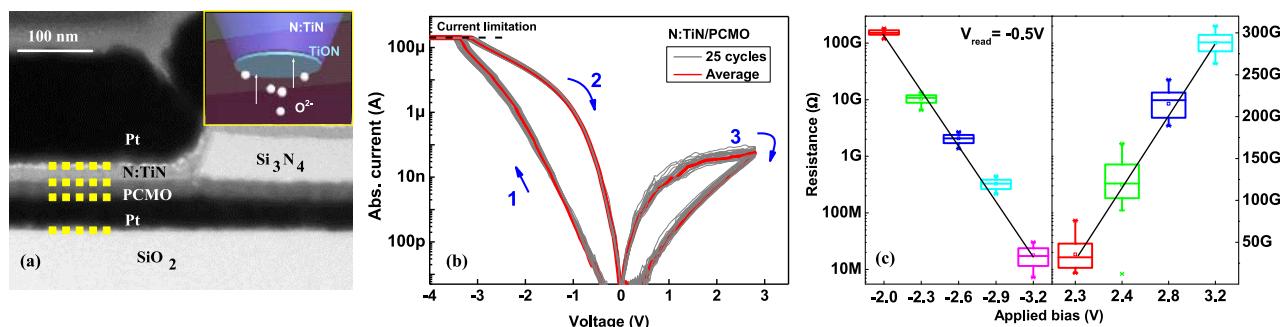


FIGURE 1. (a) The cross-sectional transmission electron microscope image of the fabricated PCMO-synapse. On the basis of a redox reaction between N:TiN layer and PCMO layer, resistance changes can be modulated, which is utilized as a conductance change of synaptic device (inset) [13]–[15]. (b) Quasi-static current-voltage (I-V) characteristics of the PCMO-synapse. The PCMO-synapse exhibited consistent gradual resistance changes. To prevent break-down of device, maximum current was limited during device operation. This bidirectional resistance change can be considered as a bidirectional conductance changes of the PCMO-synapse. (c) Bias controlled multi-level resistance states which can be utilized as the weight change of synaptic device.

by a typical semiconductor parameter analyzer: Agilent B1500 with the waveform generator/fast measurement unit.

III. RESULTS

In a quasi-static electrical measurement, the PCMO-synapse exhibited consistent and gradual resistance changes from high resistance to low resistance by negative bias, and from low resistance to high resistance by positive bias (figure 1(b)). These bidirectional and gradual resistance changes result from interfacial reaction between the N:TiN and PCMO layers, as shown in an inset of figure 1(a). When the positive bias was applied, in the PCMO layer, mobile oxygen ions are attracted to the N:TiN layer, then the oxygen ions react with the N:TiN layer. It results in a formation of induced metal oxide layer (TiON layer of the inset) at the interface between the PCMO and N:TiN layers. Therefore, the total resistance which is dependent on thickness of the induced metal oxide is increased [13], [14]. Sequentially, the induced metal oxide is dissolved under the applied negative bias, which leads to the total resistance change from high resistance to low resistance. On the basis of the reaction of N:TiN layer, we can obtain multi-level resistance states by modulating the thickness of induced oxide layer, as shown in figure 1(c). Under controlled quasi-static bias conditions, the PCMO-synapse exhibited clear multi-level resistance states. Even though the PCMO-synapse exhibited clear multi-level resistance states under the quasi-static bias conditions, for practical use as the synaptic device, it is necessary to confirm the multi-level resistance states under pulse bias conditions [10]–[12], [14].

In figure 2, the multi-level conductance states (which were derived from the multi-level resistance states) were achieved as the conductance increased and decreased per applied pulse bias number. It can be directly regarded as synaptic weight increase and decrease (potentiation and depression, respectively) for the S-neuromorphic system. For various applications of the S-neuromorphic system (especially the pattern recognition application), those potentiation and depression need to be symmetric to obtain higher recognition accuracy. In an ideal case, the potentiation and depression

are linear and fully symmetric [10]–[12], [14]. Although the PCMO-synapse exhibited bidirectional multi-level states and low power operation, it has exponentially increased potentiation and abruptly decreased depression (figure 2(a)). It can result in critical degradation of the recognition accuracy of the S-neuromorphic system. Thus, we defined Asymmetry ratio to compare a symmetry rate between the potentiation and depression at certain pulse number (N_x),

$$\text{Asymmetry ratio} = \frac{G_{\text{pot}(N_x)}}{G_{\text{dep}(N_{\max}-N_x)}} \quad (1)$$

when G_{pot} (G_{dep}) is conductance value during the potentiation (depression), and N_{\max} is a total applied pulse number for each process (figure 2(b)). In other words, the $G_{\text{pot}(N_x)}$ means conductance value during the potentiation at certain pulse number (N_x).

Comparing to the ideal case (blue dot-line in figure 2(b)), the PCMO-synapse has an incremental asymmetry ratio, which means that the PCMO-synapse exhibited worse asymmetric conductance changes when the conductance was higher. It is because the conductance was abruptly decreased during the depression. Considering the origin of the conductance changes (as described in figure 1(a)), the abrupt conductance decrease results from a rapid formation of the induced oxide at the interface between N:TiN and PCMO layers. Therefore, we need to sensitively control the progress of induced oxide formation to achieve the gradual depression, which can lead to symmetric conductance changes between the potentiation and depression.

To sensitively control the progress of induced oxide formation, during depression, we can apply smaller (larger) pulse bias for higher (smaller) conductance, which can lead to thinner (thicker) induced oxide layer. Based on the controlled thickness of induced oxide layer, gradual depression could be achieved. However, to apply modified pulse amplitude, more complex circuit and additional processes are required [10], [11], [16]. In other words, additional reading process (to confirm a current conductance) is necessary before applying each modified pulse. It will lead to not only more complexity in circuit level but also power consumption.

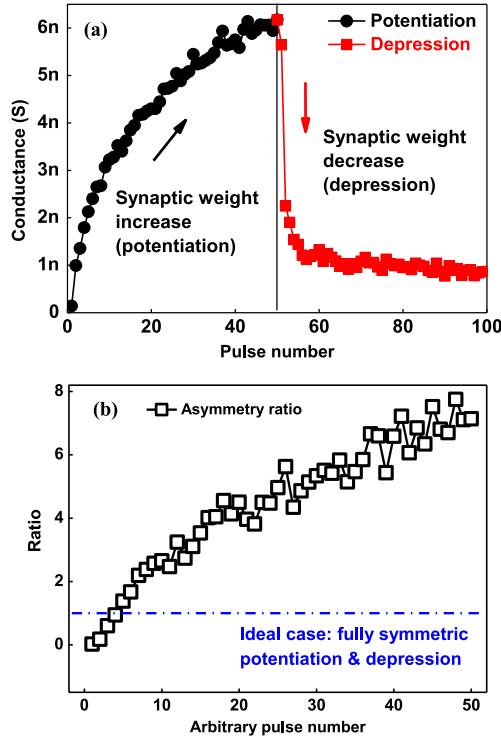


FIGURE 2. (a) Conductance increase (potentiation) and decrease (depression) of the PCMO-synapse. For the potentiation, negative identical pulse bias that has the same pulse amplitude as $-3V$ and pulse width as 1ms for all applied pulse numbers was utilized. Positive identical pulse bias ($+0.85V$, 1ms pulse) was used for the depression. (b) Asymmetry ratio between the potentiation and depression. For higher recognition accuracy of the S-neuromorphic system, at certain conductance values, similar conductance changes are necessary during the potentiation and depression. For the ideal synapse having fully symmetric conductance changes between the potentiation and depression, the asymmetry ratio is one.

Therefore, other efficient method is necessary to achieve more gradual depression under the identical pulse bias (which has the same pulse width and amplitude). To realize this, we utilized a fixed resistor (R_s , $\sim 500\text{ M}\Omega$) which is connected to the PCMO-synapse in series as a voltage divider. On the basis of voltage division equation, smaller bias can be applied on the PCMO-synapse when it has higher conductance, and vice versa. Under the identical pulse bias (V_{in}) condition, figure 3(a) shows effectively applied bias on the PCMO-synapse (V_{pcmo}) with various resistance ratio between the R_s and resistance of the PCMO-synapse (R_{pcmo}). The V_{pcmo} increased as the R_{pcmo} increased. It means that smaller bias can be applied when conductance of the PCMO-synapse is higher. For easier understanding, the V_{pcmo} is compared with the V_{in} in figure 3(b). Because the R_s plays a role of a voltage divider, for both cases: depression and potentiation, the V_{pcmo} can be modified. Thus, during the potentiation, the V_{pcmo} modified from high to small (decremental pulse) when conductance of the PCMO-synapse changes from low to high. In the same manner, the V_{pcmo} changes from small to high (incremental pulse) during the depression.

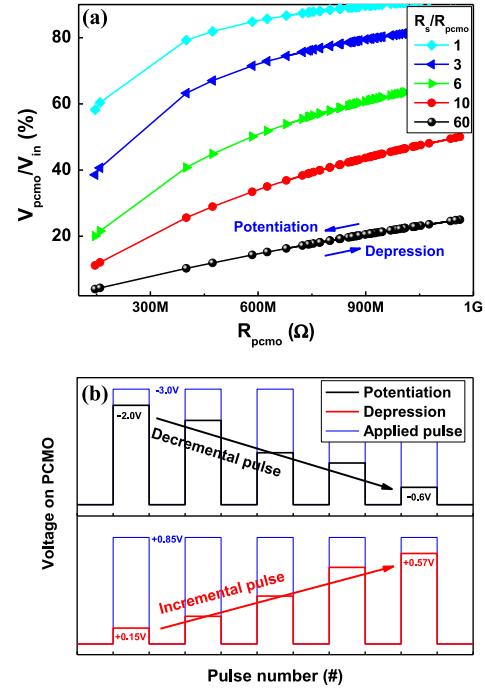


FIGURE 3. (a) Ratio between effectively applied bias on the PCMO-synapse (V_{pcmo}) and total applied bias (V_{in}). The ratio is dependent on resistance of the serial fixed resistor (R_s). On the basis of voltage division, the V_{pcmo} was changed from about 20 % to 67 % when the resistance ratio between the R_s and PCMO-synapse (R_{pcmo}) was 6 (green line with scatter). (b) Illustration of the V_{in} with the V_{pcmo} . During the potentiation, under applied fixed -3.0 V pulse amplitude (: identical pulse bias), effectively decremented pulse amplitude from -2.0 V to -0.5 V is applied on the PCMO-synapse as the R_{pcmo} changes. In the same manner, during the depression, incremented pulse amplitude from $+0.15\text{ V}$ to $+0.57\text{ V}$ is effectively applied under identical pulse bias ($+0.85\text{ V}$ pulse amplitude).

Figure 4(a) shows improved conductance changes by the R_s under the identical pulse bias described in figure 3(b). During the depression, we achieved more gradual conductance changes, which can lead to improved Asymmetry ratio (figure 4(b)). To clarify effects of the achieved symmetric conductance changes, we simulated synaptic characteristics of the PCMO-synapse by self-constructed MNIST handwritten data set based pattern recognition simulation [12]. For the pattern recognition, we utilized multilayer perceptron neural network with a backpropagation learning algorithm. Four layers (input, 1st hidden, 2nd hidden, and output layers) were employed, and each layer respectively consists of 528, 250, 125, and 10 neurons. The conductance changes of PCMO-synapse are defined as

$$G = \left(\left(G_{high}^\alpha - G_{low}^\alpha \right) \times w + G_{low}^\alpha \right)^{\frac{1}{\alpha}} \quad (2)$$

where G is conductance (G_{high} and G_{low} : higher and lower G , respectively), α is a parameter representing slope of the conductance changes, and w is cumulative synaptic weight. For this conductance model, we considered two PCMO-synapses as one synapse, which can express a negative conductance in the perceptron neural network. Moreover,

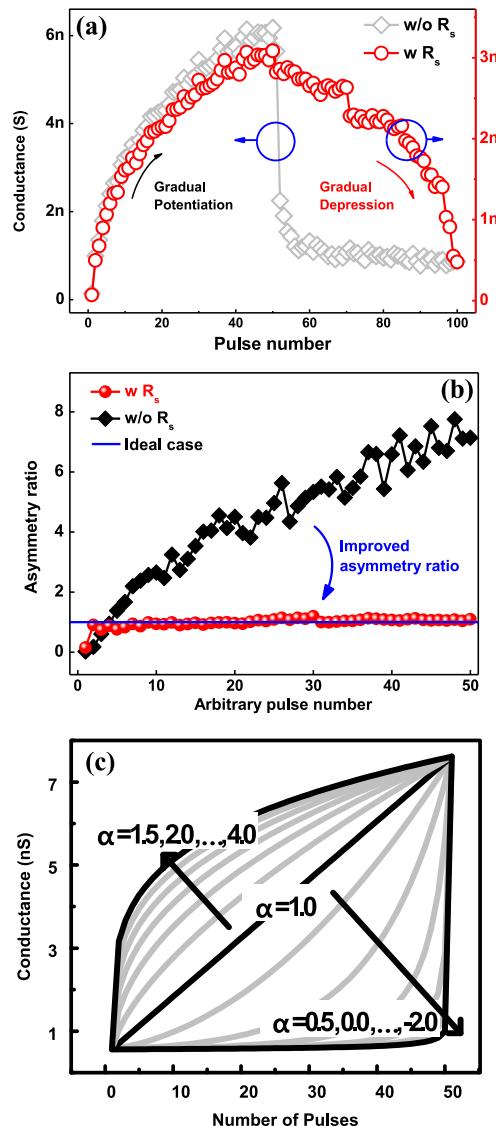


FIGURE 4. (a) Significantly improved conductance change of the PCMO-synapse. On the basis of the modulated V_{PCMO} ($w R_s$), the PCMO-synapse exhibited more symmetric conductance changes between the potentiation and depression than that of without R_s case ($w/o R_s$). (b) Comparison of the asymmetry ratio between the $w R_s$ and $w/o R_s$ cases. Improved asymmetry ratio which can lead to higher pattern recognition accuracy of the S-neuromorphic system was achieved. (c) The α values for various slopes of conductance changes.

we defined the w value from zero to one. When we applied operation pulses: potentiation or depression, the w is constantly increased or decreased [12]. As an input data, the original MNIST images (28 x 28 pixels) were cropped as 22 x 24 pixels. For reliable simulation results, randomly selected 1,000 training images were used for learning of the system while 10,000 images were utilized to test the system. More detail explanations about the simulation are described in reference [12], [14], [15].

The influence of α on conductance changes are shown in figure 4(c). For both potentiation and depression, the same conductance changes can be obtained when $\alpha = 1.0$.

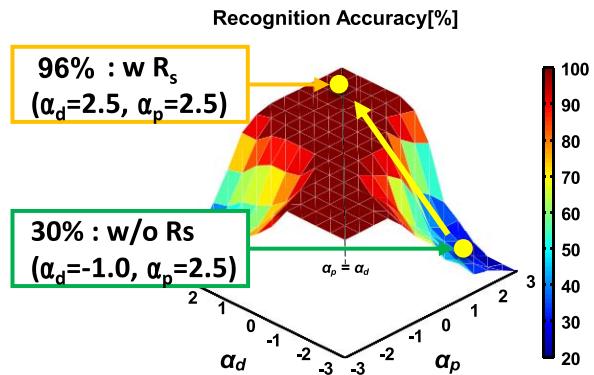


FIGURE 5. The α_d values (α during the depression) can be changed from -1.0 to -2.5 by the modulated V_{PCMO} resulted from the R_s . On the basis of the similar α values between the potentiation and depression, pattern recognition accuracy of the S-neuromorphic system was obviously improved from 30 % to 96 %.

(ideal case). However, because the pristine PCMO-synapse (without R_s) has respectively -1.0 (α_d) and 2.5 (α_p) for the depression and potentiation, the PCMO-synapse showed only about 30% recognition accuracy. Contrast to the pristine PCMO-synapse (without R_s), the PCMO-synapse exhibited about 96% recognition accuracy when it was compensated by the R_s . The α values were considered as $+2.5$ for both α_p and α_d on the basis of the results of figure 4. Consequently, the recognition accuracy was significantly improved from 30% to 96%, as shown in figure 5.

IV. CONCLUSION

Based on the PCMO-synapse, we successfully achieved significantly improved pattern recognition accuracy with the R_s . It resulted from compensated voltage drop on the PCMO-synapse. During the potentiation and depression, proper voltage was applied on the PCMO-synapse on the basis of resistance ratio between the R_s and PCMO-synapse. As a result, under the identical pulse bias, the compensated PCMO-synapse exhibited more symmetric conductance changes, which results in obviously improved recognition accuracy.

REFERENCES

- [1] D. B. Strukov, "Smart connections," *Nature*, vol. 476, no. 7361, pp. 403–405, 2011, doi: [10.1038/476403a](https://doi.org/10.1038/476403a).
- [2] G. V. Varatkar, S. Narayanan, N. R. Shanbhag, and D. L. Jones, "Stochastic networked computation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 10, pp. 1421–1432, Oct. 2010, doi: [10.1109/TVLSI.2009.2024673](https://doi.org/10.1109/TVLSI.2009.2024673).
- [3] K. K. Likharev, "CrossNets: Neuromorphic hybrid CMOS/nanoelectronic networks," *Sci. Adv. Mater.*, vol. 3, no. 3, pp. 322–331, 2011.
- [4] P. A. Merolla *et al.*, "A million spiking-neuron integrated circuit with a scalable communication network and interface," *Science*, vol. 345, no. 6197, pp. 668–673, 2014.
- [5] S. Park *et al.*, "RRAM-based synapse for neuromorphic system with pattern recognition function," in *Proc. Int. Electron Devices Meeting*, San Francisco, CA, USA, 2012, pp. 10.2.1–10.2.4.

- [6] S. Park *et al.*, "Self-formed Schottky barrier induced selector-less RRAM for cross-point memory applications," *Physica Status Solidi Rapid Res. Lett.*, vol. 6, no. 11, pp. 454–456, 2012, doi: [10.1002/pssr.201206382](https://doi.org/10.1002/pssr.201206382).
- [7] S. Park *et al.*, "Neuromorphic speech systems using advanced ReRAM-based synapse," in *Proc. IEEE Int. Electron Devices Meeting*, Washington, DC, USA, 2013, pp. 25.6.1–25.6.4.
- [8] S. Park *et al.*, "Nanoscale RRAM-based synaptic electronics: Toward a neuromorphic computing device," *Nanotechnology*, vol. 24, no. 38, 2013, Art. no. 384009.
- [9] S. Park *et al.*, "Electronic system with memristive synapses for pattern recognition," *Sci. Rep.*, vol. 5, May 2015, Art. no. 10123, doi: [10.1038/srep10123](https://doi.org/10.1038/srep10123).
- [10] G. W. Burr *et al.*, "Experimental demonstration and tolerancing of a large-scale neural network (165,000 synapses), using phase-change memory as the synaptic weight element," in *Proc. IEEE Int. Electron Devices Meeting*, San Francisco, CA, USA, 2014, pp. 29.5.1–29.5.4.
- [11] S. Yu, Y. Wu, R. Jeyasingh, D. Kuzum, and H.-S. Wong, "An electronic synapse device based on metal oxide resistive switching memory for neuromorphic computation," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2729–2737, Aug. 2011.
- [12] J.-W. Jang, S. Park, Y.-H. Jeong, and H. Hwang, "ReRAM-based synaptic device for neuromorphic computing," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Melbourne, VIC, Australia, 2014, pp. 1054–1057.
- [13] D. Lee, K. Moon, J. Park, S. Park, and H. Hwang, "Trade-off between number of conductance states and variability of conductance change in Pr_{0.7}Ca_{0.3}MnO₃-based synapse device," *Appl. Phys. Lett.*, vol. 106, no. 11, 2015, Art. no. 113701, doi: [10.1063/1.4915924](https://doi.org/10.1063/1.4915924).
- [14] D. Lee *et al.*, "Oxide based nanoscale analog synapse device for neural signal recognition system," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Washington, DC, USA, 2015, pp. 4.7.1–4.7.4.
- [15] K. Moon *et al.*, "High density neuromorphic system with Mo/Pr_{0.7}Ca_{0.3}MnO₃ synapse and NbO₂ IMT oscillator neuron," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Washington, DC, USA, 2015, pp. 17.6.1–17.6.4.
- [16] K. Duygu, Y. Shimeng, and W. H.-S. Philip, "Synaptic electronics: Materials, devices and applications," *Nanotechnology*, vol. 24, no. 38, 2013, Art. no. 382001.

CHULJUN LEE, photograph and biography not available at the time of publication.

SANG-MO KOO, photograph and biography not available at the time of publication.

JONG-MIN OH, photograph and biography not available at the time of publication.

DAESEOK LEE, photograph and biography not available at the time of publication.