Tunneling Transistors Based on MoS$_2$/MoTe$_2$ Van der Waals Heterostructures

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ABSTRACT 2-D transition metal dichalcogenides (TMDs) are promising materials for CMOS application due to their ultrathin channel with excellent electrostatic control. TMDs are especially well suited for tunneling field-effect transistors (TFETs) due to their low-dielectric constant and their promise of atomically sharp and self-passivated interfaces. Here, we experimentally demonstrate band-to-band tunneling (BTBT) in Van der Waals heterostructures formed by MoS$_2$ and MoTe$_2$. Density functional theory simulations of the band structure show our MoS$_2$-MoTe$_2$ heterojunctions have a staggered band alignment, which boosts BTBT compared to a homojunction configuration. Low-temperature measurements and electrostatic simulations provide understanding toward the role of Schottky contacts and the material thickness on device performance. Negative differential transconductance-based devices were also demonstrated using a different device architecture. This paper provides the prerequisites and challenges required to overcome at the contact region to achieve a steep subthreshold slope and high ON-currents with 2-D-based TFETs.

INDEX TERMS 2D materials, TMD, TFET, band-to-band tunneling, heterostructures, Schottky contacts.

I. INTRODUCTION

Tunnel FET's are a promising candidate for low-power logic applications, due to the reduced supply voltage enabled by a steep subthreshold slope less than 60mV/dec [4], [5]. There is increasing research interest in two dimensional TMD heterostructures based TFET's [6], [7], because the 2D layers of these materials are self-passivated and the interaction between layers are only through VdW forces. Therefore, 2D TFETs are expected to have a lower defect concentration and hence lower parasitic leakage current compared to their III-V counterparts [8].

Previous experimental works have been shown on 2D tunneling based devices exhibiting BTBT with different material stacks such as MoS$_2$/WSe$_2$ [9], [10], SnSe$_2$/WSe$_2$ [11], SnSe$_2$/BP. In another work, a steep-slope TFET with polymer electrolyte gating was realized using p-type Ge/MoS$_2$ 3D-2D VdW heterojunction [12]. Though these works have experimentally demonstrated BTBT, not much focus was

given to understanding the role of the Schottky barriers at the contacts and the recombination and generation currents on the device characteristics. And moreover, to understand the tunneling current operation with respect to the number of layers and gate electrostatics.

In this work, we address the issues mentioned above in the following sections. In Section II we calculate the band alignment using DFT and look at the impact of the number of layers, in Section III, we explain the fabrication steps of the two different device architectures along with some material characterizations performed. In Section IV, we discuss the results from temperature dependent electrical characterization and 1D electrostatic simulations and finally in Section V, we summarize the conclusions of our work. The TMD materials used to realize the TFET are Molybdenum disulfide (MoS$_2$) and Molybdenum ditelluride (MoTe$_2$). MoS$_2$ is the most widely studied 2D material after graphene and has shown to be an n-type semiconductor [1]
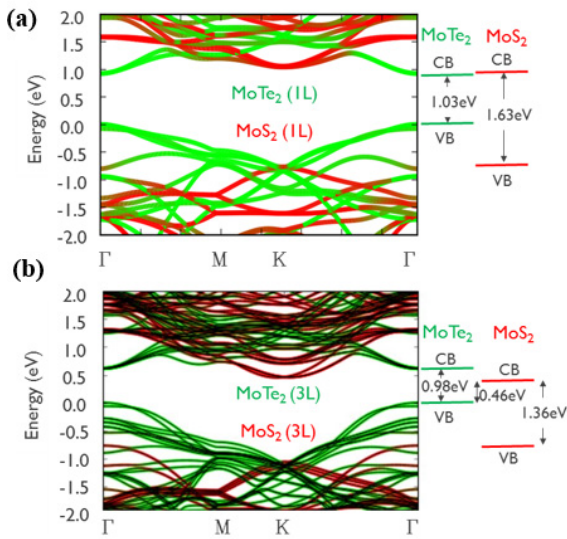
FIGURE 1. Band structure of overlapping MoS2-MoTe2 stack obtained using DFT simulations along with the band alignment and the bandgaps for (a) 1 + 1 layers and (b) 3 + 3 layers heterostack.
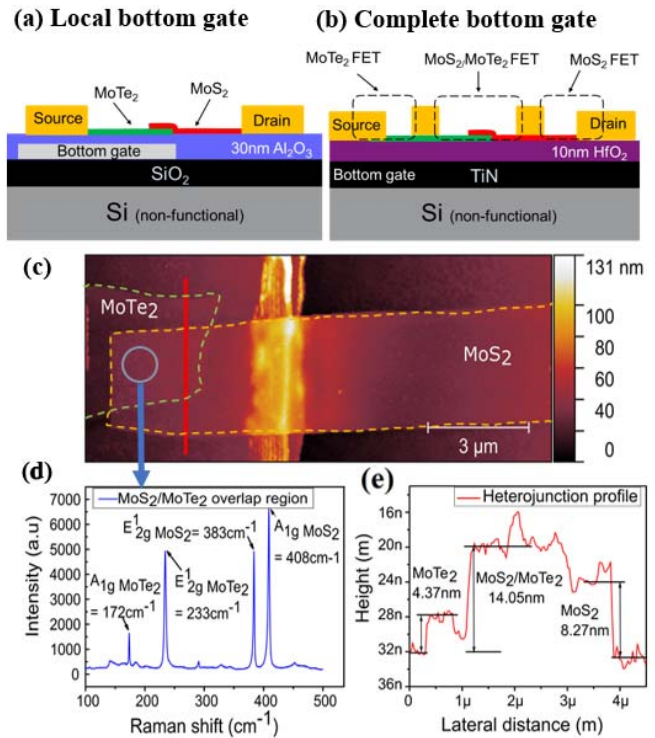

FIGURE 2. (a) Schematic cross-section of the local bottom gate and 2(b) complete bottom gate device architectures. (c) AFM showing the thickness of various parts of the heterostructure for the device with local bottom gate. (d) Raman spectra of the heterojunction depicting the characteristic peaks of MoS$_2$ and MoTe$_2$. (e) AFM height profile from the AFM on the MoTe$_2$, overlap region and MoS$_2$.

whereas MoTe$_2$ has shown to be ambipolar with a high p-type current [13], [14]. This material stack is chosen due to a staggered band alignment shown by the subsequent DFT simulations.

II. DFT SIMULATIONS

DFT simulations are performed to analyze the band alignment of the MoS$_2$/MoTe$_2$ stack (Fig. 1). We use the quantum espresso software package [15] with the Perdew-Burke-Ernzerhof exchange-correlation functional (PBE) [16] combined with project-augmented waves (PAW) pseudo potentials. Corrections for VdW forces introduced by Grimme *et al.* [17] are also included. The simulated stacks are firstly 1 layer MoS$_2$ + 1 layer MoTe$_2$ and secondly 3 layers MoS$_2$ + 3 layers MoTe$_2$. These two different stacks are chosen to understand the effect of the thickness of the layers on the band alignment at the heterojunction. Fig. 1(a) shows the 1 + 1 layers' band structure, where the band gaps are 1.63eV for MoS$_2$ and 1.14eV for MoTe$_2$. Together they form a straddled band alignment (type 1). Fig. 1(b) shows the 3 + 3 layers' band structure, where the MoS$_2$ bandgap decreases strongly to 1.36eV, and the MoTe2 bandgap decreases only slightly to 0.98eV. These form a staggered band alignment (type 2) with an effective tunneling bandgap of 0.48eV. The band alignments are in good accordance with [18] and [19]. When moving from the 1+1 to the 3+3 layer heterostructure, the decrease in effective band gap is indicative of orbital interactions between the two materials, consistent with the branch-overlaps when the bands of the MoS$_2$ and MoTe$_2$ overlap at several points in the band-structure.

III. DEVICE FABRICATION

To study the electron transport behavior of these heterojunction devices, we propose two types of device architectures,

the first one has a local bottom gate, meaning that the gate modulates only the MoTe$_2$ as shown in Fig. 2(a). The second architecture has a complete bottom gate where both the flakes are modulated together as shown in Fig. 2(b). The local bottom gate device is fabricated using palladium as metal followed by the deposition of 30nm Al$_2$O$_3$ as the gate dielectric. The devices are fabricated using exfoliated flakes where the MoS$_2$ and MoTe$_2$ flakes are transferred onto the substrate using a poly-methyl methacrylate (PMMA) dry transfer technique [20]. During the transfer, the flakes are aligned on the substrate in such a way that the entire MoTe$_2$ flake and the MoS$_2$/MoTe$_2$ overlap region are located above the bottom gate whereas the MoS$_2$ flake is ungated as shown in Fig. 2(a). The silicon back gate is non-functional. The source drain contacts were deposited by optical lithography.

For the complete bottom gate device, TiN is used as the gate metal followed by the deposition of 10nm HfO$_2$. After the transfer of the flake heterostructure on the substrate, ebeam lithography was done to pattern the contacts. MOSFET's of MoS$_2$ and MoTe$_2$ were fabricated alongside the heterostructure as shown in Fig. 2(b). This helps to measure and study the MOSFET characteristics of MoS$_2$ and MoTe$_2$ individually to aid in the understanding the heterojunction FET characteristics. Gold is deposited as contacts to the source and drain for both the device architectures.
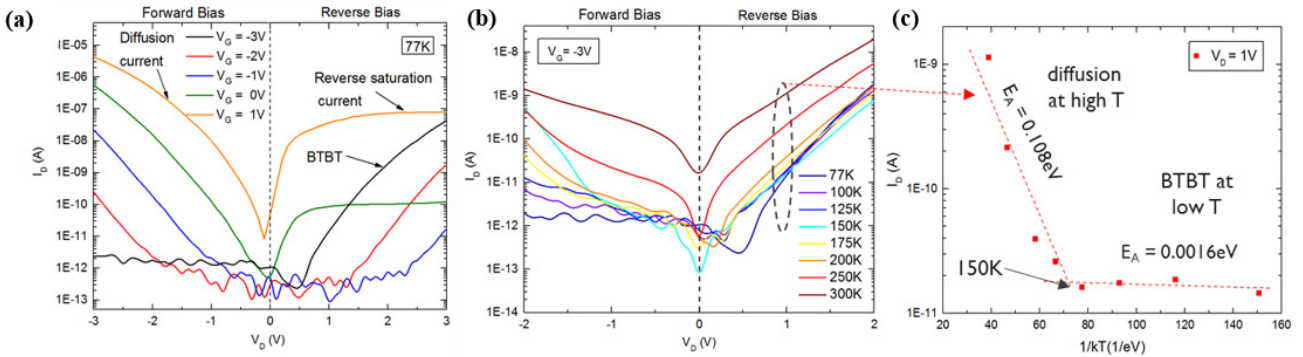
FIGURE 3. (a) $I_D - V_D$ characteristics with varying bottom gate measured at 77K.(b) Temperature dependence of tunneling current in the reverse bias at Vg = −3V.(c) Arrhenius plot extracted from (b) at V = 1V showing the change of slope from diffusion to tunneling at low temperatures.

Fig. 2(c) shows an AFM image of the fabricated device of the local bottom gate architecture along with the height profile shown in Fig. 2(e) along the indicated red line. Fig. 2(d) shows the Raman spectroscopy at the overlap region. The Raman characteristics obtained in the overlap region is a combined signal of the MoS$_2$ and MoTe$_2$ peaks, as shown in [21] and [22].

IV. RESULTS AND DISCUSSION

In the initial part of this section, we will discuss the results of the device using local bottom gate architecture followed by the results of the complete bottom gate devices. The devices are electrically characterized in vacuum at temperatures ranging from 77K to 300K. The MoS$_2$ contact is defined as the drain and the MoTe$_2$ contact as the source. Fig 3(a) shows the output characteristics at 77K and we shall discuss them at different gate biases.

At Vg = −3V, the MoTe$_2$ layer is strongly accumulated with holes. Therefore, the valence band minimum of MoTe$_2$ aligns above the conduction band maximum of MoS$_2$ creating a window for tunneling, as shown in the sketched band diagram of Fig. 5(c). The tunneling current increases for increasing reverse bias ($V_D > 0$). In forward bias ($V_D < 0$), the current is below the noise level (1pA) as the electrostatic barrier for diffusion is very high.

As the V$_g$ is increased to −2V, the electric field at the heterojunction is reduced and the BTBT current decreases. A significant forward bias current is observed at $V_D > -0.5V$ as the electrons acquire enough energy for diffusion. At higher gate biases of Vg $> -1V$, the tunneling current in the reverse bias is completely suppressed into the noise level (Fig. 3(a)) as there is no tunneling window. At Vg = 0V and above, the reverse bias is dominated by the reverse bias saturation current due to the drift in minority carrier concentration of MoTe$_2$.

We observe that when both the gate and drain biases are increased by 1V, the BTBT current remains identical. In order to understand this effect, which is also observed for other 2D TFETs [8], [9], we self-consistently calculate the 1-D electrostatic potential in the vertical direction
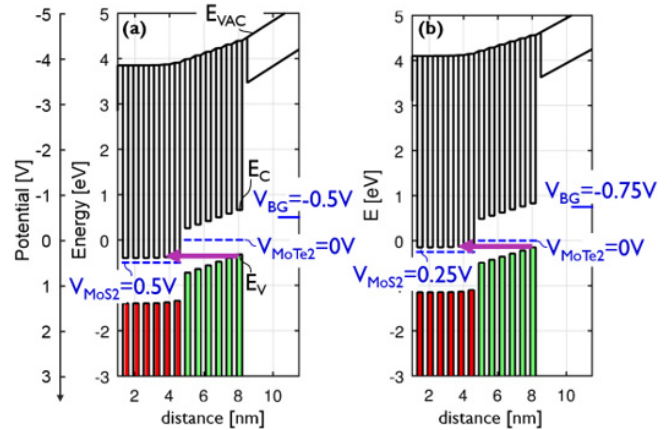

FIGURE 4. (a) Simulated band diagrams of 6-layer MoS$_2$ on 6-layer MoTe$_2$ on 30nm SiO$_2$ on a bottom gate. The MoS$_2$ layers are doped 5x10^{11}cm^{-2}. Filled electron states in are shown in red for MoS$_2$ and green for MoTe$_2$. (b) Simultaneously decreasing VMoS$_2$ and VBG shifts the band diagram up and near-identical BTBT paths are obtained.

using the Poisson equation. The electron and hole concentrations are calculated semi-classically. These simulations do not consider BTBT or other transport mechanisms, and do not consider interaction between electronic orbital positions of the different layers but the bandgaps and band alignment are taken from DFT in Fig. 1(b). The electrostatics are simulated for 6-layer MoS$_2$ on 6-layer MoTe$_2$ on 30nm SiO$_2$ with 0.3nm VdW's spacing considered between each layer. N-type doping is considered in the MoS$_2$ flake, which is commonly observed [1], The band diagram in Fig. 4(a) show this doping fixes the Fermi level position near the conduction band edge. Hence the back-gate voltage controls mainly the MoTe$_2$ bands. In Fig. 4(b) we observe that decreasing both the gate and the drain bias by 0.25V shifts the bands diagram up in energy, and near-identical BTBT paths are obtained, thus explaining the effect observed experimentally.

The simulations also show that the layers closer to the oxide are modulated more effectively compared to the ones further away. At low electric field, the electrons tunnel from the farthest layers creating long tunneling paths. As the electric field is increased, the tunneling paths are shortened. This
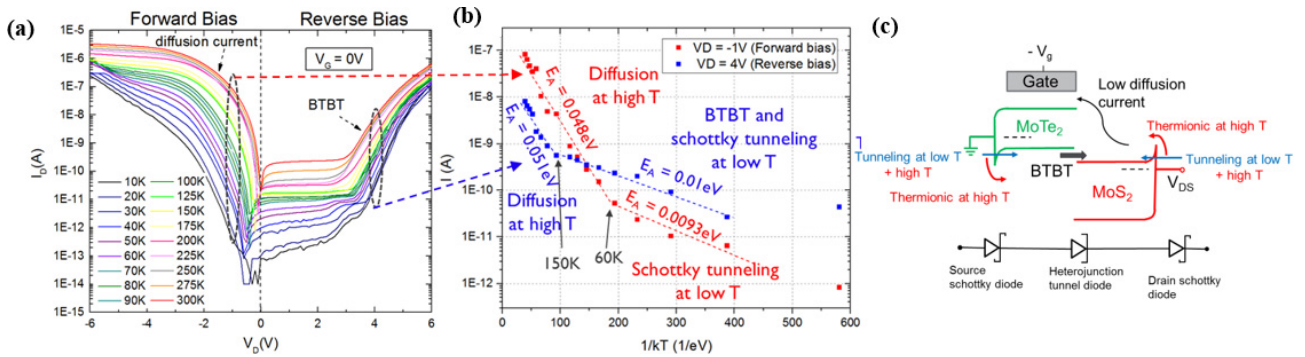
FIGURE 5. (a) $I_D - V_D$ characteristics at temperatures from 10K – 300K depicting diffusion mechanism at forward bias and BTBT at reverse bias. (b) Arrhenius plots for the temperature measurement extracted at the diffusion and tunneling regimes. (c) Schematic representation of the different transport mechanisms taking place on the device at different temperatures along showing the different diode behaviors at the Schottky contacts and tunnel junction.

transition from long to short tunnel paths is not ideal for a TFET and results in a poor subthreshold swing. To have ideal tunneling characteristics with steep switching, ideally monolayers are required for optimum electrostatic control. However, DFT simulations in Section II show monolayer MoS$_2$/MoTe$_2$ results in a straddled band alignment, which would also result in poor onset characteristics. Therefore, we conclude MoS$_2$/MoTe$_2$ is not an optimal material choice for heterojunction TFET.

When we compare our results with other work on MoS$_2$/WSe$_2$ TFETs [8], [9], the back-gate dependence of the BTBT and diffusion currents in the output characteristics is in good agreement, despite the absence of a top gate in our devices. However, we do not observe a Negative Differential resistance (NDR) in the forward bias. We interpret the lack of NDR in our devices as a lack of degenerate Fermi level in the top flake. The condition of Fermi level degeneracy is required for Esaki diode behavior, but is not required for TFET operation.

The temperature dependent $I_D - V_D$ characteristics are plotted in Fig. 3(b) at a bias of $Vg = -3V$ where the tunneling current is dominant. It is observed that the current values do not change significantly at low temperatures, but above 150K the current increases with temperature. To further understand this behavior, Arrhenius plots are extracted as shown in Fig. 3(b) at $V_D = 1V$. The plots show two different slopes with the transition taking place at 150K. The low activation energy of $E_A = 1.6meV$ below 150K is indicative of tunneling-limited current. Since the MoTe$_2$ flake is gated, the strongly negative V_g thins down the Schottky barrier for holes. As a result, at low temperatures the thermionic injection over the barrier is suppressed and the dominant mechanism is Schottky tunneling. Above 150K, generation currents become dominant and the carriers acquire enough energy for diffusion above the barrier indicated by the increase in $E_A = 108meV$.

To further understand the different transport mechanisms such as generation and recombination effects and the role of Schottky contacts in the forward and reverse biases, we

need to measure below 60K to see the effects of the Schottky contacts and its influence on the diffusion and BTBT currents. Thus, temperature measurements were done on the same device from 10K to 300K and E_A'swere extracted. Fig. 5(a) shows the output characteristics where the device is measured in a tunnel diode configuration where the gate is at zero bias. Applying no gate bias prevents gating of the contact regions. This helps in understanding how the ungated Schottky barriers play a role in the current transport at different temperatures. At $Vg = 0V$, the device functions as a diode undergoing diffusion at forward bias ($V_D < 0V$) and BTBT at reverse bias ($V_D > 3V$). Between $0 < V_D > 3V$, we also observe a reverse saturation current similarly seen in Fig. 3(a) and (b) due to the minority carrier which increases in current with increase in temperature.

Arrhenius plots are extracted from the diffusion and tunneling regimes as shown in Fig. 5(b) by the red and blue data points respectively. The Arrhenius plot of the forward bias currents are extracted at $V_D = -1V$ as shown by the red data points. Below 60K, the E_A is very low of 9.3meV which is indicative that the electrons do not have enough energy to thermionically inject across the Schottky barrier, therefore they undergo tunneling through the barrier. The high E_A of 48meV above 60K indicates that the electrons start to undergo thermionically assisted tunneling across the Schottky barrier along with increased carrier recombination and generation effects with increasing temperature.

Similarly, the Arrhenius plot for the tunneling regime was extracted at reverse bias of $V_D = 4V$ shown by the blue data points in Fig. 5(b). The E_A obtained from 150K to 300K is similar to the E_A in the diffusion regime (60K to 300K) with $E_A = 51meV$. As observed previously in Fig. 3(b) and (c), above 150K, the carriers acquire enough energy to undergo diffusion due to the increased thermionic injection from the contacts and generation effects thereby dominating the BTBT current to vary with temperature. Below 150K, it was observed from the previous Arrhenius plot in Fig. 3(c) that the E_A for the BTBT current is very low with a value of 1.6 meV. The reason for the very low
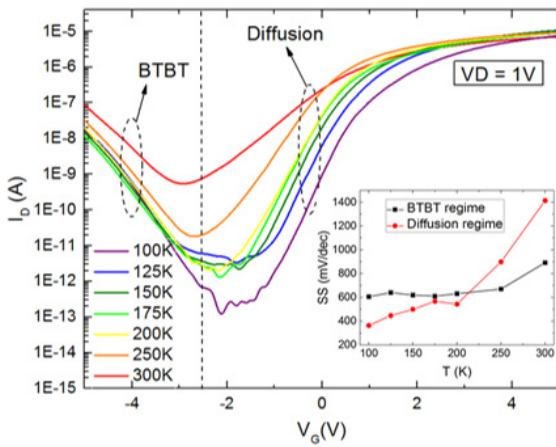
FIGURE 6. $I_D - V_G$ characteristics shown at different temperatures with the dependence of the diffusion and tunneling currents with temperature shown in the inset.

E_A obtained is due to the thinning down of the barrier by the applied gate bias. But for Fig. 5(a), there is no gate bias applied, therefore the barriers at the contacts are dominantly present. The E_A obtained in Fig. 5(b) is 10meV, which is 6 times higher and very close to the E_A in the diffusion regime below 60K. This can be understood by the fact that the Schottky contacts are more dominant on the current transport and the tunneling in the Schottky contacts are in series with the BTBT current.

Therefore, the study shows that the Schottky contacts have a current limiting contribution towards the device. From the plots, we see that, Schottky barriers act as individual Schottky diodes that are in series with our heterojunction tunnel diode. Fig. 5(c) shows a schematic of the different transport mechanisms in the device at different temperatures. The E_A obtained for these barriers are higher than that of the BTBT current which affect the device performance in terms of low subthreshold swing and low ON currents, hence an ohmic contact is required to eliminate the influence at the contacts to solely study the behavior at the heterojunction tunneling region.

Fig. 6. shows the transfer characteristics for the device at different temperatures. The device behaves as a p-TFET for Vg < −2V or a n-MOSFET for Vg > −2V. In the p-TFET mode, the BTBT current does not significantly vary with T in the range 100-200K and the subthreshold swing is 600mV/Dec and constant with temperature (inset of Fig. 6), indicative of BTBT. However, for T > 200K, the current increases with temperature due to recombination and Schottky contacts undergo thermionic injection. In the n-MOSFET mode the SS increases linearly with temperature, indicative of diffusion current. The subthreshold swing of these modes is very high, which is due to the large estimated oxide thickness (EOT) present thereby preventing fast switching.

All the results shown above are using the local bottom gate device, that has an ungated MoS_2 region. With the absence of a gate on the MoS_2 channel, there is no charge accumulation or depletion taking place over it. This leads to a high contact resistance and access resistance over the channel. But nonetheless, BTBT is still observed on our devices with the influence of the contacts.

Next, we discuss the results of the complete bottomgate devices. This architecture shown in Fig. 2(b) helps to understand the device behavior when both MoS_2 and $MoTe_2$ regions are modulated under the same gate bias. This creates a situation in which both the MoS_2 and $MoTe_2$ are accumulated or depleted with charge carriers simultaneously. In the case of $MoTe_2$, due to its ambipolar nature, accumulation of either electrons or holes are possible depending on the gate bias. Based on the gate bias applied, the hetero-FET can either undergo recombination of electrons and holes or diffusion. This recombination effect brings rise to the interesting phenomenon of negative differential transconductance, as explained in the following paragraphs.

Figure 7(a) and (b) show the transfer characteristics measured at room temperature where V_G is the voltage applied to the bottom gate. The plot shows the characteristics of MoS_2 FET, $MoTe_2$ FET and the MoS_2/$MoTe_2$ Hetero FET. The optical images of the devices are shown in the inset of Fig. 7(a) and (b). The transconductance of the MoS_2/$MoTe_2$ hetero FET are also shown for each device.

In case of the MoS_2/$MoTe_2$ Hetero FET in Fig. 7(a), for the region of Vg from −2V to −1V depicted as region A, I_D is very low within the gate leakage level of the measurement (not shown). This is because the MoS_2 is depleted of carriers and $MoTe_2$ shows hole accumulation. As a result, the electron path is blocked from source to drain resulting in low current. As we move from Vg −1V to 0V as shown by region B, the current increases and reaches a peak and starts to decrease. This peak which is centered around 0.6V corresponds to the condition where MoS_2 and $MoTe_2$ are in the subthreshold regimes. This is due to the exponential increase of electron current on the MoS_2 side followed by an exponential decrease of hole current from the $MoTe_2$ side. In other words, in region B, the current is governed by the recombination between the holes in $MoTe_2$ and electrons in the MoS_2. And the current peak observed around 0.6V is when the rate of flow of electrons and holes are matched. This is also shown by the gated transconductance alongside Fig. 7(a) as a change in current peak from positive to negative. This behavior is also known as NDT and has been demonstrated previously with other 2D material stack [10], [24], [25] in resonant tunneling devices [26] and modulation doped FETs [27]. The NDT phenomenon is observed in the transfer characteristics unlike Negative differential resistance which is observed in the output characteristics of degenerately doped heterojunction diodes [28]. Next, for Vg > 0V or region C, the current increases exponentially again as the electron conduction is dominated both by the MoS_2 and $MoTe_2$ regions. The $MoTe_2$ FET for this device has a low On -Off ratio, due to this, the peak to valley ratio of the negative differential transconductance peak
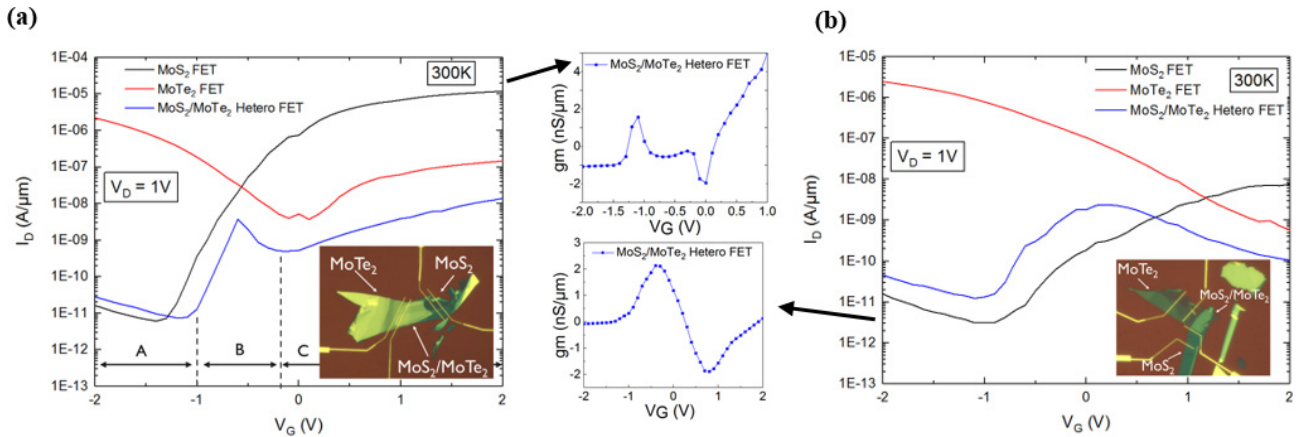
FIGURE 7. (a) $I_D - V_G$ characteristics of the device showing individual characteristics of the MoS$_2$ FET, MoTe$_2$ FET and heterojunction FET. The optical image of the device is shown in the inset of the graph withe the transconductance of the MoS$_2$/MoTe$_2$ hetero FET also plotted aside the graph. (b) $I_D - V_G$ characteristics of another device with the MoTe$_2$ FET showing only p-type conduction along with the optical image of the device in the inset and the transconductance curve alongside the plot.

in region B is lower in the MoTe$_2$ conduction side compared to the MoS$_2$ side.

Fig. 7(b) shows another hetero FET where the MoTe$_2$ flake shows a predominant p-type conduction. The origin of only p-type behavior is not clearly understood but could possibly be due to threshold voltage shift due to charge trapping. However further analysis must be done on this. For this device, with increasing V_G the NDT peak of the Hetero FET does not increase back as shown for the ambipolar MoTe$_2$ in Fig. 7(a). This is because at $V_g > 1V$ the MoTe$_2$ is depleted of carriers whereas the MoS$_2$ is accumulated with electrons. This creates a Hetero-FET device mainly dominated by recombination. These kinds of devices which show a sign changing gm are interesting for applications such as multi valued logic [29].

We observe that in the complete bottom gate configuration, recombination and diffusion are the dominant mechanisms. Even though BTBT is possible with this configuration, it is not the dominating mechanism. This is because when both the materials are under the same gate bias, the bands of MoS$_2$ and MoTe$_2$ are modulated with the same potential making it difficult to create a tunneling window (broken gap configuration). To overcome this, a higher V_D is required [24] as the electrons have to tunnel through long tunnel paths mentioned above by the 1D electrostatic simulations. However, to enhance the BTBT current, two separate gates that modulate the MoS$_2$ and MoTe$_2$ individually would be ideal. This ensures by applying different bias voltages on each flake to open the window for tunneling.

V. CONCLUSION

In summary, we have demonstrated band-to-band tunneling in a TMD based MoS$_2$/MoTe$_2$ heterostructures. DFT simulations shows a straddled band alignment for monolayer flakes, and a staggered band alignment for three or more layers. However, 1-D electrostatic potential simulations show poor electrostatic control and long tunneling paths with

thicker layers. Therefore, we conclude MoS$_2$/MoTe$_2$ is not an optimal material choice for heterojunction TFET. The low temperature measurements clearly distinguish the different mechanisms in the forward bias and reverse bias, and that the diffusion and tunneling currents are largely contact limited. The transfer characteristics show the device as a p-TFET for negative V_g and n-MOSFET for positive V_g. Negative differential transconductance was demonstrated using a complete bottom gate design with recombination and diffusion mechanisms dominating over BTBT current cannot be achieved with this architecture. In conclusion, a key challenge in achieving a steep subthreshold swing in 2D hetero TFETs apart from a low EOT and thinner layers are having ohmic contacts with a low contact resistance.

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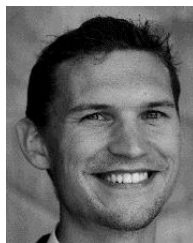
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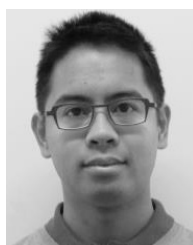
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