Received 4 December 2017; revised 2 March 2018; accepted 8 March 2018. Date of publication 13 March 2018;
date of current version 26 March 2018. The review of this paper was arranged by Editor M. K. Radhakrishnan.

Digital Object Identifier 10.1109/JEDS.2018.2815344

3-D Stacked Technology of DRAM-Logic Controller Using Through-Silicon Via (TSV)

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ABSTRACT This paper describes a four-layer-stacked chip with 45-nm dynamic random access memory (DRAM) dice and 65-nm logic controller, which are interconnected by backside-via-last through-silicon via (TSV) processes. Fabrication of backside-via-last process and multiple die stacking using chip-to-chip bonding are presented with electrical connection between TSV (5-μm-diameter/50-μm-length) and Cu interconnects. Excellent fabrication of stacked dice verified that the micro bumps with 12-μm diameter are bonded using three step temperature bonding profile. Further stacked DRAM/Logic performance and system verifications are demonstrated successfully using 3-D heterogeneous integration.

INDEX TERMS Backside-via-last TSV, three-dimensional heterogeneous integration.

I. INTRODUCTION

Increasing demands for faster computing ability on electronic devices such as smartphone, Internet of Things (IoT), and artificial intelligence (AI) applications promote the development of Dynamic Random Access Memory (DRAM) towards higher bandwidth, lower power consumption, and finer-pitch input/output (I/O) connection. However, semiconductor industry is approaching the bottleneck for transistor scaling. Three-dimensional (3D) integration technology is viewed as a promising solution to extend Moore's law for the next-generation semiconductor technology [1], [2]. In particular, 3D heterogeneous integration enables an approach to enhance efficiency significantly for DRAM/logic system architecture.

The key technologies include through-silicon via (TSV), thin wafer handling, wafer bonding, and micro bumps interconnection in the 3D platform. Vertical interconnection of Cu TSV connection with Cu/Sn micro bumps is an attractive approach for 3D integration [3]–[8]. A 3D packaging technology has been developed for DRAM using highly doped poly-Si TSVs [9]. The integration of Via-middle TSV processes in DRAM technology with major process issues were discussed [10]. Micron's 3D DRAM with re-architected DRAM dies achieves significant improvements in power and timing compared to a coarse-grained 3D DRAM design [11]. A 3-D test chip (DRAM/logic die) with temperature sensors and heaters were used to explore thermal effects and to develop advanced thermal modeling [12]. Although similar DRAM/logic system architectures have been presented, the lack of detailed chip-to-chip (C2C) bonding specification and system verification leads to this scheme difficult for further development.

In this study, the integrated 65-nm logic controller and 45-nm DRAM stacking with Cu TSVs is demonstrated. The Cu/Sn and Cu/Ni/Au micro bumps with 12 μm diameter are connected for inter-die to achieve vertical interconnection with TSVs. The C2C bonding method is adopted a three-step temperature profile for four DRAM dice stacked on a logic die. The structure design, die-stacking process flow, and system performance with the heterogeneous integration are presented as well.

II. TSV PROCESSES DEVELOPMENT

Fig. 1(a) shows TSV via-last schematic process flow which is fabricated from the backside of the Si wafer after the Complementary Metal-Oxide-Semiconductor (CMOS) process was completed. Firstly, the front-side micro bumps

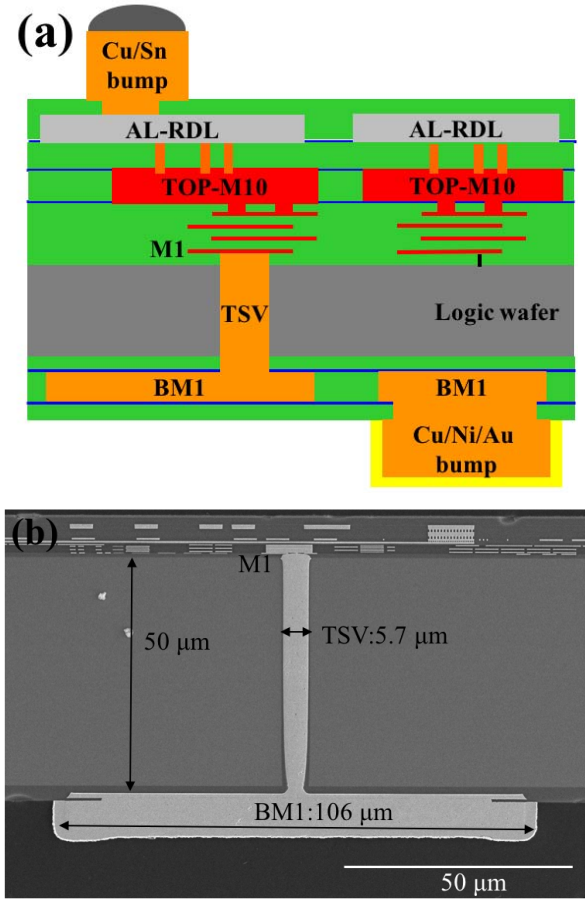

FIGURE 1. The Logic structure of via last TSV: (a) schematic, and(b) cross-sectional SEM images for a 5 × 50 μm TSV in the logic die.

(3-μm-thick Cu and 6-μm-thick Sn) with 12 μm diameter were fabricated on the Al pads. Secondly, the device wafer was bonded temporarily onto a Si carrier wafer using a thin-wafer handling process, and is thinned down to 50 μm. Thirdly, passivation layers were deposited on the backside of the device wafer to avoid leakage current, and then passivation opening and Si etching were subsequently performed for backside metal and TSV (5×50 μm) formation. Fourthly, the TSVs and backside metal-1(BM1) were plated using Cu-Damascene process. Then, the 7.1 μm-thick micro bumps (5-μm-thick Cu, 2-μm-thick Sn and 0.1-μm-thick Au) with 12 μm diameter were fabricated after backside metal finishing in the DRAM dice. However, the 7.1 μm-thick Cu/Ni/Au bumps with 100 μm diameter were fabricated in the backside of logic die to joint with the substrate. Finally, the Si carrier was de-bonded and is mounted onto blue tape for dicing. Fig. 1(b) shows the cross-sectional scanning electron microscope (SEM) image of the completed TSV scheme in the logic die.

III. DRAM AND LOGIC STACKING

In order to achieve a complex 3D IC package, a novel multi-layer die-stacking technology was applied in the stacked

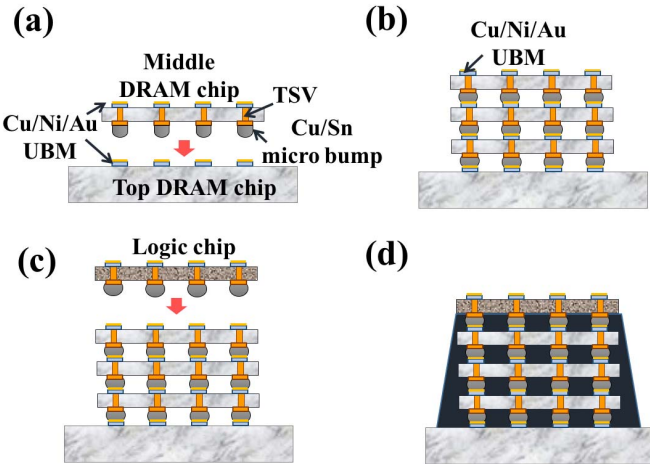

FIGURE 2. Process flow of DRAM/logic die stacking module: (a) a thin middle DRAM die stacked on the thick top DRAM die, (b) three middle DRAM dice stacked on the top DRAM die, (c) a thin logic die stacked on the DRAM dice, and (d) underfill encapsulation for the die-stacking module.

DRAM/logic integrated system. The 3D integrated circuit (IC) package comprises four DRAM dice, one logic die, and an organic substrate. The DRAM chips are divided into the top and the middle dice. Besides, the top DRAM die has a thickness of 200 μm and Cu/Ni/Au under bump metallization (UBM) fabricated onto the die surface. The thickness of the middle DRAM die was thinned down to 50 μm, then Cu/Ni/Au UBM and Cu/Sn micro solder bumps were fabricated onto the front side and back side of the die, respectively. As shown in Fig. 2(a)–(d), the process flow of DRAM/logic die-stacking module is carried out first. All these dice were surface cleaned by vacuum plasma treatment before the assembly process. A thicker top DRAM die was adopted to be abase. Middle DRAM die was bonded onto the top DRAM die with thermo-compression bonding using the flip-chip method. As three middle DRAM dice were stacked on the top DRAM die, the logic die was bonded onto the last middle DRAM die. The underfill encapsulation process for die-stacking module was performed and is used to protect micro solder bump and the module. After post curing, a rigid die-stacking module with multiple layers of thin DRAM/logic dice was established successfully.

Fig. 2 demonstrates that four-times bonding processes were executed on top DRAM die. Two types of bonding profile were developed to meet each layer of bonding process, as shown in Fig. 3 and Fig. 4. Bonding temp._1 in Fig. 3 is applied to layer 1 and layer 2 for chip stacking. However, Bonding_temp._2 is performed to layer 3 and layer 4. Fig. 3 shows temperature profile for Cu/Sn micro bumps bonding. Primarily bonding head uses a three-step temperature profile until achieving the melting temperature of Sn. The bonding substrate of Cu/Ni/Au UBM was adopted a bonding temperature of 100 °C for micro bump joints. Step 1 and Step 2 are bonded at 80 °C and 200 °C, respectively, before the melting point of Sn and are brought into contact with a constant bonding force. The two steps allow the

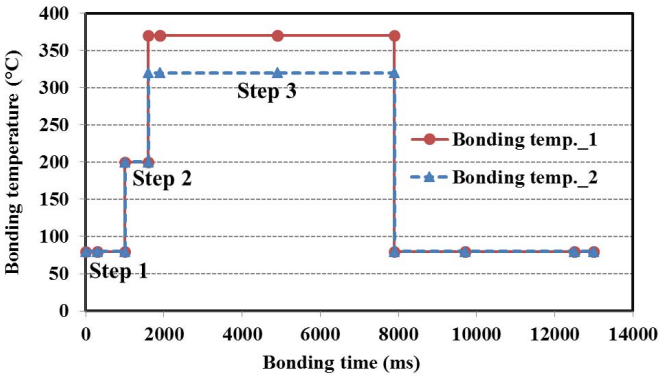

FIGURE 3. Temperature Schematic of micro bump bonding profile.

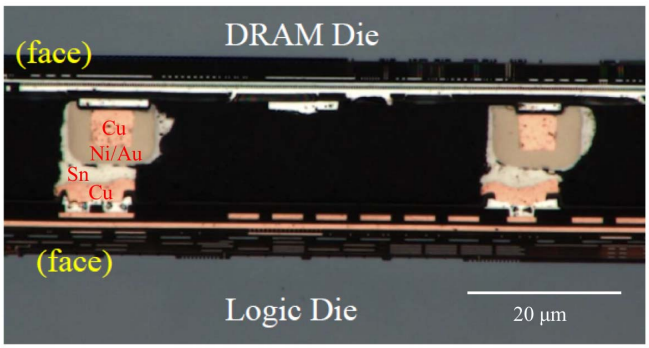

FIGURE 5. Cross-section of the DRAM/logic die stack.

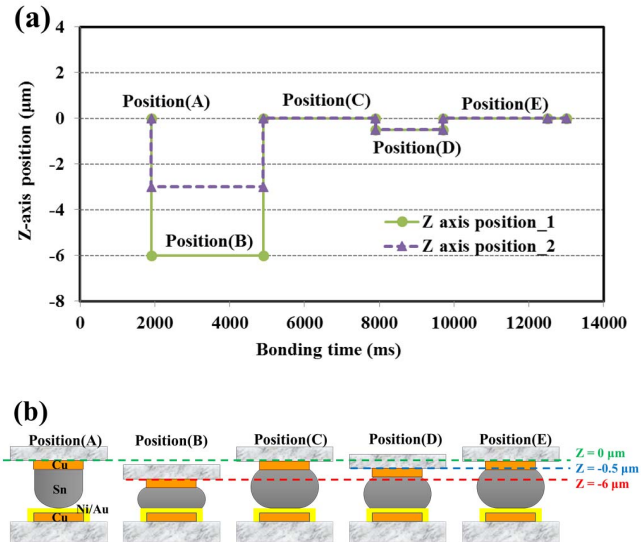

FIGURE 4. Micro bump bonding profile: (a) a schematic of Z-axis position, and (b) stress positon during bonding time.

softening of solder material and were close to contact in the micro bump joints early in the process. The bonding temperature of Step 3 is needed to be higher than the melting point of Sn (230 °C) because the thermal energy can consume easily through the Si die. Therefore, the final bonding temperature of Bonding temp._1 was set at 370°C to stack each other for layer 1 and layer 2. However, layer 3 and layer 4 were bonded at 320°C to prevent Sn melting in layer 1 and layer 2. Besides, the final step of bonding temperature was combined with a cool down at least 5100 ms.

Fig. 4 provides the Z-axis Schematic of micro bump bonding profile. The bonding method is adopted the force mode with a bonding force of 10 N before 2000 ms, and then the Z-axis bonding mode is applied to micro bumps bond after 2000 ms. Layer 1 and layer 2 were bonded using Z axis position_1 in Fig. 4(a), but layer 3 and layer 4 of chip stacking were adopted by Z axis position_2. As shown in Fig. 4(b), the movement of Position (A)-(E) during different bonding period. The Z value of Position (A) was defined to zero when the micro bumps were in contact with each other. Z axis position_1 of Position (B) shows that the movement is stressed to -6μm to ensure bonding quality during 3000 ms. However, Z axis position_2 was only stressed to -3 μm to avoid the micro bump misaligned joints below the bonding layers at peak temperature above the melting point of Sn (230 °C). Position (C) presents the Z position is moved to original point. Moreover, the bonding interface could be joined well between Sn and Au layer. Micro bump joints transform a bulk and have a thermal expansion during cooling down. Therefore, micro bump joints were needed to give -0.5 μm in order to prevent the variation between chip gaps in Position (D). Finally, Position (E) shows the Z position is returned to original point.

Furthermore, a relationship between Fig. 3 and Fig. 4(b) could be also discussed. The bonding head of Position (A) was bonded at 200 °C for 2000 ms to soften solder material and then contact micro bump joints early in Step 1 and Step 2. For the main bonding process of Step 3, the Position (B) and Position (C) were bonded at 370 °C (layer 1 and layer 2) or at 320 °C (layer 3 and layer 4) to stack each other between 2000 ms and 8000 ms. Finally, the Position (D) and Position (E) were combined to cool down after 8000 ms. After bonding process, the micro bumps are converted to intermetallic compound (IMC) through interdiffusion process and has an excellent bonding between metal joints. Final bonding process finished and micro solder joints can be seen in Fig. 5.

In Fig. 6, the X-ray photo shows that the TSVs and micro bumps are connected precisely between stacked DRAM and logic dice. Furthermore, the DRAM/logic die-stacking module was flipped and placed on the organic substrate with the conventional solder flip-chip mounting through the reflow process. Then, underfill encapsulation for the 3D IC package was also applied. Related processes were illustrated in Fig. 7(a)–(b). Warpage at the die edge sometimes observed during the C2C bonding. However, optimized underfill dispersion and bonding pressure can effectively overcome the issue, as shown in Fig. 8.

Finally, Fig. 9 (a) shows that four DRAM and one logic dies are stacked and assembled on the Bismaleimide Triazine (BT) substrate using the flip-chip mounting and

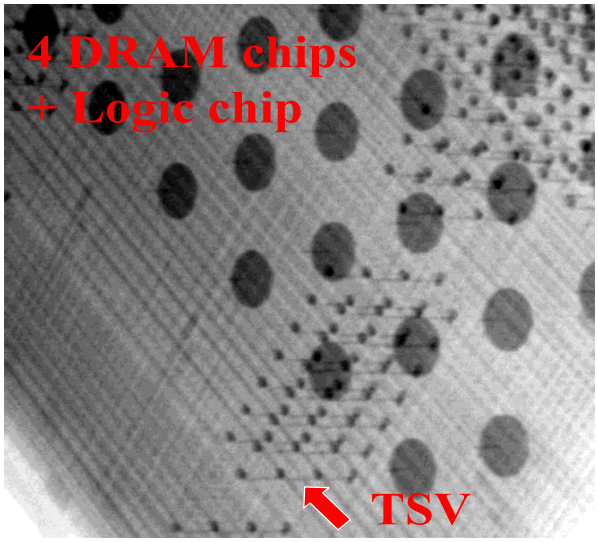

FIGURE 6. X-ray image of stacked logic-DRAM.

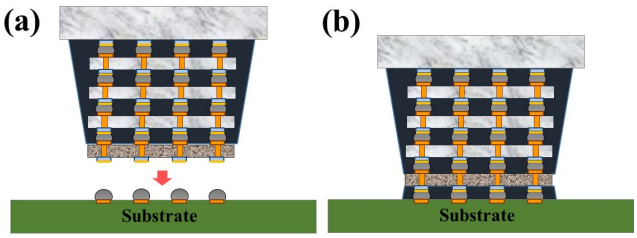

FIGURE 7. Process flow of DRAM/logic die-stacking module: (a) DRAM/logic die-stacking module flipped and bonded onto the substrate, and b) Underfill encapsulation for packaging.

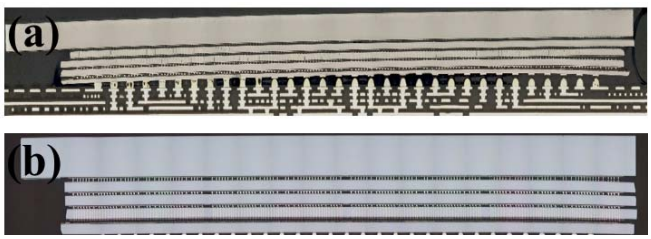

FIGURE 8. Four DRAMs and one logic stacking (a) before, and (b) after warpage optimization (dimension not to scale).

reflow soldering. Then, the stacked dice were assembled onto printed circuit board (PCB) with a socket to measure the signals, as shown in Fig. 9(b).

IV. STACKED LOGIC-DRAM PERFORMANCE EVALUATION

The logic die, which was incorporated in the 3D-stacked IC, acts as an I/O interface to the external memory controller with the DRAM dice shown in Fig. 10. In the package, the DRAM dice is connected to the logic die through TSV and micro bump connections. Each DRAM die has a half Gb capacity and is divided into 16 tiny channels distributed over the die area. Each channel, including individual TSVs and micro bumps for I/O, command, and address signal

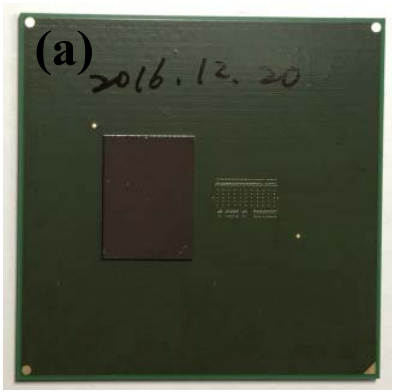

FIGURE 9. 3D stacked DRAM (a) on substrate, and (b) on board for signal measurements.

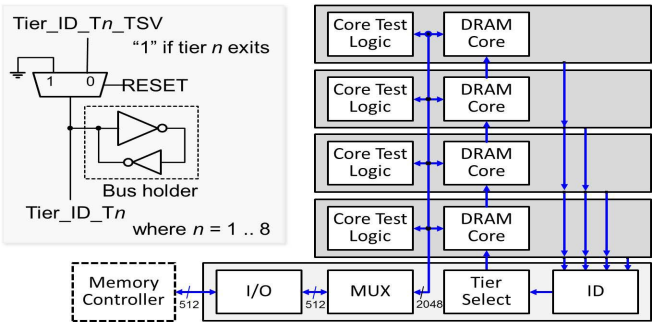

FIGURE 10. 3D stacked DRAM and tier ID circuit.

connections was further divided into four quadrants. Each quadrant has 32-bit I/O, therefore, one channel has 128-bit I/O. As a result, the DRAM dice with 16 channels have 2048-bit I/O totally. Besides, the logic die multiplexes four channels with 512 bit I/O at a time. Test pads were positioned at the center of the die for the probe test during the wafer sort.

The interface between the DRAM and logic dice is made asynchronous to save power. The operations of the DRAM dice were governed by a column-access strobe signal CAS_ST provided by the logic die. When inactive, CAS_ST keeps low. The data words within each channel are reconfigurable for fault tolerance [13]. In other words, the four quadrants of a channel can come from one DRAM die, two DRAM dice, or four DRAM dice, depending on the number of DRAM dice available and configured in the stack.

The tier ID circuit identifies the presence of each DRAM die in the stack by simply propagating a "1" towards the logic die. Fig. 11 shows the detected outcomes of the one- and

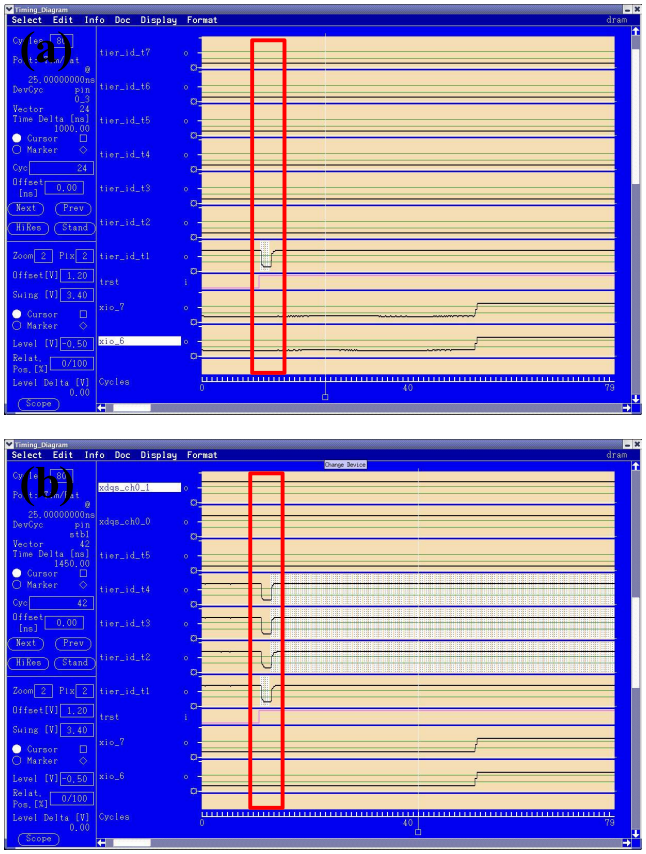

FIGURE 11. **(a) One DRAM die/Logic can be shown in the stack, and (b) Four DRAM dies/Logic are presented in the stack.**

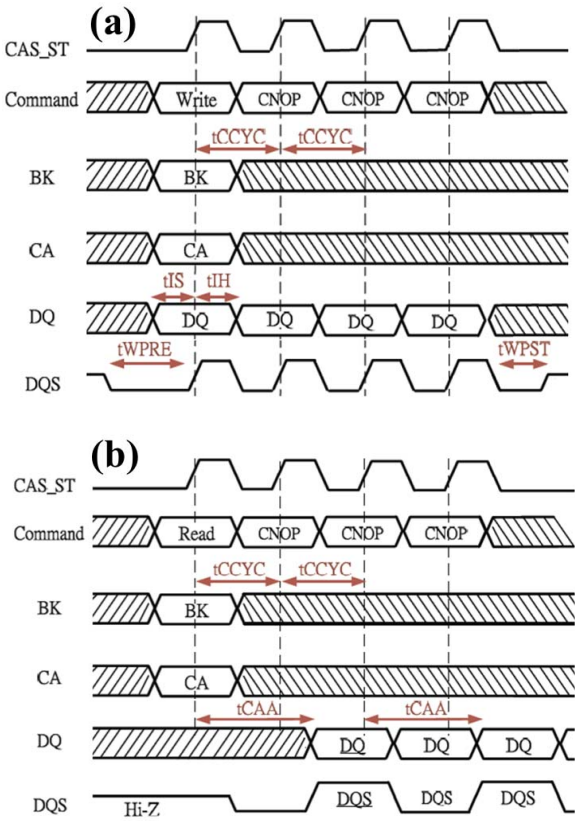

FIGURE 12. **DRAM/logic integrated system (a) Burst write, and (b) Read.**

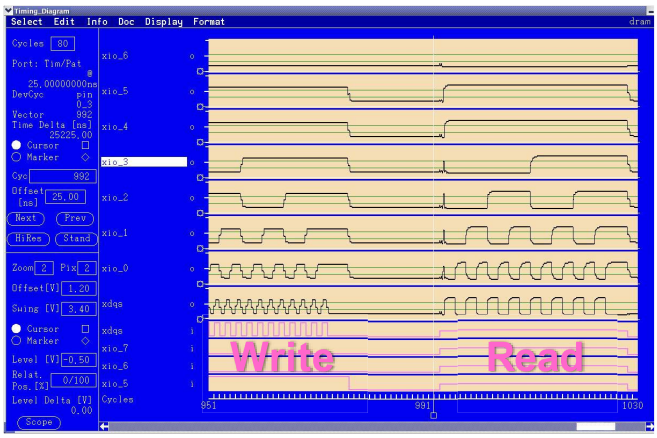

FIGURE 13. **Write-Read test of the DRAM/logic die stack.**

four-DRAM die stacks of the tier ID test, where a negative pulse indicates the presence of a particular tier during the detection phase. The information is sent to the tier-select circuit in the logic die. Note that up to eight DRAM dice can be presented in the stack, even though only a maximum of four dice can be activated at the same time. The extra DRAM dice become redundant and serve as spares.

In Figure 12, BK (bank address): signals for bank selection; CA (command and address): signals for command (C) and row/column address (A); DQ (input/output data): signals for data input (D) when write and data output (Q) when read; DQS (input/output data strobe): signals for data strobe (by rising edges when write and by both rising and falling edges when read). A Burst write and burst read schemes were implemented with CAS_ST and data strobe signal DQS. During write, DQS implements the same frequency as CAS_ST using only rising edges to strobe the DQ signals, while during read, DQS implements a half of the frequency using both rising and falling edges to strobe the DQ signals. The logic die access each channel of the DRAM dies in a cache line of 512 bits or four consecutive cycles. To simplify the interface design, the data strobe is made to operate at single data rate, similar to JEDEC wide I/O. A write-read test was performed to verify the functionality. Fig. 13 shows the waveforms of the DRAM die stack operating at 40 MHz with cycle time tCCYC = 25 ns. The highest operable frequency during the test is 160 MHz, albeit lower than the 200 MHz target, still demonstrating a data bandwidth of 40.96 GB/s.

V. CONCLUSION

A five-layer die stack with four 45-nm DRAM dice and one 65-nm logic die has been demonstrated using a back side via-last TSV process. Excellent fabrication, such as 5-μm-diameter TSVs, 12-μm-diameter micro bumps, 50-μm-thick

die bonding, and substrate/board stacking have been incorporated in the 3D integration scheme. The stacked dice verified that the Cu/Sn micro bumps shown excellent bonding quality using a three-step temperature bonding profile. A write-read test of the die stack has been executed to confirm the functionality successfully. In this paper, the stacked DRAM/logic performance and system verifications has shown the manufacturing ability in high performance 3D heterogeneous integration.

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Dr. Chen has authored over 270 publications and holds 80 patents. He has given over 70 invited talks in industries, research institutes, and universities worldwide. He is currently the committee member of IEDM, IEEE IITC, IEEE 3DIC, IEEE SSDM, and IEEE VLSI-TSA. He is a member of Phi Tau Phi Scholastic Honor Society. His current research interests are 3-D integrated circuits, advanced packaging, and heterogeneous integration.