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Low Power and Low Noise Shift Register for In-Cell Touch Display Applications

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ABSTRACT This paper proposes a shift register circuit integrated in in-cell touch display panels that achieves low power operation, low coupling noise, and high long-term reliability with 11 thin film transistors (TFTs) and two capacitors. A time division driving method is utilized to prevent the crosstalk of display signals into touch circuits, and two pre-charging nodes are employed to relieve the uniformity degradation of output signals caused by different stresses on pull-up TFTs. The proposed circuit activates a drain of the first pre-charging TFT only at display scanning periods, which reduces coupling noises and power consumption. In addition, an internal inverter is turned off for touch sensing operations, resulting in a wide range of threshold voltage shift compensation and low power consumption. SPICE simulation results with a low temperature poly silicon TFT model show that the proposed circuit compensates for the threshold voltage shift up to 17 V. In a 60 Hz full-HD display with a 120 Hz touch reporting rate, the noise level of the first pre-charging node is −16.78 dB in between 2.37 and −28.95 dB of two previous circuits, and the total power consumption for 160 stages is substantially reduced to 4.44 mW compared to previous approaches.

INDEX TERMS Low power, low noise, shift register, in-cell touch, TFT.

I. INTRODUCTION

Gate driver circuits have been integrated on display panels at the backplane of thin film transistors (TFTs) to simplify a manufacturing process and lower the overall price of products [1]–[7]. In addition, touch panels have been widespread in most mobile devices such as smartphones, tablet PCs, and laptops, due to their effectiveness as an intuitive user interface to displays. Particularly, in-cell touch technologies have attracted much attention thanks to its thin thickness, light weight, and low price [8]–[12], because touch sensors are embodied in conjunction with display pixel circuits. On the other hand, the crosstalk becomes more serious between display and touch sensing signals owing to their integration with very small gaps. To reduce this crosstalk while increasing the touch reporting rate, two operations of touch sensing and display scanning are separately conducted at different time slots by a time division driving method (TDDM) [13], [14]. The display area is divided into several blocks and the touch sensing puts into action in between scanning operations of display blocks. Therefore, the gate driver circuit must be able to stop at a certain line and restart from that line to drive a next display block. In contrast, a specific shift register circuit that is the first stage of each display block experiences the longer high voltage stress on a pull-up TFT than others, leading to the uniformity degradation of gate pulses and resultant visible line artifacts [14] that must be addressed. This uniformity issue caused by threshold voltage (V_{th}) shifts can be solved by putting the long voltage stress on a pull-up TFT of a first pre-charging node instead of a second pull-up TFT that directly drives an output [15], [16]. It has been reported that the V_{th} shift of the first pull-up TFT has very little impact on the uniformity degradation compared to the second pull-up TFT. There have been two approaches to control the drain voltage of the first pull-up TFT. One applies the clock signal and the other connects the constant supply voltage. While the clock signal causes the coupling noise on the first pre-charging node, the constant voltage increases the power consumption with substantial reduction on coupling noises. However, this paper proposes a shift

register circuit that achieves low power consumption as well as low coupling noise at the same time. Furthermore, this scheme extends the compensation range for V_{th} shifts of the first pull-up TFT, compared to the supply voltage connection scheme. The extended compensation range allows proposed shift registers to be implemented at various TFT backplanes such as amorphous silicon (a-Si) and oxide TFTs.

II. PROPOSED LOW POWER AND LOW NOISE SHIFT REGISTER

A proposed shift register circuit for in-cell touch display panels is composed of eleven TFTs (T1-T11) and two capacitors (C1, C2) with high and low supply voltages of VGH and VGL as shown in Fig. 1. A[n] is a first pre-charging node to hold high voltage during touch sensing periods and Q[n] is a second conventional pre-charging node to drive an output (V_g[n]). A[n] is charged through T1 by a previous output (V_g[n−1]) and is discharged through T2 by a clock signal (CLK). Q[n] is generally charged via T3 controlled by A[n] and is discharged through T4 and T7 by a next output (V_g[n+1]) and an inverter output (QB[n]). However, Q[n] can be also discharged through T3, T10, and T11 in touch sensing periods by setting EN1 to low. When Q[n] is lower than EN1, T11 is off by a zero gate-source voltage. In the opposite situation, T10 is turned off when EN1 and EN2 are set to the same voltage level. Therefore, T10 and T11 allow Q[n] to be discharged only when EN1 is low and EN2 is high as shown in Fig. 2.

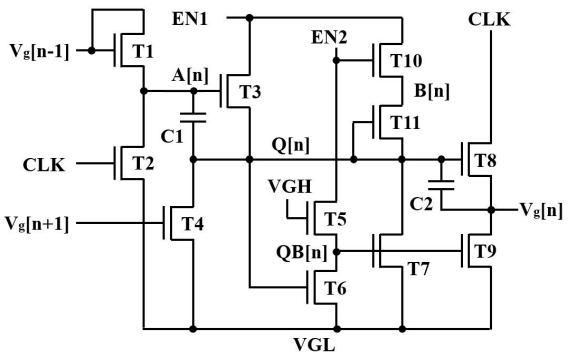

FIGURE 1. Schematic of a proposed shift register.

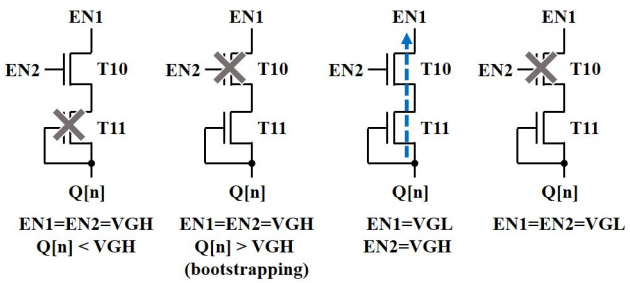

FIGURE 2. Q[n] discharging path control by T10 and T11. A discharging path is marked by a blue dotted line.

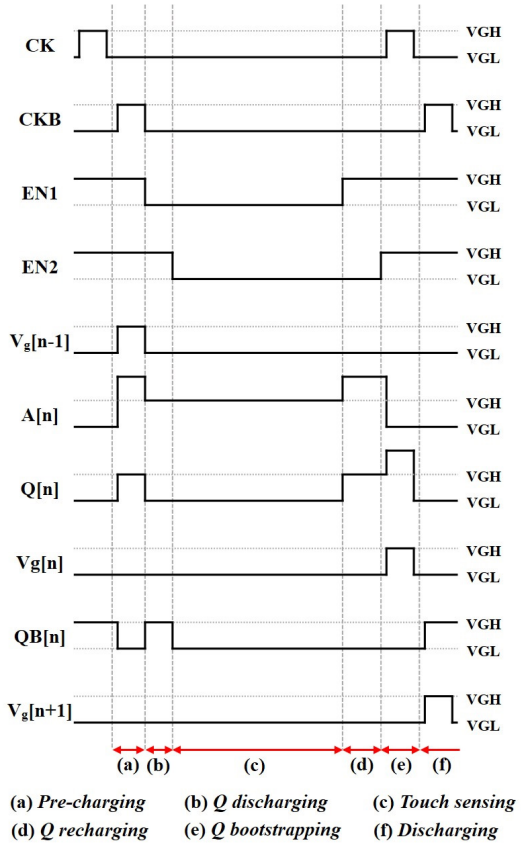

FIGURE 3. Timing diagram of a first shift register in a scanning period. The previous pulse is sampled at A[n] that maintains the high voltage during a touch sensing period. The output pulse takes place behind the end of the touch sensing period.

Unlike two previous approaches of clock and supply connection methods [15], [16], a drain of T3 is connected to EN1 that is set to high and low voltages during display scanning and touch sensing periods, respectively. Additionally, EN2 that is a delayed version of EN1 is linked to an internal inverter to enhance the compensation range for V_{th} shifts of T3 along with reduced power consumption.

To explain the operation of a proposed shift register in more detail, it is assumed that a n-th circuit is a first stage in a current scanning period and a (n-1)-th one is a last shift register in a previous scanning period. In addition, CLK signals of first and last stages are driven by CK and CKB, respectively. CK and CKB are clock signals that are out of phase to each other with some non-overlap interval.

The operation of the first shift register in a current scanning period is explained with six steps of *Pre-charging*, *Q discharging*, *Touch sensing*, *Q recharging*, *Q bootstrapping*, and *Discharging* as depicted in Fig. 3 and Fig. 4.

1) *Pre-charging:* A[n] and Q[n] are pre-charged through T1 and T3 by V_g[n−1] and EN1 as shown in Fig. 4(a). Especially, C1 takes a role to bootstrap A[n] to higher voltage than VGH and to maintain A[n] over the current leakages of TFTs. Because EN1 is higher than Q[n], source and gate of

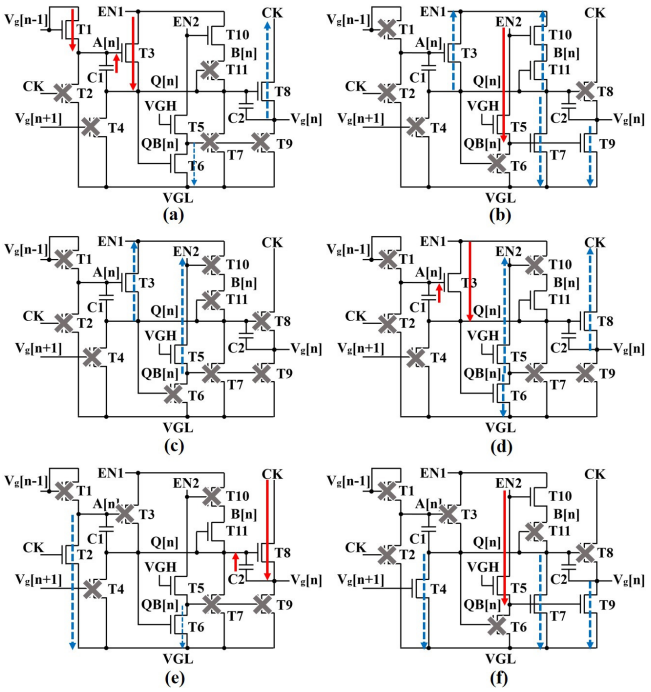

FIGURE 4. **Operations of a first shift register in a scanning period after the end of a touch sensing period (a) *Pre-charging* (b) *Q discharging* (c) *Touch sensing* (d) *Q recharging* (e) *Q bootstrapping* (f) *Discharging*. Red solid lines are charging paths and blue dotted lines are discharging paths.**

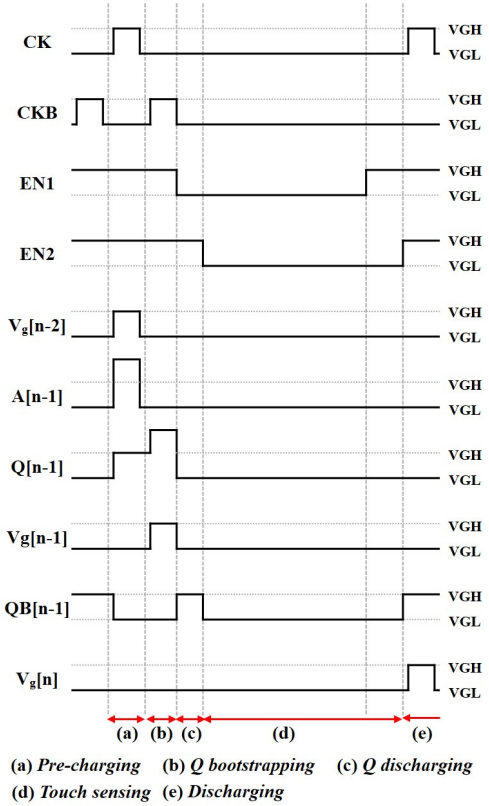

FIGURE 5. **Timing diagram of a last shift register in a scanning period. After the output pulse is generated, a touch sensing period begins.**

T11 get shorted, which disconnects a current path through T10 and T11. QB[n] is pulled down to VGL by an inverter of T5 and T6 and turns T7 and T9 off.

2) *Q discharging:* Q[n] is discharged through T3, T7, T10, and T11 as presented in Fig. 4(b). T3 is turned on due to A[n] storing the pre-charged voltage, T7 is on by an inverter, and T10 and T11 become a pull-down path by low EN1 and high EN2. A delay between falling edges of EN1 and EN2 needs to be set sufficiently to discharge Q[n] and to charge QB[n]. In this paper, a line time is assigned to the delay. This step is of the most importance to improve the V_{th} uniformity of T8 for shift registers by maintaining Q[n] at the discharged state in touch sensing periods.

3) *Touch sensing:* All signals of EN1, EN2, and CK are driven at VGL. Therefore, node voltages at the previous *Q discharging* step are held on except for QB[n] as illustrated in Fig. 4(c). Especially, the low EN2 at a drain of T5 completely removes the through current from VGH to VGL in the inverter, resulting in the reduced power consumption.

4) *Q recharging:* EN1 returns to VGH to charge Q[n] again through T3 by high voltage stored at A[n] as depicted in Fig. 4(d). QB[n] is kept at VGL by low EN2, which enables T3 to charge Q[n] without any pull-down paths. Thus, the delay between rising edges of EN1 and EN2 has only to guarantee that EN1 becomes VGH prior to EN2. This enhances the compensation capability for V_{th} shifts of T3.

5) *Q bootstrapping:* A[n] is discharged via T2 and Q[n] becomes a floating node of high voltage as shown in Fig. 4(e). Then, the rising transition of CK boosts Q[n] into higher than VGH. Even though Q[n] is bigger than EN1, source and drain of T10 get shorted by EN1 and EN2 of VGH. Therefore, T10 is turned off and Q[n] is retained as a floating node during bootstrapping.

6) *Discharging:* The output of a next stage (V_g[n+1]) is asserted and Q[n] and V_g[n] are pulled down with T4, T7, and T9 as described in Fig. 4(f).

Whereas, the operation of a (n-1)-th stage that is a last one in a scanning period is explained with five steps of *Pre-charging*, *Q bootstrapping*, *Q discharging*, *Touch sensing*, and *Discharging* as depicted in Fig. 5 and Fig. 6. Since this shift register finishes the pulse generation before a following touch sensing period, the *Q recharging* step is skipped.

1) *Pre-charging:* This is exactly the same as the *Pre-charging* step of the n-th shift register. A[n−1] and Q[n−1] are pre-charged through T1 and T3 by V_g[n-2] and EN1 as shown in Fig. 6(a).

2) *Q bootstrapping:* This is also equivalent to the *Q bootstrapping* step of the n-th shift register as illustrated in Fig. 6(b). A[n−1] is discharged by CKB turning T3 off and Q[n−1] is retained as a floating node of high voltage. Then, Q[n−1] is boosted to higher voltage than VGH at the rising transition of CKB for the output pulse (V_g[n−1]) generation.

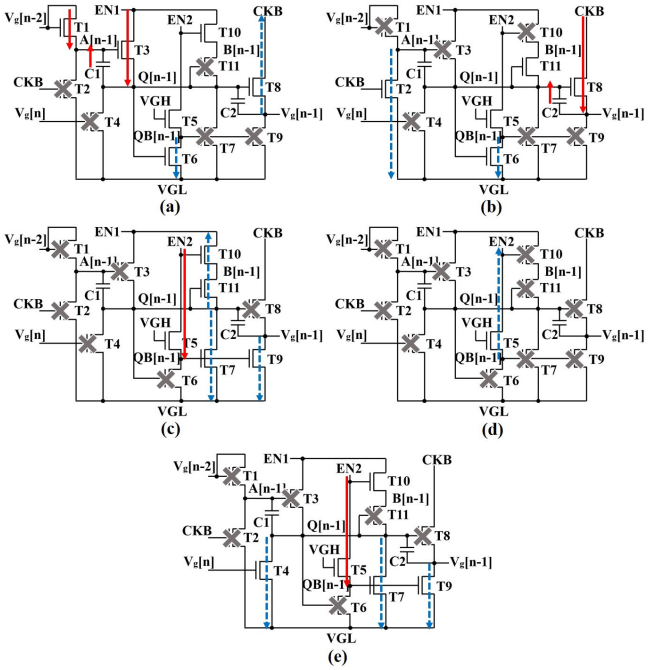

FIGURE 6. **Operations of a last shift register in a scanning period prior to a touch sensing period (a) *Pre-charging* (b) *Q bootstrapping* (c) *Q discharging* (d) *Touch sensing* (e) *Discharging*. Red solid lines are charging paths and blue dotted lines are discharging paths.**

3) *Q discharging:* Because A[n−1] is VGL, Q[n−1] is discharged mainly through T10 and T11 as presented in Fig. 6(c). Therefore, the duration of the voltage stress on T8 is not extended for the touch sensing period. T7 is turned on after Q[n−1] is fairly pulled down to activate the inverter.

4) *Touch sensing:* All signals of EN1, EN2, and CKB are driven at VGL to maintain internal voltages at low level as shown in Fig. 6(d) that is equal to the n-th stage.

5) *Discharging:* The output of a next stage (V_g[n]) is asserted after a touch sensing period is completed and Q[n−1] and V_g[n−1] are pulled down with T4, T7, and T9 as described in Fig. 6(e).

All other shift registers in scanning periods put into action at the sequence of *Pre-charging*, *Q bootstrapping*, and *Discharging*.

III. SIMULATION RESULTS

A proposed shift register has been simulated with a n-channel low temperature poly silicon (LTPS) TFT model by simulation program with an integrated circuit emphasis (SPICE). Threshold voltage, mobility, and overlap capacitance of TFTs are 1.94 V, 37.907 cm^2/V·s, and 0.16 fF/mm, respectively [6] and the transfer curve is represented in Fig. 7.

The channel widths of TFTs are as shown in Table 1 and all channel lengths are equal to 7 μm with C1 and C2 of 0.3 pF and 2 pF. Supply voltage levels of VGH and VGL are 25 V and 0 V and resistive and capacitive loads of a gate line are assumed to be 2.2 kΩ, and 60 pF [15]. A line time and a frame time are set to be 4 μs and 16 ms for

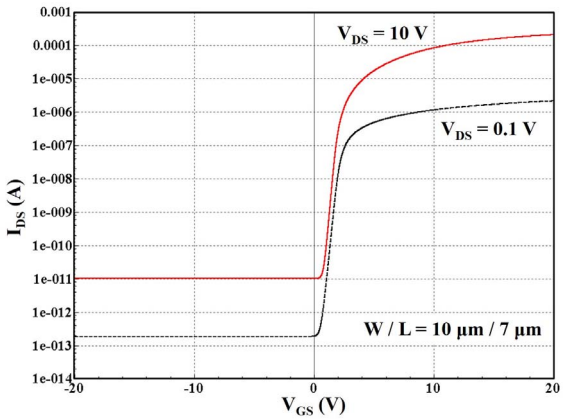

FIGURE 7. **Transfer curve of LTPS TFT for SPICE simulation.**

TABLE 1. **Channel widths of TFTs in a proposed shift register.**

TFT	Width	TFT	Width	TFT	Width
T1	10 μm	T2	10 μm	T3	30 μm
T4	10 μm	T5	10 μm	T6	100 μm
T7	10 μm	T8	1000 μm	T9	1000 μm
T10	10 μm	T11	10 μm		

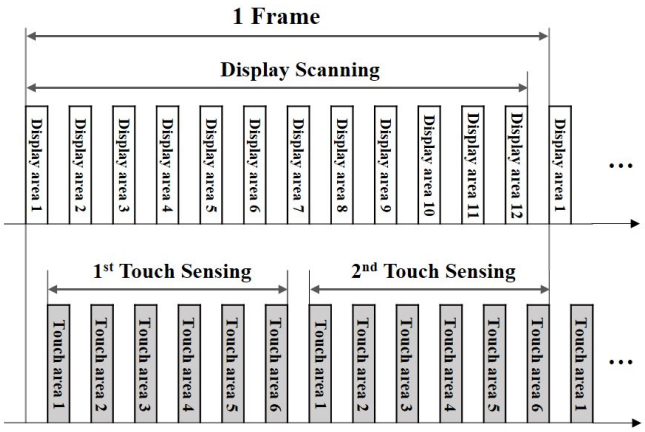

FIGURE 8. **Timing diagram of TDDM used for simulation.**

a 60 Hz full HD (1920 × 1080) display panel with a 120 Hz touch reporting rate. By applying TDDM, one frame time is divided into twelve display blocks, that is, 160 lines per each display block and one touch information is reported every six touch sensing periods as depicted in Fig. 8 [13].

Shift registers are configured for a gate driver as shown in Fig. 9, where EN1 and EN2 are applied to all stages in a same fashion and CK and CKB are connected to odd and even ones, respectively.

First of all, waveforms of a 9-th shift register in the middle of a first scanning period are presented in Fig. 10. EN1 and

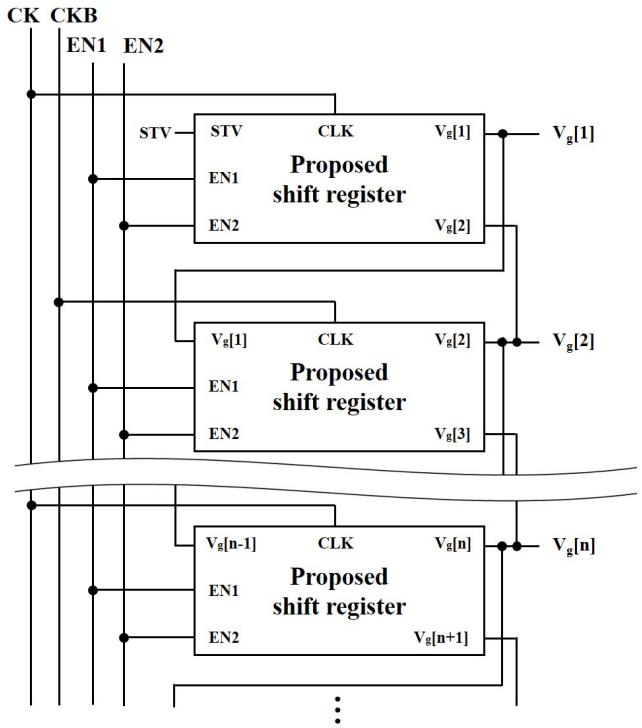

FIGURE 9. Configuration of proposed shift registers for a gate driver. While EN1 and EN2 are connected to all shift registers in a same way, CK is connected to odd ones and CKB is connected to even stages.

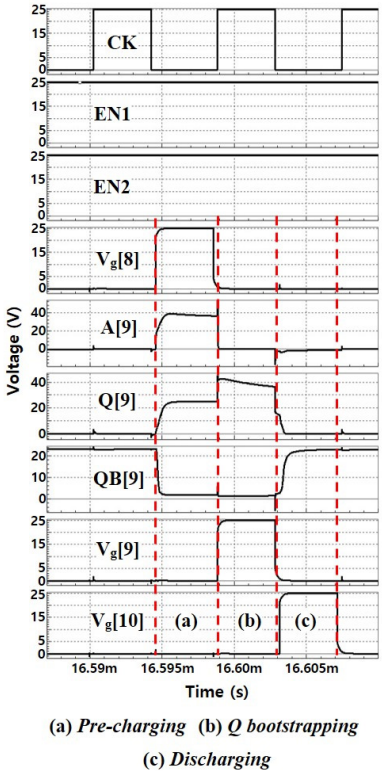

FIGURE 10. Simulated waveforms of a 9-th shift register in a scanning period.

EN2 stay at VGH and the pulse of V_g [9] takes place in a conventional way through *Pre-charging*, *Q bootstrapping*, and *Discharging* steps.

Waveforms of first and last stages in a scanning period are depicted regarding 161-st and 160-th shift registers in Fig. 11 and Fig. 12, respectively. For a 161-st stage, A[161] is pre-charged by V_g[160] causing Q[161] to be charged by EN1. Then, since Q[161] is pulled down to VGL, touch sensing periods do not bring about any different stress on T8 of the 161-st shift register from others. On the other hand, A161] keeps the pre-charged voltage during a touch sensing period.

In Fig. 11, A[161] shows some voltage drop at a falling transition of EN1 by the capacitor coupling at C1. The falling transition of EN1 pulls down Q[161], which causes the voltage drop at a floating A[161] through C1. However, this drop is not problematic since it is compensated for by a rising transition of EN1 after a touch sensing period. After the touch sensing is completed, Q[161] is re-charged while QB[161] is held on at a low level of VGL by low EN2. Then, V_g[161] is successfully generated through bootstrapping. In the end, Q[161] and V_g[161] are discharged by the pulse of V_g[162].

In the case of the 160-th stage, A[160] and Q[160] are pre-charged with V_g[159] and then, the pulse of V_g[160] takes place by bootstrapping Q[160]. Even though there is no pulse of V_g[161] until a touch sensing period ends, Q[160] and V_g[160] are pulled down by low EN1. After a touch sensing period, the activated V_g[161] discharges Q[160] and V_g[160] again.

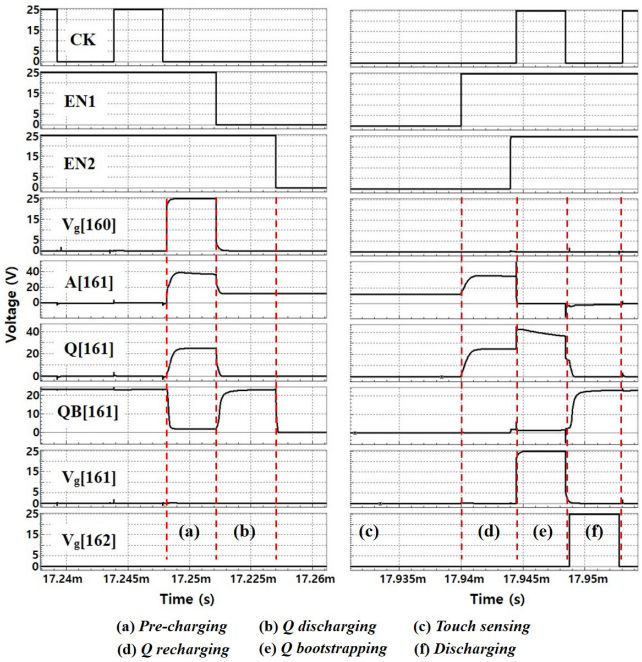

FIGURE 11. Simulated waveforms of a 161-st stage for a first shift register in a scanning period.

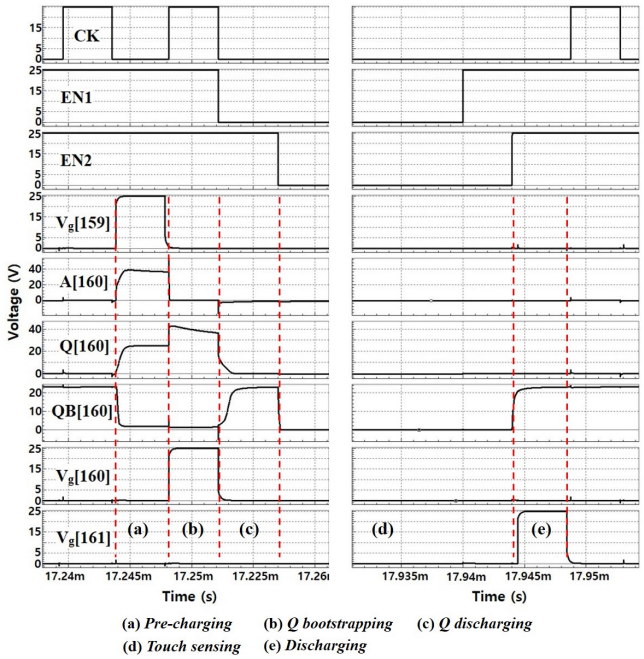

FIGURE 12. Simulated waveforms of a 160-th stage for a last shift register in a scanning period.

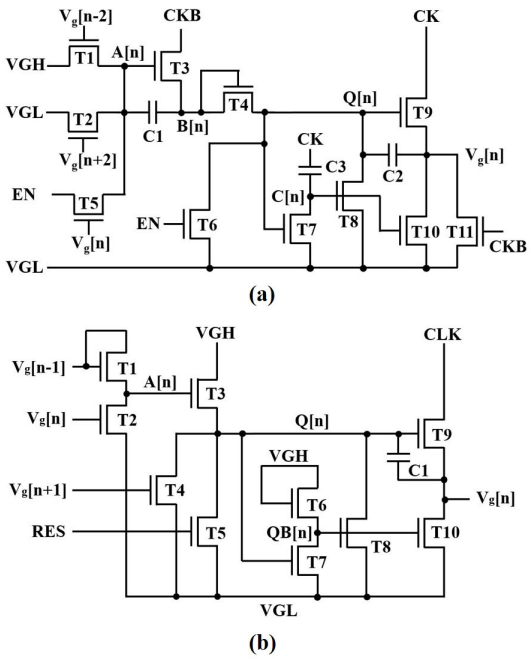

FIGURE 13. Schematics of previous shift registers (a) clock connection [15] (b) supply connection [16].

The proposed shift register is evaluated as to three performance metrics of V_{th} compensation range, coupling noise level, and power consumption along with two previous clock and supply connection methods of Fig. 13(a) and (b) [15], [16]. Two previous circuits are designed at the same backplane of a LTPS TFT with channel widths summarized in Table 2 and 3. While C1, C2, and C3 of a clock connection method are 0.5 pF, 2 pF, and 1.5 pF, C1 of a supply connection method is 1 pF.

TABLE 2. Channel widths of TFTs in a clock connection shift register [15].

TFT	Width	TFT	Width	TFT	Width
T1	10 μm	T2	10 μm	T3	10 μm
T4	10 μm	T5	10 μm	T6	10 μm
T7	100 μm	T8	10 μm	T9	1000 μm
T10	1000 μm	T11	10 μm		

TABLE 3. Channel widths of TFTs in a supply connection shift register [16].

TFT	Width	TFT	Width	TFT	Width
T1	10 μm	T2	10 μm	T3	50 μm
T4	10 μm	T5	100 μm	T6	10 μm
T7	200 μm	T8	10 μm	T9	1000 μm
T10	1000 μm				

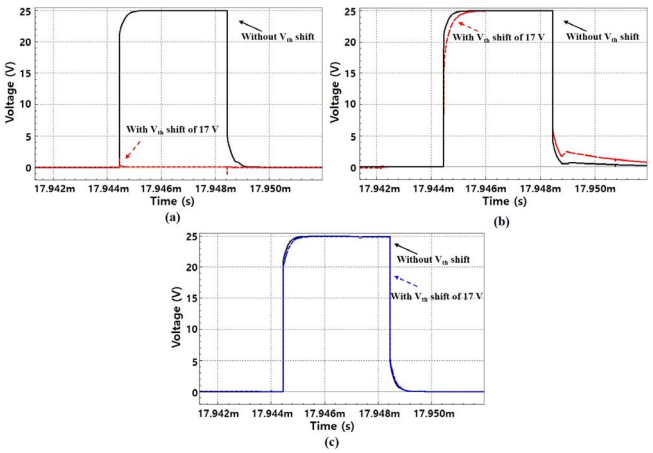

FIGURE 14. Output waveforms for V_{th} shift of 17 V in T3 (a) supply connection circuit [16] (b) clock connection circuit [15] (c) proposed circuit.

Proposed and clock connection methods can cover the V_{th} shift up to 17 V for T3 with which the supply connection circuit cannot generate the output pulse as shown in Fig. 14(a) to (c). Regarding coupling noise levels, supply connection scheme outperforms with -28.95 dB and the proposed circuit also shows the reduced noise level of -16.78 dB, compared to 2.37 dB of the clock connection method as fast Fourier transform (FFT) plots illustrated in Fig. 15(a) to (c). Lastly, the power consumptions are summarized in Table 4 for 160 stages including one touch sensing period. The power consumption of the

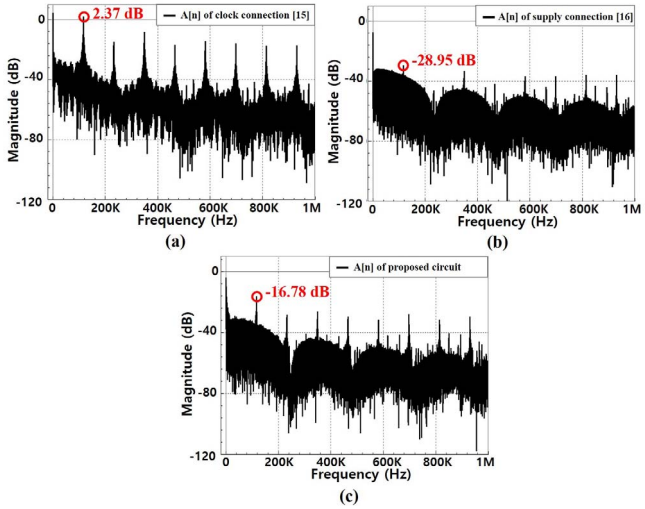

FIGURE 15. **FFT plots for coupling noise level of a first pre-charging node (a) clock connection [15] (b) supply connection [16] (c) proposed method.**

TABLE 4. **Power consumption at 160 stages of shift registers.**

	Clocks (mW)	VGH (mW)	EN [15], RES [16], EN1/EN2 (mW)	Total (mW)
Clock Connection [15]	12.77	0.010	0.0154	12.79
Supply Connection [16]	7.13	12.94	0.0016	20.07
Proposed	3.18	0.00026	1.2548	4.44

proposed circuit is substantially reduced to 4.44 mW, compared to 12.79 mW and 20.07 mW of two previous circuits.

IV. CONCLUSION

This paper demonstrates a low power and low noise shift register for in-cell touch display panels. In addition, the V_{th} non-uniformity issue of a pull-up TFT, T8, is resolved by employing two pre-charging nodes, A[n] and Q[n]. SPICE simulation with a n-channel LTPS TFT model has verified that the proposed shift register compensates for V_{th} shifts of T3 up to 17 V and reduces the coupling noise level to -16.78 dB compared to 2.37 dB of a clock connection scheme. Furthermore, the lowest power consumption of 4.44 mW is achieved at 160 stages of shift registers while 12.79 mW and 20.07 mW are dissipated in clock and supply connection methods.

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