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Enhancing Near-Infrared Photodetection Efficiency in SPAD With Silicon Surface Nanostructuration

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ABSTRACT We propose a straightforward technique to increase the near-infrared photo-detection efficiency (PDE) in single photon avalanche photodiodes (SPAD) manufactured in CMOS industrial foundries, without any change in the usual semiconductor process flow. The mask used for the photolithography of shallow trench isolation (STI) is modified to generate sub-wavelength patterns in the silicon area illuminated by incident light. The dimensions of the nanostructures are easily accessible by standard UV-lithography. The resulting improved anti-reflection effect and absorption in Si due to diffraction can provide up to 50% relative gain in PDE at 850-nm wavelength in simulation, while 25% gain is demonstrated in this paper, without degrading the median dark count rate (DCR) at ambient temperature. Some performance degradation is observed with the appearance of after-pulses, possibly due to the absence of surface passivation specific to the nanostructures in this first demonstration. The effect is angularly robust, relatively broadband, and relatively tolerant to fabrication errors. High PDE enables longer range or lower power consumption in applications for distance measurement with an active illumination, such as proximity sensing, 3-D ranging, or 3-D imaging.

INDEX TERMS Avalanche photodiodes, CMOS image sensors, CMOS process, nanophotonics, gratings, surface structures, optical diffraction.

I. INTRODUCTION

Single photon avalanche diodes are detectors of choice for applications with low light level and high temporal resolution [1]. Nowadays, silicon SPAD are mass-produced in CMOS technology with proven performances for proximity detection or 3D ranging in the near-infrared domain [2]. However, one limitation of system performance for next products is the PDE which is limited to a few percent, partly due to the relatively weak extinction coefficient of Si at these wavelengths and to the small thickness of active Si layer. To enhance the PDE, modifications of the SPAD internal structure have been proposed, by extending the depletion region [3] or the charge diffusion region in the Si [4]. This approach implies a complete revision of the SPAD technological process, less favorable operating conditions, and often compromises between the relevant performance parameters of the detector. The PDE can also be enhanced by fully optical ways, for example in 3D stacked SPAD by integrating a metal plate below the illuminated area to enable a double path of the light in Si [5].

In this study, we propose PDE improvement in SPAD formed in a bulk Si substrate by another optical approach [6]. Nanostructuring the Si surface can both improve the anti-reflection behavior compared to the thin film coating usually deposited on Si in image sensors, and diffract light inside the Si, which increases the photon path length and optical absorption within the depletion region. The operating principle is inspired by photon absorption management in thin solar cells [7] but it has been only recently applied to SPAD [8], by introducing a specific technological process. The surface of the semiconductor is usually considered highly critical as any modification of the surrounding process may directly impact the photodiode electrical performances, in particular, the DCR in SPAD. Interestingly, the patterning of Si in the optical path can be realized on a SPAD without any change in the technological process flow. A patterning step of Si surface is already present in the existing

process, the etching of STI around the Si active area, for electrical isolation [9], [10]. A simple modification of the STI mask enables to simultaneously form the STI and some patterns with sub-wavelength lateral dimensions. The etching depth of the conventional STI process is able to generate favorable optical effects. We target the least possible effort from the technological side, to enable a rapid implementation of the concept in SPAD industrial production. Section II presents the nanostructure optical design related to the SPAD characteristics and process constraints. In Section III, electro-optical characterization results are detailed, for the nanostructured SPAD and compared to reference SPAD, including PDE and DCR measurements.

II. DESIGN

The SPAD structure is similar to the original design of previous works [10], engineered for low DCR (median DCR $<$ 100Hz at room temperature), scalable lateral dimensions, and manufactured on 12 inches diameter substrates, in 130nm CMOS imaging technology (Fig. 1). The pn junction is about 0.8μm deep in Si between a p-well and a buried n-well implant region with retrograde doping profile. From TCAD simulations, the breakdown voltage is around 14V and the breakdown avalanche region is estimated to be between 0.7 and 1μm below Si surface. We denote by "avalanche triggering probability" or Pat(z), the probability that a photon, absorbed inside or outside the depletion region, will be detected. Pat is maximum in the depletion region, but it also extends outside, due to the diffusion or drift of minority carriers from the neutral regions to the depleted region. On the bottom side, the charge collection vanishes at around 1.7μm depth close to the second junction between the n-well and the lightly p-doped substrate. This limit in the depth of carrier collection minimizes the jitter to low values (typically 100ps) but also restrains the optical sensitivity and the PDE in the long wavelengths. This SPAD structure is considered as the reference in this work.

The geometry of the nanostructures (Fig. 1), is based on SiO_2 patches with 300nm depth spaced by Si in a 2D-periodic pattern in order to be independent of the light polarization. The grating period scales preferably, but not necessarily, between the wavelengths in the back-end oxide layers and in Si, to avoid/favor diffraction in reflection/transmission respectively. Interferences between the diffracted orders generate a 3D-interference pattern with horizontal periodicity and variable with the depth. The lateral dimensions of the oxide patches are optimized to position the interference lobes advantageously in or close to the avalanche region. This is why the knowledge of the Pat profile versus depth is of importance for the design of high PDE structures. Basically, PDE is the product of the optical absorption calculated by Rigorous Coupled Wave Analysis [11] and the Pat probability integrated over depth. The Pat profile is estimated by the best fit of the PDE spectral measurements (Fig. 2a) with a simple piece-wise linear function (Fig. 2b). The fit also takes into account the interference occurring

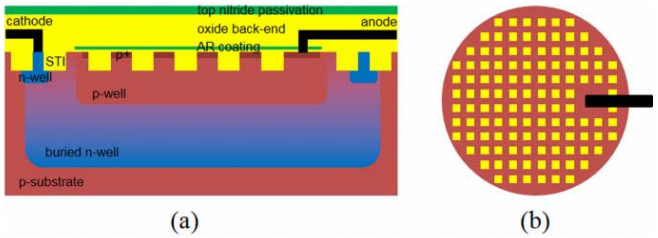

FIGURE 1. Cross-section (a) and top view (b) of a SPAD pixel with Si surface structured by STI holes.

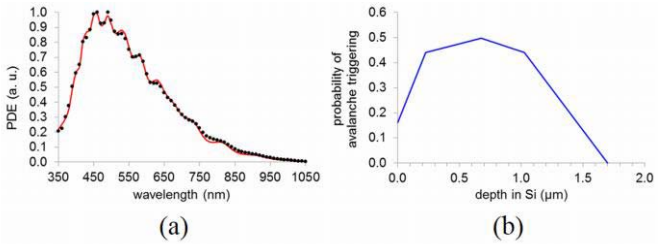

FIGURE 2. (a) Fit (red line) of the measured (black points) PDE on a reference SPAD without Si structuration, (b) Model of probability of avalanche triggering versus depth in Si, used as fitting parameters.

between nitride layers in the back-end stack and generating the high-frequency spectral oscillations observed in the PDE measurements. This approach of avalanche probability evaluation is a phenomenological alternative to the complete electro-optical modeling with the McIntyre formalism [12].

PDE gain is defined as the ratio between the PDE of the device under study and the reference PDE. The mapping of the PDE gain versus the lateral dimensions of the pattern, simulated at the 850nm working wavelength, has complex variations shaped by the existence of multiple diffraction orders depending on the grating period (Fig. 3a). However, some gain is observed compared to the conventional anti-reflective (AR) coating, nearly whatever the dimensions of the patterns. The maximum PDE gain is +55% for 310nm/160nm wide STI patches/Si spacings (design A) and benefits from a substantial improvement of the AR effect since the reflectivity of the grating at 850nm is below 0.1%, a value unattainable with the usual nitride unstructured AR coating (typically 5% with a bi-layer SiO_2/SiN). Instead, we select the second maximum with +45% PDE gain for 425/305nm lateral dimensions (design B), because the contribution of the optical absorption within the grating, close to the top Si interface, is expected to be lower. This may help making the SPAD insensitive to surface defects. For design B, the PDE gain is essentially obtained by diffraction in transmission, since the grating reflectivity is similar to the conventional AR coating.

The design is spectrally broadband with several maxima in the near infrared range beyond 700nm (Fig. 4), and angularly robust with PDE gain still high (+32%) at 25° incidence angle in average polarization.

In the modified STI level, square openings cover the whole surface of the 8μm diameter active silicon, except around

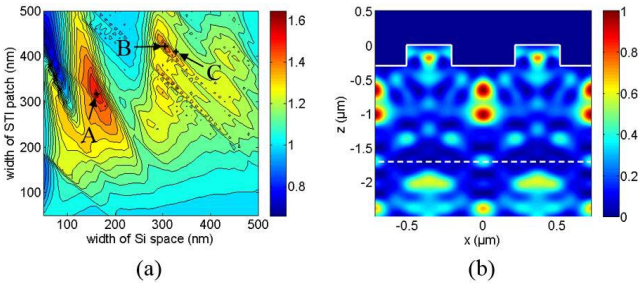

FIGURE 3. (a) PDE gain simulated versus lateral dimensions of nanostructures, (b) Squared modulus of light electric field (a. u.) simulated for design B, averaged in TE and TM polarizations, in a vertical cross-section centered on STI patches. The photosensitive region extends between the Si/SiO_2 interface (white plain line) and the top of the deep depletion region (dashed line).

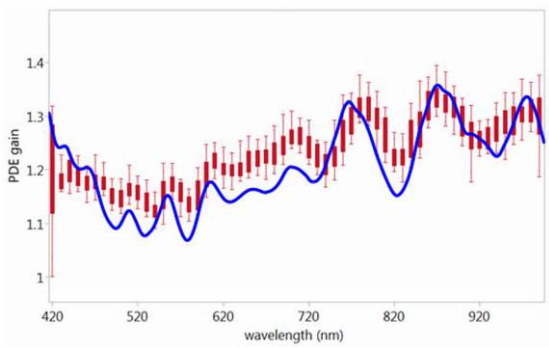

FIGURE 4. Spectral variations of PDE gain simulated (blue curve) for measured dimensions of nanostructures, corresponding to design C shown in Fig. 3a, and spectral PDE gain measured (red graph) on 24 nanostructured/reference couples of SPAD over the 12" wafer surface, at 0.6V excess bias voltage and ambient temperature. Thick/thin bars respectively represent standard deviation/extreme values.

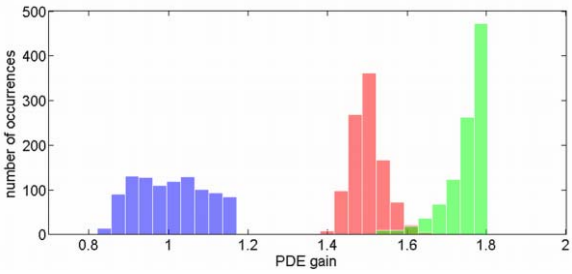

FIGURE 5. Simulated histograms of PDE gain at 850nm for reference SPAD with complete back-end stack (blue), nanostructured SPAD design B with complete back-end stack (red) and with elimination of top nitride layer in back-end stack (green). The statistics are calculated over 1000 cases with independent thickness variations of the 12 back-end layers and STI depth corresponding to process errors with Gaussian distribution and standard deviation of 3 to 5%.

the anode. The standard SPAD fabrication process is applied including Si dry etching for the simultaneous formation of STI and optical patterns, followed by high temperature annealing for surface passivation, SiO_2 gap-filling and planarization by chemical-mechanical polishing. The usual nitride AR coating is then realized over the Si. Although not really necessary in the optical design, it is used as an etching stop layer in the technological flow.

III. RESULTS AND DISCUSSION

The breakdown voltage measured at room temperature on structured SPAD (14.1V) was slightly higher than the reference SPAD (13.9V), probably due to a small variation of the implantation depth through the STI. The PDE of both types of SPAD were measured at 0.6V excess bias voltage over the visible and near infrared range on 24 chips over the wafer surface. The average value of absolute PDE at 850nm is 4.6% for the reference SPAD. PDE enhancement is clearly observed with the structured SPAD, with an average gain of +25% at 850nm (Fig. 4). The PDE gain is lower than expected for several reasons. First, the profile of the patterns is not perfectly straight with a 7° angle from vertical. The design is not very sensitive to the slope itself, but the trapezoidal STI holes have 30nm smaller width than the target design (design C in Fig. 3a). This systematic error can be easily anticipated in the mask layout in future trials. Second, the variations on thickness and refractive index of the back-end layers in the standard CMOS technology induce some dispersion of the PDE. This is because the intensity of light entering the Si, and hence the PDE, depend on the multiple reflections in the back-end stack, as evidenced by the oscillations in the PDE gain spectrum (Fig. 4). The simulated dispersion on the PDE is already present on the reference SPAD but does not degrade on the nanostructured SPAD (Fig. 5), since the dispersion on STI holes dimensions is not the major contribution. Removing the top nitride layer after the final imager annealing by a single additional etching step would further enhance the PDE up to +80% (Fig. 5).

Although the median DCR measured at 0.6V excess bias voltage and room temperature was about 40Hz for both reference and structured SPAD, we observed a decrease of the DCR for some part of the overall SPAD population on a wafer. This is visible in Fig. 6a, where for example the third quartile of the structured SPAD devices is lower than the reference. This suggests that the DCR is influenced by the process at the surface, far from the junction. From the nonzero PDE in UV wavelengths (Fig. 2a), it is already clear that charges generated close to the Si surface can generate an avalanche. The quality of the surface passivation is not equal in standard p-doped surface and under thermal oxide of STI surface. This is probably the origin of DCR variations. DCR is even more decreased in other tests with Si etching all over the active surface of Si to form an STI sheet.

However, on the structured SPAD, we observe a 6% rate of after-pulses detected at minimum inter-pulse time fixed at 5ns in the measurement setup, in contrast with the reference SPAD that is almost not affected by after-pulsing. This is evidenced by the deviation from the Poisson fit law (Fig. 6b). It seems that the Si/SiO_2 STI interface induces after-pulsing. The generation of after-pulsing with traps located outside the depletion region is not well understood at this stage [13]. Future runs with specific passivation of the Si surface may both help to understand and minimize the after-pulses.

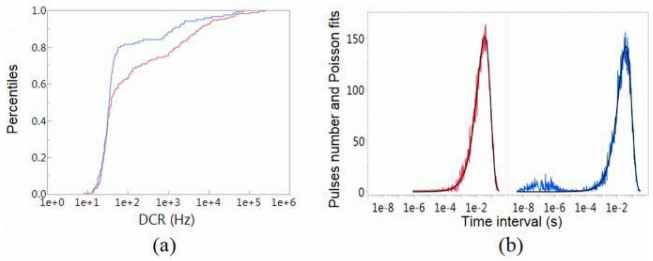

FIGURE 6. (a) DCR cumulative distributions of reference SPAD (red), and nanostructured SPAD (blue) on a wafer, (b) typical time interval histograms measured in the dark on a reference (blue) and a structured SPAD (red), Poisson distribution fits are plotted in black lines.

IV. CONCLUSION

In this study, we tried to address the challenge of improving the PDE of thin CMOS SPAD without any modification of the current technological process flow and Si thickness. We introduced sub-wavelength patterning on the active Si surface with a simple modification of the STI mask, and measured a modest but significant +25% relative increase of PDE at 850nm wavelength together with a reduction of DCR compared to the unstructured reference SPAD, but also observed a 6% after-pulse rate. A few additional processing steps, specific STI passivation and etching of nitride layer in the back-end stack, may finally be necessary in next developments to suppress the after-pulses and further enhance the PDE up to +80% along with a reduced sensitivity to manufacturing process error dispersion. In addition, applying the concept on a SPAD implemented in Silicon-On-Insulator substrate is expected to provide much higher PDE gain, typically several-fold improvement [14], [15].

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