Received 17 August 2017; revised 31 October 2017 and 10 January 2018; accepted 17 January 2018. Date of publication 28 February 2018; date of current version 26 April 2018. The review of this paper was arranged by Editor H. Wakabayashi.

Digital Object Identifier 10.1109/JEDS.2018.2808494

Nano-Structure-Controlled Very Low Resistivity Cu Wires Formed by High Purity and Optimized Additives

JIN ONUKI [1], KUNIHIRO TAMAHASHI [1], TAKASHI INAMI [1], TAKATOSHI NAGANO [1], YASUSHI SASAJIMA [1], AND SHUJI IKEDA [2] (Fellow, IEEE)

1 Graduate School of Science and Technology, Ibaraki University, Hitachi 316-8511, Japan
2 Tsukuba Reseach Laboratory, Tei Solutions, Tsukuba 305-0053, Japan

CORRESPONDING AUTHOR: J. ONUKI (e-mail: jin.ohnuki.jn@vc.ibaraki.ac.jp)

This work was supported in part by the Japan Science and Technology Agency under Grant JST-AS2525014J, and in part by the Grants-in-Aid for Scientific Research under Contract 17206071 and Contract 20226014.

ABSTRACT Resistivity increase in nano-level Cu wires is becoming a critical issue for high speed ULSIs. We have established a new manufacturing process utilizing very high purity 9N electrolyte and optimized additives to control nano-structures of Cu wires, and we realized Cu wires for practical use with 50% lower resistivity than those made with the conventional process. Using STEM analyses and phase field simulation, we also ascertained the reason for getting the very low resistivity Cu wires.

INDEX TERMS High purity electrolyte, nano-structure controlled Cu wire, optimized additives, low resistivity.

I. INTRODUCTION

Cu wire resistivity increase due to miniaturization is a crucial and shared issue to be solved among leading LSI manufacturing companies. Researchers [1]–[3] have worked on the thinning of high resistivity barrier metals. Replacement of high resistivity barrier metals with low resistivity barrier metals like Ru has also been investigated [4]. However, the area percentage of barrier metals to the entire Cu wire area is less than 20%. This means that thinning barrier metals is not so effective against resistivity increase. Hence, a decrease in resistivity in Cu wires (Cu core) is much more important.

Resistivity increase in narrow Cu wire has been reported to be caused by electron scattering not only at grain boundaries but also at surface and sidewalls [5].

We have been insisting that the resistivity increase of very narrow Cu wires is due to electron scattering at very small grain boundaries of around 50nm [6]. Recently, grain boundary scattering in the Cu core was shown to be the dominant factor for the resistivity increase [7]. Hence, the objective for our study was to lower electron scattering at grain boundaries by nano-structure control of the Cu core, i.e., enlargement and homogenization, leading to very narrow Cu wires with much lower resistivity than those of conventional Cu wires.

II. HYPOTHESIS FOR LOW RESISTIVITY CU WIRES

In order to reduce resistivity, we thought lowering of electron scattering at grain boundaries by enlargement and homogenization as shown in Fig. 1 is mandatory.

III. EXPERIMENTAL PROCEDURES

A. TEG STRUCTURE AND ELECTROPLATING

The TEG (test element group) structure is shown in Fig. 2(a). The trench width was from 50nm to 100nm and trench depth was 200nm. Ta and TaN were sputter deposited at layer thicknesses of 8nm and 5nm in this order. Cu seed layer was also sputter deposited at thickness of 20nm. Fig. 2(b) shows a schematic set-up of the electroplating equipment. The 10mm x 10mm chip was attached on its reverse side to a rotating electrode. Rotating speed was fixed as 1000rpm. The purities of Cu electrolytes were conventional 6N and 9N. Additives, like accelerator and suppressor, were used according to the standard specification. Leveler was also used according to the standard specification and it was varied in quantity as well, i.e., at 1/5, 1/10, and 1/20. Current density of 5mA/cm^2 was applied to chips during plating. Furthermore, Cu wires were also formed in a 12-inch wafer

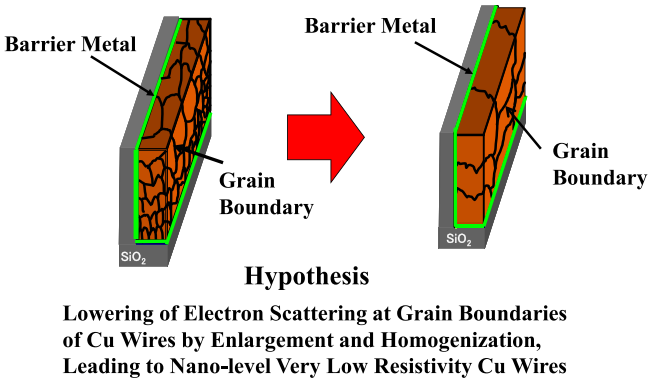


FIGURE 1. Concept for Low Resistivity Narrow Cu Wires.

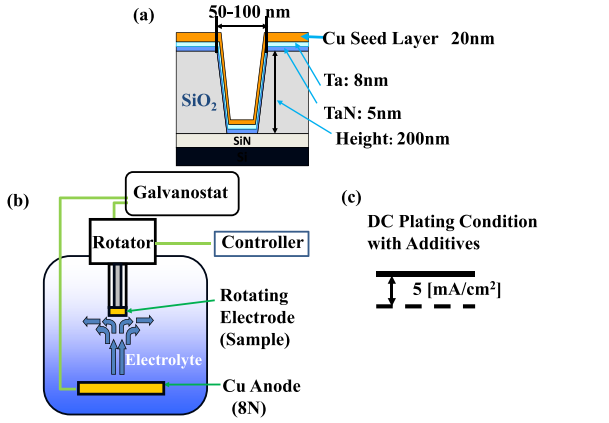


FIGURE 2. TEG Structure and Electroplating Condition.

to confirm the effectiveness of the newly developed process on the resistivity.

B. ANNEALING AND CMP

After plating, the chip and wafer were heated to 573K and kept for 10min in N_2 atmosphere to enhance grain growth of Cu wires. After annealing, CMP (chemical mechanical polishing) was done using slurries, manually for the chip and automatically for the 12-inch wafer, to remove excess Cu.

C. MICROSTRUCTURAL ANALYSES USING CS-CORRECTED STEM AND X-RAY DIFFRACTION

Microstructural analysis along the longitudinal direction was done using Cs (spherical aberration-corrected) STEM as shown in Fig. 3. STEM observation along the longitudinal direction shows grain size distributions in the Cu wires explicitly [8].

Fig. 4 shows grain size measurement results of Cu wires obtained using X-ray diffraction. Fig. 4(a) shows diffraction patterns from Cu powder. We see many peaks from (111), (200), (310), and (222) Cu planes. For Cu wire, only (111) and (222) Cu planes are obtained. Grain size distributions were measured using these two peaks [9].

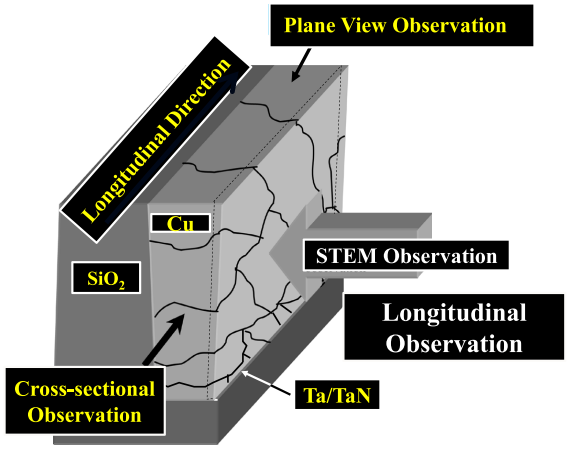


FIGURE 3. Reproduced Image Showing Appearances of the Cu Wire and STEM Observation along the Longitudinal Direction.

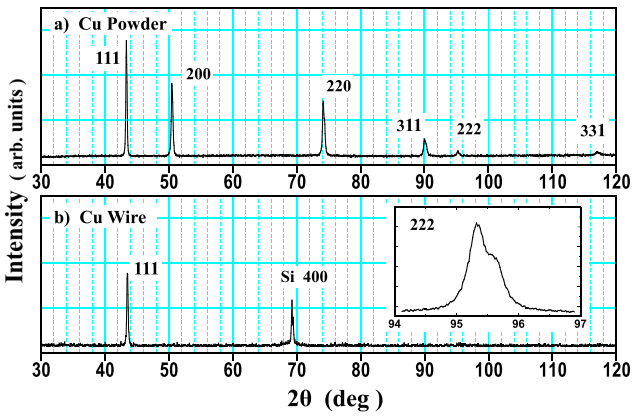


FIGURE 4. X-ray Diffraction Patterns for (a) Cu Powder and (b) Cu Wire.

IV. RESULTS AND DISCUSSION

A. INVESTIGATION OF UNIFORM GRAIN SIZE ENLARGEMENT PROCESS

A.1. RESISTIVITY OF CU WIRES AS A FUNCTION OF LINE WIDTH MADE BY PLATING USING CONVENTIONAL 6N ELECTROLYTE AND STANDARD ADDITIVES IN CURRENT USE

Fig. 5 shows resistivity of Cu wires including barrier metals consisting of Ta and TaN as a function of line width. 6N Cu electrolyte and three kinds of additives, i.e., accelerator, leveler and suppressor were used. Resistivity increased with the decrease of line width and becomes about 5.8 $\mu\Omega \cdot$ cm when width is 50nm.

Fig. 6 shows a STEM image around grain boundaries in the longitudinal cross-sectional direction of 60nm wide Cu wire made by plating with conventional Cu electrolyte and standard additives. We see many impurities, indicated by pink arrows, of 5nm to 10nm diameter along the grain boundaries. From line analysis, we found these impurities include O, Cl, and Fe as shown in this Fig. Using the ab initio calculation, we found that FeClO is more stable at

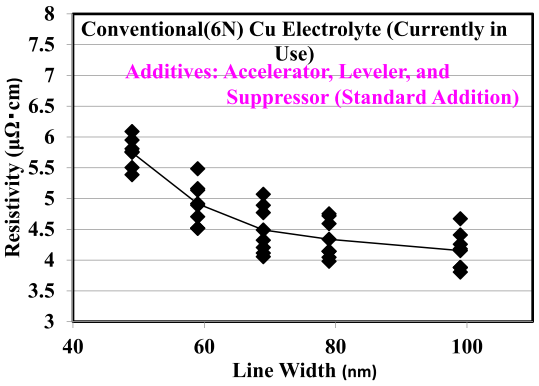


FIGURE 5. Resistivity as a Function of Line Width.

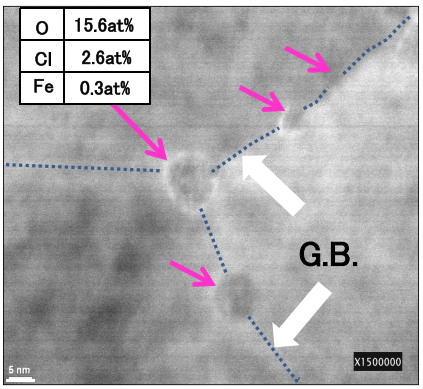


FIGURE 6. STEM Image around Grain Boundaries (White arrows indicate Grain Boundaries, while red arrows indicate impurities).

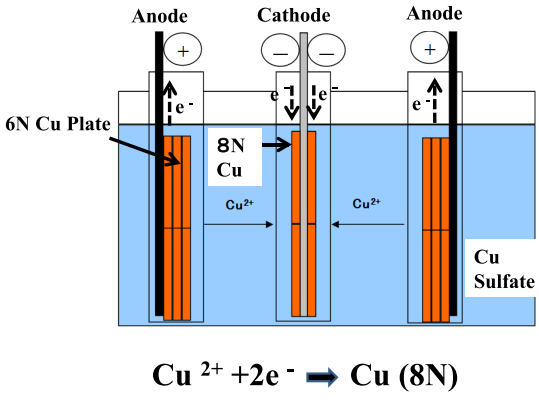
grain boundaries than at inside of grains. These FeClO can pin the grain growth during annealing [10].

The effect of C on grain size and resistivity of Cu films was investigated [11], [12], and the Cu films with higher C concentration were found to have higher resistivity with smaller grain size.

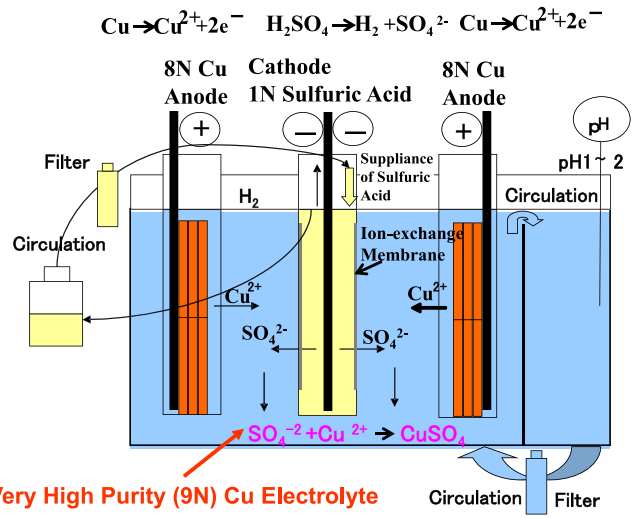
A.2. PURIFICATION OF CU ELECTROLYTE FROM 6N TO 9N

We have developed high purity Cu electrolyte through an electrolytic method. At first, 6N Cu plate was dissolved into sulfuric acid electrochemically and precipitated onto a cathode as 8N Cu as shown in the reaction equation of Fig. 7(a).

Next, we made 9N Cu electrolyte by electrolytic dissolution of 8N Cu into high purity sulfuric acid solution as shown in Fig. 7(b).



(a)



(b)

FIGURE 7. (a) High Purity 8N Cu Plates by Electric Methods. (b) Manufacturing Method of Very High Purity 9N Cu Electrolyte by Electrolytic Dissolution of 8NCu Plate into High Purity Sulfuric Acid Solution.

B. GRAIN SIZE MINIATURIZATION PROCESS TO UTILIZE HIGH GRAIN BOUNDARY ENERGY FOR GRAIN GROWTH DURING ANNEALING

Next, we investigated grain size miniaturization process in as-deposited Cu films formed both by conventional 6N and 9N electrolytes to utilize high grain boundary energy [13]. Fig. 8 shows mean grain size before annealing as a function of leveler content for Cu wires formed with conventional and 9N electrolytes obtained by X-ray diffraction. Two other additives like accelerator and suppressor were the standard addition. Mean grain size decreases with the decrease of leveler content and becomes less than 30nm when leveler content is 1/10 of the standard addition independent of electrolyte purity. This result is considered to be due to the fact that the number of Cu nucleation sites increases with the decrease of leveler.

Fig. 9 shows mean grain size of Cu wires made with conventional and 9N electrolytes as a function of leveler content after annealing at 300°C for 0.5h. Mean grain size is increased by the decrease of leveler content for both electrolytes. However, mean grain size of Cu wires made with 9N electrolyte is much larger than that of Cu wires made by conventional electrolyte even if original grain size was almost the same. This result suggests to us that the amount of impurities at the grain boundaries of Cu wires formed by

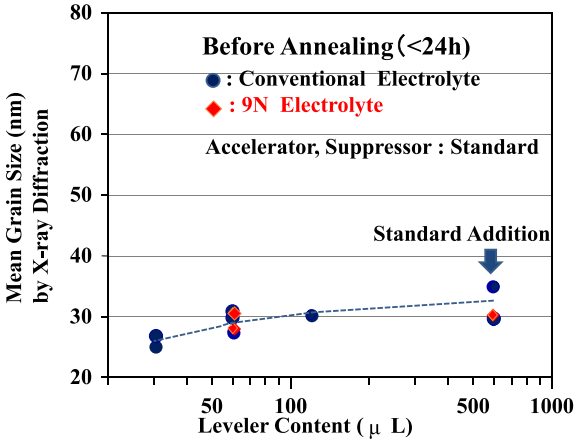


FIGURE 8. Mean Grain Size by X-ray Diffraction as a Function of Leveler Content for Cu wires made by Plating with Conventional 6N and 9N Electrolytes before Annealing.

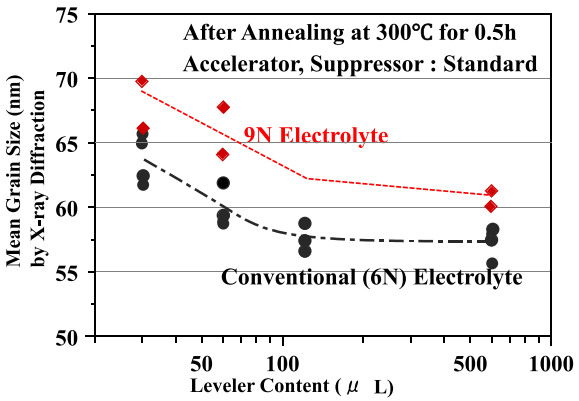


FIGURE 9. Mean Grain Size by X-ray Diffraction as a Function of Leveler Content for Cu wires made by Plating with Conventional 6N and 9N Electrolytes after Annealing.

9N electrolyte was much lower than that of Cu wires formed by conventional electrolyte.

To confirm our hypothesis, we analyzed the atomic concentrations of Fe, Cl and O on the grain boundaries by EDX. We found that concentrations of Fe and Cl in grain boundaries of Cu wires made with 9N electrolyte with 1/10 leveler are much lower than those of Cu wires made with 6N electrolyte with standard additives. However, atomic concentrations of O in the two Cu wires are almost the same.

C. COMPARISON OF GRAIN SIZES AND RESISTIVITY BETWEEN CU WIRES FORMED BY 6N ELECTROLYTE WITH STANDARD ADDITIVES AND 9N ELECTROLYTE WITH 1/10 LEVELER

Fig. 10 shows the comparison of grain sizes between 50nm Cu wires plated with (a) 6N Cu electrolyte with 3 kinds of standard additives and (b) 9N Cu electrolyte with additives of 1/10 leveler and 2 other kinds of standard additives. It is clear that Cu wire with large homogeneous grains forms by newly developed plating process. Average grain size for

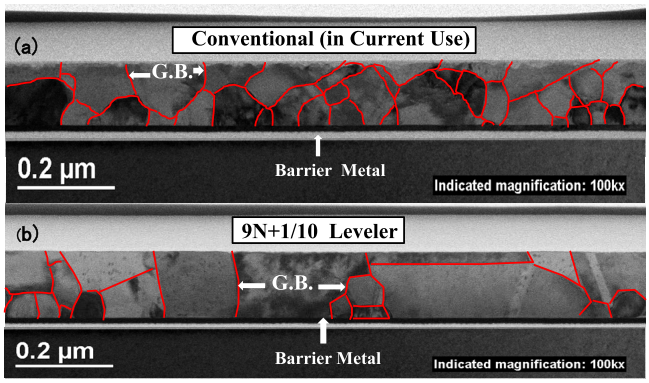


FIGURE 10. Comparison of Grain Sizes between Cu Wires Plated with (a) Conventional Cu Electrolyte with 3 Kinds of Standard Additives and (b) 9N Cu Electrolyte with Additives of 1/10 Leveler and Other 2 Kinds of Standard Additives. (a) Average Grain Size: 50nm (b) Average Grain Size: 80nm.

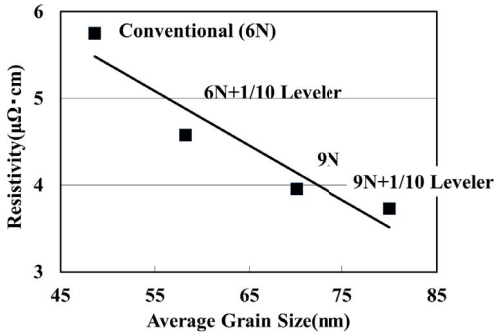


FIGURE 11. Effect of Average Grain Size on Resistivity of Cu Wires.

conventional process is 50nm, while that for new process is 80nm.

Fig. 11 shows the effect of average grain size on the resistivity of 50nm wide Cu wires. Resistivity of Cu wires decreases with the increase of average grain size. Resistivity of Cu wires made by 9N + 1/10 leveler is $3.7\mu\Omega \cdot$ cm and that of the conventional process is $5.8\mu\Omega \cdot$ cm.

D. GRAIN GROWTH MECHANISM OF CU WIRES

We investigated the grain growth mechanism of Cu wires by using phase field simulation. Fig. 12(a) shows grain boundaries of two-dimensional Cu wire simulation models before annealing. The average grain size is set as 40nm. Fig. 12(b) shows grain boundaries of two-dimensional Cu wire simulation models after annealing at 300°C for 10min. In this case, all grains of the Cu wire before annealing were assumed to be pinned by impurities during annealing. It is clear that grain growth did not occur after annealing based on a comparison of grain size distributions of Fig. 12(b) with those of (a).

Fig. 12(c) shows grain size distributions after annealing for 50% of the Cu grains are pinned by impurities during annealing. We see large grains are obtained after annealing by reducing impurities at the grain boundaries. Fig. 12(d) corresponds to the case of 5% of the grains being pinned by

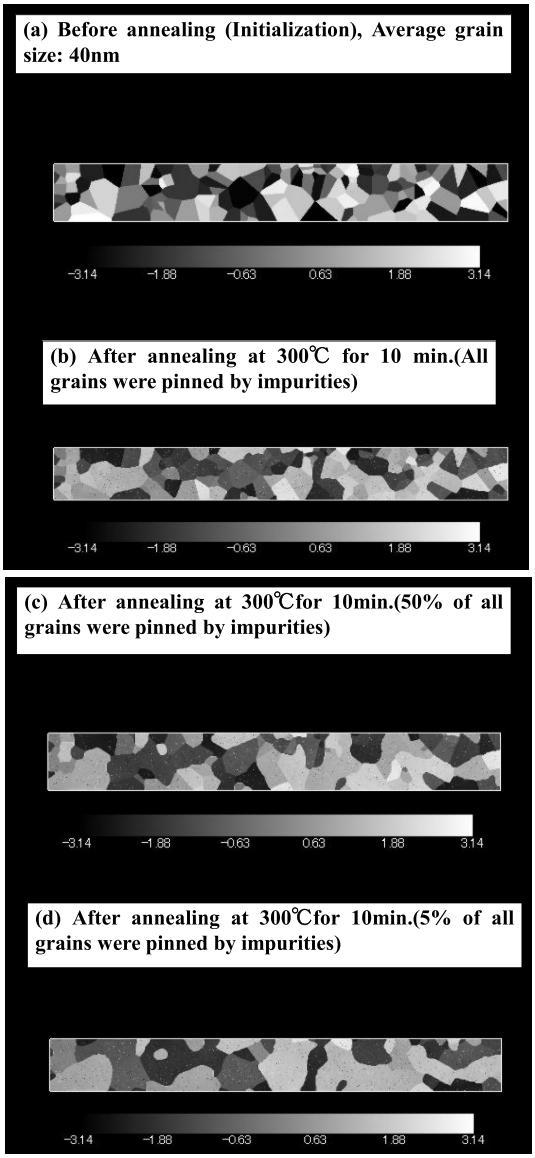


FIGURE 12. **(a)(b) Grain Boundaries of Two Dimensional Cu Wire Simulation Models. (c)(d) Grain Boundaries of Two Dimensional Cu Wire Simulation Models.**

impurities during annealing. If we compare grain size distributions in (d) with those of grain sizes shown in STEM images of Cu wires formed with 9N electrolyte with 1/10 leveler, almost the same grain size distributions are realized (see Fig. 10 (b)).

E. VERIFICATION OF RESISTIVITY OF CU WIRES FORMED BY THE NEWLY DEVELOPED PROCESS USING 12-INCH WAFER

As the next step, we expanded the newly developed process to form Cu wires in a 12-inch wafer to confirm applicability of high purity Cu electrolyte with optimum additives to produce very low resistivity Cu wires comparable to the Cu wires in a chip. Fig. 13 shows resistivity of Cu wires formed in 12-inch wafer by conventional 6N electrolyte

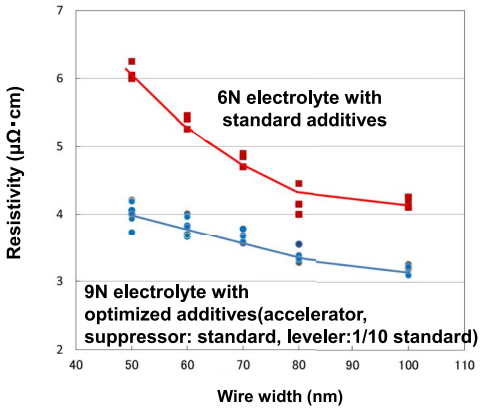


FIGURE 13. **Resistivity of Cu wires formed in 12 inch wafer by conventional and the new developed processes as a function wire width.**

with standard additives and 9N electrolyte with 1/10 leveler (accelerator and suppressor: standard). Resistivity of both wires increases with the decrease of line width. However, resistivity of Cu wires made by the new process is much lower than that of Cu wires made by the conventional process.

V. CONCLUSION

We clarified that grain growth of Cu wires is reduced by the pinning effect of Fe (ClO) compounds at grain boundaries based on results of a nano-order analysis of Cs-corrected STEM observations and a phase field simulation of Cu wires made using conventional Cu electrolyte. We also developed a uniform enlargement process of grain sizes in Cu wires by (a) using very high purity 9N Cu electrolyte and (b) optimizing additives. Very high purity 9N Cu electrolyte and optimization of additives reduced impurity content in Cu film, thus leading to a drop in the amount of Fe (ClO) compounds at the grain boundaries. Optimization of additives caused miniaturization of grain sizes of as-deposited Cu wires, thus leading to large grain size after annealing utilizing large grain boundary energy. By combining 9NCu electrolyte with additive optimization, we realized Cu wires with 1.6 times larger grain sizes and 50% lower resistivity than those of Cu wires made by conventional Cu electrolyte.

Furthermore, we confirmed applicability of high purity Cu electrolyte with optimum additives to get very low resistivity Cu wires in the 12-inch wafer comparable to the Cu wires in a chip. We investigated grain growth behaviors as a function of boundary pinning ratio by phase field simulation during annealing, and found the large and uniform grain size Cu wires obtained by the new process were reproduced when the impurity existing ratio at the grain boundary was lower than 5%.

ACKNOWLEDGMENT

The authors would like to thank lab member, Mr. A. Chiba and graduate students, Mr. T. Miyamoto and Mr. T. Saginoya, for their great contributions to this presentation. They also

would like to thank Prof. K. Kondo of Osaka Prefectural University, Mr. T. Ishigami and T. Nakamura of Kusaka Rare Metal Products, Mr. S. Yoshida of Toshiba Corp., Associate Prof. K. Mimura, Assistant Prof. M. Uchikoshi of Tohoku University, Dr. N. Ishikawa of NIMS, and Mr. T. Majima of JST for their encouragement and valuable discussions.

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JIN ONUKI received the M.S. degree in materials science from Tohoku University, Sendai, Japan, in 1974 and the Ph.D. degree in electronic engineering from Hokkaido University, Sapporo, Japan, in 1984. In 1974, he joined Hitachi Research Laboratory, Hitachi Ltd., where he was engaged in the research and development of interconnecting materials. Since 2003, he has been engaged in research of low resistivity Cu interconnects in ULSI's as a Professor with Ibaraki University, Hitachi, Japan, where he is currently a Professor Emeritus. He has published over 140 technical papers and authored six books.

KUNIHIRO TAMAHASHI received the M.S. degree in metallurgical engineering from Tohoku University, Sendai, Japan, in 1973 and the Ph.D. degree in electronic engineering from Osaka Prefecture University, Osaka, Japan, in 2001. In 1973, he joined Hitachi Research Laboratory, Hitachi Ltd., where he engaged in the research and development of photoreceptor drum materials for high speed laser beam printers, such as amorphous selenium and hydrogenated amorphous silicon thin films. In 2001, he moved to Katsuta Research Laboratory, Hitachi Koki Ltd., Katsuta, Japan, where he engaged in the research and development of reliability and quality enhancement for dot printers and PZT materials of ink jet printers. From 2008 to 2017, he was a Researcher of Industry-University Cooperation with Ibaraki University, Hitachi, Japan, where he engaged in the research of low resistivity Cu interconnects materials of ULSI's.

TAKASHI INAMI received the M.S. degree in physical metallurgy from Ibaraki University, Hitachi, Japan, in 1975 and the Ph.D. degree in ferrous processing metallurgy from Tohoku University, Sendai, Japan, in 2002. In 1975, he joined the Faculty of Engineering, Ibaraki University, where he engaged in the research of kinetic and morphological analysis of iron oxide reduction. Since 2007, he has been engaged in the research of grain size evaluation of narrow Cu interconnects using X-ray diffraction method as an Associate Professor with Ibaraki University. He has published 26 technical papers.

TAKATOSHI NAGANO received the M.S. and Ph.D. degrees in mechanical engineering from Meiji University, Tokyo, Japan, in 1998 and 2001, respectively. In 2002, he joined the Ibaraki University, Hitachi Ltd., where he engaged in the research the material science engineering using the *ab initio* calculation, especially ferrite alloy with the impurities. In 2011, he began research in low resistivity Cu interconnects in ULSI's Hitachi, Japan.

YASUSHI SASAJIMA received the M.E. and Ph.D. degrees in materials science from Tokyo University, Tokyo, Japan, in 1986 and 1992, respectively. In 1986, he joined Ibaraki University, Hitachi, Japan, where he engaged in the research of computer experiments of materials, especially film formation process and structure of nanomaterials. In 2007, he began research in computer experiments of grain growth process of Cu interconnects in ULSI's as a Professor with Ibaraki University. He has published 80 technical papers and authored two books.

SHUJI IKEDA (F'04) received the B.S. degree from the Tokyo Institute of Technology, Tokyo, Japan, the M.S.E.E. degree from Princeton University, NJ, USA, and the Ph.D. degree from the Tokyo Institute of Technology. He is the CEO of Tei Solutions Inc. He joined Hitachi, Japan, in 1978, where he was engaged in research and development of state-of-the-art SRAM process and devices. He was also working on developing process technology for LOGIC, embedded-memories, and RF devices. In 2005, he joined SEMATECH/ATDF, where he developed various kinds of technologies including scaled CMOS, nonclassical CMOS, and new materials/tools. He established tei Technology, TX, USA, in 2008 and tei Solutions Inc. in Japan in 2010. He holds over 200 patents in Japan and over 70 patents in the U.S. He chaired IEDM in 2002 and EDTM in 2017. He chairs VLSI Technology and Circuits committee of EDS from 2009 and serve as an EDS BoD member from 2017.