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Advanced FDSOI Device Design: The U-Channel Device for 7 nm Node and Beyond

RAMACHANDRAN MURALIDHAR^{ID}, ROBERT H. DENNARD, Life Fellow, IEEE,
TAKASHI ANDO^{ID}, ISAAC LAUER, AND TERENCE HOOK

IBM T. J. Watson Laboratory, Yorktown Heights, NY 10598 USA

CORRESPONDING AUTHOR: R. MURALIDHAR (e-mail: muralidr@us.ibm.com)

This paper is based on a paper entitled "Advanced FDSOI Design: The U-channel Device for 7nm Node and Beyond" presented at the 2017 IEEE S3S Conference.

ABSTRACT In this paper, we propose the extendibility of ultra-thin body and box (UTBB) devices to 7 and 5 nm technology nodes focusing on electrostatics. A difficulty in scaling traditional UTBB is the need for SOI scaling to about one fourth of the gate length. We propose a U-channel fully depleted silicon on insulator architecture that starts off with a thicker SOI (8–11 nm) and has a U-shaped channel enabled by a recessed metal gate. This device improves the electrostatics by increasing the overall gate length at fixed metal gate opening, mitigating drain field coupling to the source due to the recessed metal gate region and having thin SOI below the center of the device (4–5 nm). Modeling shows that good electrostatics can be maintained at small metal gate opening to enable pitch scaling. This device provides lower cost options for mobile and IOT technologies.

INDEX TERMS UTBB, U-channel, TCAD, multiple thresholds.

I. INTRODUCTION

In order to scale MOSFETs to 7 and 5 nm nodes with 30–40 nm gate pitch, aggressive gate length scaling to 12–14 nm is required. Of paramount importance is the electrostatic integrity at such short gate lengths as it is significantly influenced by drain induced barrier lowering (DIBL). Possessing good subthreshold slope and DIBL are critical for good overdrive and hence device switching speed. The industry has adopted FinFET technology in the 22 nm [1] and 14 nm technology nodes [2], [3]. Scale length theory [4], [5] shows that FinFETs can provide gate length scaling by reducing fin thickness, D_{fin} , and it is expected that more advanced nodes will be enabled by continued D_{fin} and fin pitch scaling. However, in addition to process complexities with making tall thin fins and cost associated with process integration, FinFETs are limited in enabling multiple device thresholds for power-performance optimization without the use of multiple work function metals and, as such, are not optimal for growing IOT and mobile markets.

Planar ultra-thin body and box (UTBB) [6]–[8] fully depleted silicon on insulator (FDSOI) devices have many advantages for future low-cost energy-efficient applications.

However, process steps for scaling to ultra-thin FDSOI devices can be difficult to control, and extrinsic resistance can hinder any performance improvement. In this paper, we present a novel planar U-channel UTBB FDSOI device that can alleviate these problems.

Figure 1 summarizes the salient features of FDSOI technology variants in production and as reported in research publications, along with the extension proposed herein. Improvements in access resistance have been accomplished through improved epitaxy techniques and activation anneals [6], [7], [9], [10]. Channel conductance has been primarily addressed directly through strain engineering [9], [10]. While reduction of the silicon thickness (and secondarily the BOX thickness) has enabled scaling of the channel length, further reduction of the silicon thickness below 5nm is problematic due to quantum effects, mobility degradation, and the need to form the source/drain epitaxy after the gate stack etch. Therefore, additional scaling beyond the '10nm node' requires a new approach. In this paper we propose a modified device structure – the U-channel device – that addresses basic scaling issues and enables superior performance at reduced gate pitch for extension to future nodes.

"Node"	28nm	22nm	14nm	10nm	Proposed
Lgate	24nm	est. 24nm	20nm	20nm	< 20nm
Tsi	7nm	< 7nm	6nm	< 5nm	U-Channel
BOX	25nm	est. 20nm	25nm	< 20nm	< 20nm
Gate	Gate first HKMG	Gate first HKMG	Gate first HKMG	Gate first HKMG	Gate last HKMG
N-Channel	Si	Si		Strained Si	Strained Si
P Channel	Si	SiGe	SiGe	SiGe	SiGe
N S/D	Implanted	In-situ Si:P	In-situ Si C:P	ISDP	ISDP
P S/D	Implanted	In-situ SiGe:B	In-situ SiGe:B	ISDB	ISDB
BackGate				Dual STI	Dual STI
Reference	8	7	6	9,10	

FIGURE 1. Salient features of FDSOI technology variants in production and as reported in research publications, along with the extension proposed herein.

II. U-CHANNEL FDSOI DEVICE FEATURES

Figure 2 contrasts a conventional UTBB device with the proposed U-channel device.

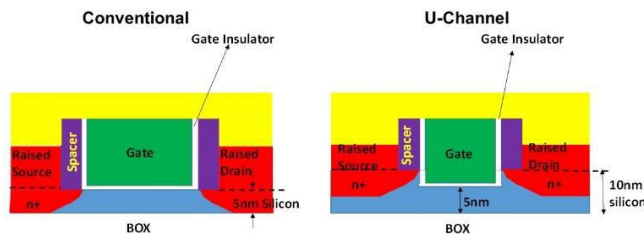


FIGURE 2. On left a conventional FDSOI device with starting SOI thickness of 5nm and on right a U-channel FDSOI with starting SOI thickness of 10nm and gate recessed by 5nm.

Unlike the conventional device, the U-channel device has a recessed gate region below the source/drain extension regions under the spacers. This allows a thicker starting SOI and provides a thin SOI layer in the part of the channel region under the recessed gate. This device construct is enabled by advances in High-k Metal Gate (HKMG) gate-last replacement gate technology. The device fits into a much smaller gate pitch without degrading electrostatics. The recessed portion of the gate helps by screening the drain field from the source region. Another advantage of the U-channel device is that the contact length can be larger at fixed pitch which helps in mitigating the increasing problem of contact resistance. The idea of grooved gate MOSFET was explained in a pioneering paper [11] that showed the benefits of achieving a negative junction depth. The authors observed improved punch through breakdown characteristics and less threshold change due to channel length variations. Improved short channel characteristics were observed with negative junction depth in other bulk devices as well [12], [13]. An SOI ultra-short junction-less V-shaped channel device was fabricated [14] which appears to have high gate to S/D overlap capacitance.

We now investigate the electrostatics of the proposed device using 2D Technology Computer Aided Design (TCAD). Idealized structures were generated using uniform doping profiles with Gaussian tails and the

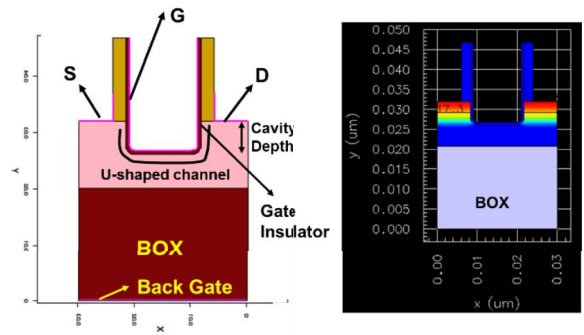


FIGURE 3. (Left): Geometry of structure and (right) extension doping used in TCAD. The well has a uniform Boron doping of $1E17cm^{-3}$. The steep arsenic shallow junction profile shown has a metallurgical junction depth of about 3nm. The shallow extension carries current only a short distance to raised S/D regions (not shown).

electrostatics were investigated by using the FIELDAY drift-diffusion simulator including SRH recombination, Mujtaba mobility model, quantum correction for inversion layer and band gap narrowing [15].

Figure 3 shows the U-channel structure and the doping profile used for 2D-TCAD simulation studies of an NFET device. It represents an ideal ultimate process which starts with a shallow heavily doped n-type blanket layer on a lightly doped p-type SOI wafer. This can be followed by the process steps for the U-channel device including the recessing step which will go through and beyond the blanket layer. It is crucial in this device to maintain a shallow junction at the gate edge to minimize both the gate-overlap capacitance [16] and the doping gradient where the source links to the U-channel. Therefore, thermal process steps need to be limited. The key parameters are summarized in Figure 4.

Voltage	0.9V
Gate WF (eV)	4.36 (~ quarter gap for NFET)
EOT(nm)	0.7
Back gate WF	Mid-gap/NFET/PFET

FIGURE 4. Parameters used in TCAD simulation.

For these simulations, the gate insulator equivalent oxide thickness (EOT) was assumed to be 0.7 nm as it is becoming increasingly difficult to scale the gate insulator. Further, a realistic quarter-gap (Q-gap) work-function (WF) of 4.36eV, was assumed, which can be achieved in a small gate opening (< 20nm) by optimizing the WF setting metal process. All simulations were performed at $V_{dd} = 0.9V$ for illustration. Figure 5 shows the IV characteristics in linear and saturation conditions, demonstrating good subthreshold and DIBL characteristics.

Figure 6 shows V_t roll-off, subthreshold slope in saturation, and DIBL as a function of total channel length which

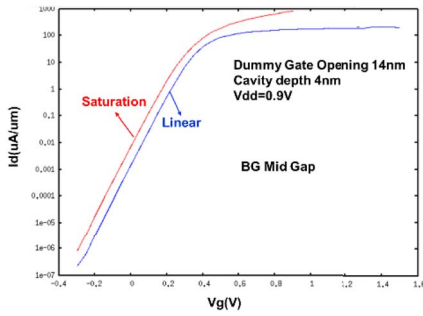


FIGURE 5. IV characteristics showing excellent DIBL and subthreshold behavior. The starting SOI is 8nm, gate opening is 14nm and cavity depth is 4nm.

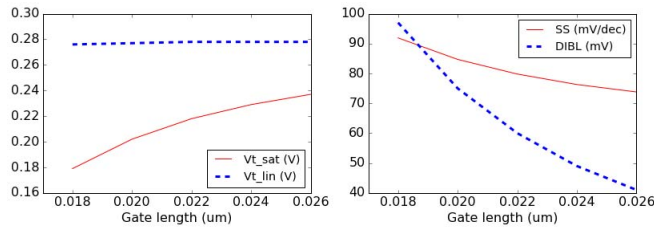


FIGURE 6. (Left): NFET roll-off characteristics with a PFET back-gate work-function and Q-gap NFET gate WF. (Right): Sub-threshold slope (SS) and DIBL as a function of gate length. Notice that a target device of $L = 0.022\mu\text{m}$ ($L_{\text{eff}} \sim 0.018\mu\text{m}$) has excellent DIBL and SS.

is varied with cavity opening. The starting SOI is 8nm and cavity is 4nm.

It is important to control the starting SOI thickness and the gate recess cavity depth. Figure 7 shows the effect of each of these parameters on the electrostatics of the device.

	Si below Chnl 4nm	Si below Chnl 5nm	Si below Chnl 6nm		Cavity 5nm	Cavity 6nm	Cavity 7nm
Starting SOI (nm)	10	11	12	Starting SOI (nm)	11	11	11
V_{t_lin} (V)	0.333	0.311	0.294	V_{t_lin} (V)	0.294	0.311	0.332
V_{t_sat} (V)	0.293	0.263	0.240	V_{t_sat} (V)	0.229	0.263	0.296
SS (mV/dec)	76	80	84.5	SS (mV/dec)	88	80	74
DIBL (mV)	40	48	54	DIBL (mV)	65	48	36
Ioff (nA/um)	3	10	25	Ioff (nA/um)	45	10	2

FIGURE 7. (Left): The NFET electrostatics for different starting SOI thicknesses but same cavity depth ($L = 26\text{nm}$, cavity = 6nm and gate opening = 14nm). (Right): The NFET electrostatics for same starting SOI thickness but different cavity depths. The front gate WF is Q-gap and back gate WF is mid-gap with a gate insulator EOT of 0.7nm.

The nominal case is assumed to be starting SOI of 11nm and 6nm gate recess cavity. As expected, the electrostatics get worse for thicker starting SOI or under-etched cavity, but the impact is not severe even with these extreme variations and should be manageable with careful process control.

It is of interest to compare the U-channel device with UTBB devices of same effective gate length. Both conventional UTBB and U-channel devices were simulated with TCAD. In Figure 8, the U-channel device is compared to conventional UTBB devices with uniform SOI thickness equal to that below the recessed gate of the U-channel device. The conventional UTBB devices had a gate recess of about

	Si below chn. 4nm	Si below chn. 4nm	Si below chn. 4nm
Channel	aprox. horizontal	aprox horizontal	U-shaped
Gate Opening (nm)	20	14	14
L total (nm)	22	16	26
Cavity (nm)	1	1	6
L_{eff} (nm)	21.4	15.4	22
Starting SOI (nm)	4	4	10
SSsat (mV/dec)	74.5	88	76
DIBL (mV)	41	76	40
Ioff (nA/um)	4	44	3

FIGURE 8. Results show that a U-channel device behaves like a conventional UTBB device of similar effective channel length.

	BG: N Type	BG: Mid	BG: P Type
Cavity (nm)	4	4	4
Gate Opening (nm)	14	14	14
L total (nm)	22	22	22
L_{eff} (nm)	18	18	18
Gate WF (eV)	4.36	4.36	4.36
EOT (nm)	0.7	0.7	0.7
Starting SOI (nm)	8	8	8
V_{tlin} (V)	0.283	0.333	0.379
V_{tsat} (V)	0.233	0.282	0.320
SSsat (mV/dec)	81	80	80
DIBL (mV)	50 /49	51/ 51	59/ 60
Ioff (nA/um)	25.8	7.3	2.9

FIGURE 9. The back-gate WF can be used to get additional thresholds. For example, changing the back-gate WF from N-type to P-type changes the off-current by a factor of about 9X with a BOX thickness of 20nm. The same effect can be obtained by fixing BG WF and changing the BG bias voltage.

1nm to simulate the effects of dummy gate removal and any wet cleans prior to gate insulator processing. It is seen that the electrostatics of the U-channel device are similar to those of conventional UTBB with similar effective channel length modeled with the same ideal doping profile, but only the U-channel process has the capability to produce low-resistance self-aligned doping regions under the spacers. Thus, to a first approximation, the U-channel device is an effective way of scaling gate pitch at equivalent electrostatics as a conventional UTBB FDSOI device.

The U-channel UTBB device, like the UTBB FDSOI, has an advantage over FinFET technology in having back gates which can set or modulate threshold voltage. Such capability is useful in system level power-performance optimization. The back gate (BG) of the U-channel device can be doped and also biased to influence the device threshold voltage. Thus, low Ioff and low threshold devices can be obtained by applying reverse and forward biases on BG respectively.

TCAD simulations were performed with N-type and P-type BGs held at a bias of 0V. Figure 9 shows that using N-type or P-type back-gates provides low V_t or high V_t devices with about 9X difference in Ioff for a BOX thickness of 20nm. Further, for example, changing the bias potential of either back gate type by about 1V (the difference in N-type and P-type WF) can be used to modulate Ioff an additional 9X. Example architecture of a UTBB biasing scheme [17] is

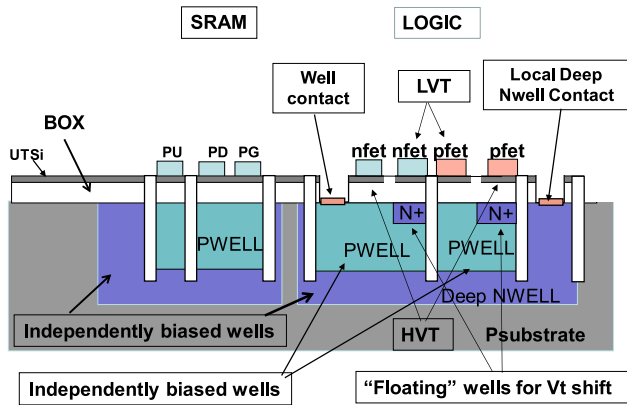


FIGURE 10. An example illustration of SRAM and 2 levels of logic obtained by well doping and biasing [17].

reproduced in Figure 10. In the simplest version of U-channel UTBB, the substrate can be a common node. For system level optimization, N-Type and P-Type wells can be situated beneath both nfets and pfets and independently contacted and biased to achieve desired threshold voltages. In doing so, care should be taken to minimize and mitigate proximity effects of metal gate WFs [17].

III. GIDL ESTIMATES

Another design factor is Gate Induced Drain Leakage (GIDL) in the proposed architecture. GIDL occurs by band-to-band tunneling (BTBT) between any 2 points in the device having a potential difference at-least equal to the band-gap of the semiconductor. Solomon *et al.* [18] have shown that the BTB tunneling current density is a function of the tunneling distance, which can be measured on a two-dimensional potential plot. The tunneling density (A/cm^2) can be converted to tunneling current per unit device width (A/cm) by assessing the width on the two-dimensional potential plot where the shortest possible tunneling distance exists.

Equipotential contours in the U-channel nfet device are shown in Figure 11(left). The crowding and termination of drain field lines in the recessed portion of the metal gate confirms that the recessed metal gate screens the field lines emanating from the drain, thus benefiting short channel effects. Also, the minimum distance between 2 equipotential contours separated by the band-gap of Si is seen from Figure 11(right) to be about 7nm in this device at the simulated voltage conditions. This leads to a BTBT current density value of about $10nA/\mu m^2$ from the data in the Solomon paper. It is seen that the cross-sectional area over which BTBT can occur is extremely small, with a width of about 1nm at the most. Thus, the BTBT current is less than 10 pA/ μm . These DIBL estimates do not include any parasitic bipolar enhancement because the FDSOI structure mitigates that effect. Additionally, low I_{off} devices with reverse-biased back gates increase the source to body barrier, further precluding bipolar effects [19].

This low GIDL current is negligible for logic, and furthermore can enable very dense low-power SRAM or embedded

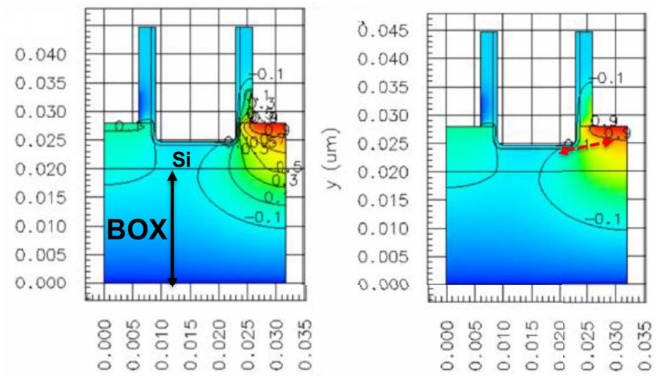


FIGURE 11. (Left) NFET potential contours for U-channel UTBB show drain field screening by gate and (right) potentials separated by 1V near the drain junction with a minimum tunneling distance of at least 7nm.

Starting SOI (nm)	10	10
Cavity (nm)	6	6
Si thickness (nm)	4	4
LMG(nm)	14	20
EOT (nm)	0.7	2.0
SSsat (mV/dec)	76	86
DIBL (mV)	40	68
Device	Logic	IO/DRAM

FIGURE 12. Comparison of a feasible DRAM device design to the logic device design point for this technology.

DRAM. The low V_t or high-performance logic pfet device will benefit with a SiGe channel. However, the SiGe channel makes the pfet more vulnerable to GIDL than the nfet due to reduced band-gap of SiGe compared to Si. Assuming a band-gap of 0.8V, the minimum tunneling distance becomes about 5nm for the pfet with a GIDL current estimate of $1nA/\mu m$. In SRAM, SiGe channel is not likely to be used and so the GIDL becomes less of a concern.

The table in Figure 12 shows a comparison of a possible embedded DRAM or Input/Output (IO) device design to the logic device design point for this technology. The DRAM design requires a higher gate voltage on the word-line to write the highest bit-line voltage into the capacitor. The higher voltage supply V_{pp} could be of the order 1.5V, while the logic voltage in the upcoming timeframe would be perhaps 0.7V or lower. The DRAM device requires a larger EOT to support the higher voltage and maintain very low tunneling current in the gate insulator. Thus, the electric field at the gate/drain edge is no higher than the logic device and maintains low I_{off} current sufficient for embedded DRAM applications. The larger EOT degrades the electrostatics somewhat but still gives quite acceptable results for IO/DRAM applications.

IV. GATE STACK FEASIBILITY

A key requirement for this technology is a suitable gate stack (with the desired effective metal gate WF) with a gate

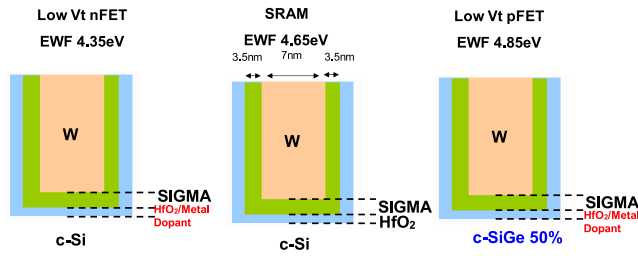


FIGURE 13. Channel and gate stack architectures for a narrow gate opening.

	7nm Node	5nm Node
Cavity (nm)	6	6
LMG(nm)	14	12
L total (nm)	26	24
Leff (nm)	~22	~20
WF (eV)	4.36	4.36
EOT (nm)	0.7	0.7
Starting SOI (nm)	11	10
Vtlin (V)	0.311	0.3355
Vtsat (V)	0.263	0.2854
SSsat (mV/dec)	80	80
DIBL (mV)	48	50
Ioff (nA/um)	10	6

FIGURE 14. A possible scaling path for the U-channel device.

opening as small as 14nm for the 7nm node. The gate stack proposal is depicted in Figure 13.

All devices are enabled by using a SIGMA metal and hafnium oxide [20] with tungsten as gap-filling metal. An nfet q-gap WF (left) can be achieved by using hafnium oxide with a metal dopant. An SRAM mid-gap WF (center) for nfet and pfet is achieved without using any metal dopant. A low-Vt pfet WF (right) is obtained using metal dopant with hafnium oxide in conjunction with SiGe channel. The q-gap nfet and pfet work functions were demonstrated at an inversion gate insulator thickness of 12.5Å [20].

V. SUMMARY AND CONCLUSION

In this paper, a novel U-channel UTBB FDSOI technology with recessed metal gate is proposed as an option to continue scaling UTBB FDSOI to the 7nm node. 2D TCAD modeling shows electrostatic feasibility of the device which mitigates the need to scale starting SOI and gate insulator thickness and offers the benefit of obtaining multiple device thresholds using back-gate doping and/or biasing. GIDL analysis shows that Ioff can be generally below an acceptable level and feasibility for obtaining desired metal gate work-functions is shown.

We also investigate the continued scaling path of the U-channel device to the 5nm technology node using TCAD. Figure 14 shows a possible path that does not require further gate insulator scaling and reduces the metal gate

opening (LMG) to 12nm. With the suggested scaling path, similar DIBL and sub-threshold characteristics are obtained from the simulations.

Further modeling work and experimentation is needed to understand the transport characteristics in the U-channel including the effects of strain. Experimental verification of the critical shallow junctions is also suggested. However, we believe that the proposed U-channel device may be the most attractive option for continued Si CMOS scaling with ability to obtain multiple device thresholds and to control parasitic capacitance and resistance.

REFERENCES

- [1] C. Auth *et al.*, "A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," in *VLSI Symp. Tech. Dig.*, Honolulu, HI, USA, 2012, pp. 131–132.
- [2] S. Natarajan *et al.*, "A 14nm logic technology featuring 2nd-generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588 μm^2 SRAM cell size," in *IEDM Tech. Dig.*, San Francisco, CA, USA, 2014, pp. 71–73.
- [3] C.-H. Lin *et al.*, "High performance 14nm SOI FinFET CMOS technology with 0.0174 μm^2 embedded DRAM and 15 levels of Cu metallization," in *IEDM Tech. Dig.*, San Francisco, CA, USA, 2014, pp. 3.8.1–3.8.3.
- [4] D. J. Frank, Y. Taur, and H.-S. P. Wong, "Generalized scale length for two-dimensional effects in MOSFETs," *IEEE Electron Device Lett.*, vol. 19, no. 10, pp. 385–387, Oct. 1998.
- [5] D. J. Frank *et al.*, "Device scaling limits of Si MOSFETs and their application dependencies," *Proc. IEEE*, vol. 89, no. 3, pp. 259–285, Mar. 2001.
- [6] Q. Liu *et al.*, "High performance UTBB FDSOI devices featuring 20nm gate length for 14nm node and beyond," in *IEDM Tech. Dig.*, Washington, DC, USA, 2013, pp. 9.2.1–9.2.4.
- [7] R. Carter *et al.*, "22nm FDSOI technology for emerging mobile, Internet-of-Things, and RF applications," in *IEDM Tech. Dig.*, San Francisco, CA, USA, 2016, pp. 2.2.1–2.2.4.
- [8] N. Planes *et al.*, "28nm FDSOI technology platform for high-speed low-voltage digital applications," in *IEDM Tech. Dig.*, Honolulu, HI, USA, 2016, pp. 133–134.
- [9] L. Grennouille *et al.*, "UTBB FDSOI scaling enablers for the 10nm node," in *Proc. 33S*, Monterey, CA, USA, 2013, pp. 1–2.
- [10] Q. Liu *et al.*, "FDSOI CMOS devices featuring dual strained channel and thin BOX extendable to the 10nm node," in *Proc. IEDM*, San Francisco, CA, USA, 2014, pp. 9.1.1–9.1.4.
- [11] S. Nishimatsu, Y. Kawamoto, H. Masuda, R. Hori, and O. Minato, "Grooved gate MOSFET," *Jap. J. App. Phys.*, vol. 16, pp. 179–183, Jan. 1977.
- [12] E. Takeda, H. Kume, and S. Asai, "New grooved-gate MOSFET with drain separated from channel implanted region (DSC)," *IEEE Trans. Electron Devices*, vol. ED-30, no. 6, pp. 681–688, Jun. 1983.
- [13] W.-H. Lee, Y.-J. Park, and J. D. Lee, "A new recessed gate MOSFET structure with graded source/drain," *IEEE Trans. Electron Devices*, vol. 40, no. 11, pp. 2102–2103, Nov. 1993.
- [14] S. Migita, Y. Morita, M. Masahara, and H. Ota, "Impact of atomic-scale structural design on ultra-short channel (3 nm) MOSFETs," presented at the IEEE 5th Int. Nanoelectron. Conf. (INEC), Singapore, 2013, pp. 132–135.
- [15] E. M. Buturla, J. Johnson, S. Furkay, and P. Cottrell, "A new three-dimensional device simulation formulation," in *Proc. 6th Int. Conf. Numer. Anal. Semicond. Devices Integr. Circuits (NASECODE VI)*, 1989, pp. 291–296.
- [16] Y. Omura, A. Mallik, and N. Matsuo, *MOS Devices for Low-Voltage and Low-Energy Applications*. Singapore: Wiley, 2017, pp. 198–202.
- [17] T. Hook *et al.*, "Fully-depleted planar technologies and static RAM," in *VLSI Symp. Tech. Dig.*, Kyoto, Japan, 2013, pp. T206–T207.
- [18] P. M. Solomon *et al.*, "Universal tunneling behavior in technologically relevant P/N junction diodes," *J. Appl. Phys.*, vol. 95, no. 10, pp. 5800–5812, 2004.

- [19] F. Liu, I. Ionica, M. Bawedin, and S. Christoloveanu, "Effect of back gate on parasitic bipolar effect in FD SOI MOSFETs," presented at the IEEE SOI-3D Subthreshold Microelectron. Technol. Unified Conf. (S3S), Millbrae, CA, USA, 2014, pp. 1–2.
- [20] T. Ando *et al.*, "Simple gate metal anneal (SIGMA) stack for FinFET replacement metal gate toward 14nm and beyond," in *Proc. VLSI Symp.*, Honolulu, HI, USA, 2014, pp. 1–2.

RAMACHANDRAN MURALIDHAR received the Ph.D. degree in chemical engineering from Purdue University in 1988. He has been with IBM since 2008. He has an interdisciplinary modeling background and has contributed in many areas, including inverse problems for colloidal systems and methane leak detection, nonequilibrium statistical physics of condensed phases, and modeling dispersion of accidental releases of HF mixtures. His contributions in semiconductor technology include the development of silicon nanocrystal memory in Freescale Semiconductor, and investigating process and logic and memory device scaling via simulations for 22 nm node and beyond. He has been recently working on AI applications in the semiconductor industry and methane leak detection. He has over 35 issued patents and has co-authored over 40 publications/conference proceedings and book chapters.

ROBERT H. DENNARD (LF'99) is an IBM Fellow Emeritus with the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA, where he was involved in microelectronics research and development from its early days. In 1967, he invented the single-transistor dynamic memory cell (DRAM) used in most computers today. With co-workers, he developed the concept of MOSFET scaling in 1972. He currently works on extending CMOS scaling toward its fundamental limits, and on energy efficient computing.

He was a recipient of the IEEE Medal of Honor in 2009 and the National Medal of technology presented by President Reagan in 1988, and was inducted into the National Inventors Hall of Fame in 1997.

TAKASHI ANDO received the B.S. and M.E. degrees from the University of Tokyo in 1999 and 2001, respectively, and the Ph.D. degree from Osaka University in 2010. He has been a Research Staff Member with IBM T. J. Watson Research Center since 2008. He has authored or co-authored over 100 publications in peer-reviewed journals, refereed conference proceedings, and book chapters. He was a recipient of the IBM Outstanding Technical Achievement Award for his contributions to high-k/metal gate technology and SiGe FinFET technology in 2013, 2016, and 2017, the Japan Society of Applied Physics Young Scientist Award in 2011, and the IEEE EDS George E. Smith Award in 2013.

ISAAC LAUER, photograph and biography not available at the time of publication.

TERENCE HOOK received the B.Sc. degree from Brown University and the Ph.D. degree in EE from Yale University in 1986. He has been with IBM since 1980. While at IBM he has worked on technology integration and device design for bipolar, BiCMOS, and CMOS technologies from two micrometer to 5 nm and beyond. He has authored many dozens of conference and journal papers and holds over 100 patents. He is currently with IBM Research, Albany, NY, USA.