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A New On-Chip ESD Strategy Using TFETs-TCAD Based Device and Network Simulations

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ABSTRACT For the first time, this paper reports the quasi-static behavior and the applicability of the tunnel field effect transistor (TFET) for the on-chip electrostatic discharge (ESD) protection. ESD evaluations are performed on 28-nm fully depleted silicon-on-insulator (FDSOI), bulk TFET and compared with conventional shallow trench isolation (STI) diode using a well calibrated 3-D technology computer aided design (TCAD) device and process simulation deck. Initial design insights are obtained using the DC characteristics. The quasi-static behavior of a TFET is studied by applying transmission line pulsing (TLP) and very fast TLP (VFTLP) pulses at its drain terminal with gate shorted together and source connected to the ground. During negative TLP pulse at the drain, the TFET becomes a forward biased gated diode and exhibits reduced on-resistance compared to the STI diode. During positive TLP pulse, the tunneling current at the source-channel junction introduces a low impedance current path from drain to source compared to the blocking behavior of the STI diode. A short description of the advantages and challenges of the TFET from ESD perspective are also discussed. Finally, a new TFET ESD network is proposed and shown to exhibit multiple current paths compared to STI diode-based ESD network. From the network simulations, the proposed TFET-based ESD network is shown to exhibit better CDM response and hence providing a robust ESD solution for future system-on-chip design.

INDEX TERMS Tunneling field effect transistor (TFET), electrostatic discharge (ESD), silicon on insulator (SOI), transmission line pulsing (TLP), very fast transmission line pulsing (VFTLP).

I. INTRODUCTION

Developing a robust electrostatic discharge (ESD) network in the advanced complementary metal oxide semiconductor (CMOS) technologies is quite challenging because of the reduced off-state breakdown voltages, gate oxide breakdown and safe operating area (SOA) of the load to be protected. This results in a narrow ESD design window [1]. Added to this challenge, the robustness of the ESD protection devices are also degrading in the advanced CMOS technologies due to the degenerative doping and lower junction depths (to ensure scaling) resulting in reduced failure current per unit area compared to the mature CMOS technologies. Though there is a continuous research on-going to reduce the on-chip HBM and CDM standards from 2 kV to 1 kV and 500 V to 250 V respectively by implementing ESD control measures during manufacturing environment without affecting the yield, the proposal has not been accepted as the ESD standard across various semiconductor original equipment manufacturers (OEM) and the ESD targets remains unaltered with device scaling. This motivated us to evaluate the novel device architectures and networks in state of the art CMOS technologies.

Tunneling Field Effect Transistor (TFET) is a promising steep sub-threshold switching device with faster switching speed targeted for sub 7 nm CMOS applications. Extensive research has been carried to improve the performance parameters like I_{ON}/I_{OFF} ratio [2], sub-threshold swing [3], scaling behavior [4], transport characteristics through abrupt doping profile of junctions, vertical transistors for line tunneling, material engineering [5] and hetero-structures for improving the tunneling probability [6], [7]. Various applications like static random access memory (SRAM), dynamic random access memory, digital and analog sub-systems using TFET are proposed [8]–[10]. However the reliability studies about these tunneling devices are limited [11], [12]. Hence, understanding ESD response of the TFET is important for

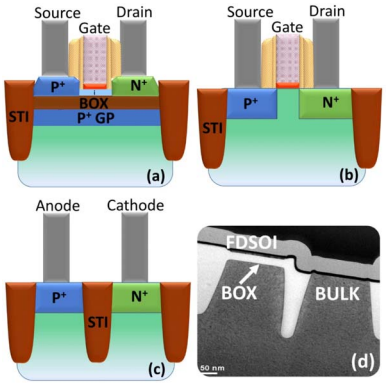

FIGURE 1. Device cross-section of (a) FDSOI TFET (b) Bulk TFET (c) STI Diode (d) FDSOI-Hybrid integration [13].

two reasons (1) If the ESD response of the TFET is better than the conventional ESD devices, then it opens up an new opportunity for TFET based ESD network design (2) If TFET augments the conventional CMOS devices portfolio in the mainstream integrated circuit design, then TFET becomes the potential load to be protected from HBM and CDM ESD stresses, hence from both the dimensions understanding the ESD behavior of the TFET becomes the necessity.

This paper extensively studies the quasi-static behavior of both the fully depleted silicon-on-insulator (FDSOI) and bulk TFET and compares with the conventional STI diode during ESD scenarios using a well calibrated 3D technology computer aided design (TCAD) process and electro-thermal device simulations. The schematic cross sections of the devices under study are shown in Fig. 1. The paper is organized as follows; first a brief discussion on the simulation parameters and TCAD methodology followed in this paper is discussed. Further, we discuss the DC, TLP and VFTLP simulations. Finally, we discuss the advantages of the TFET in ESD and a new TFET based ESD network is also proposed and validated through mixed mode simulations.

II. SIMULATION PARAMETERS AND TCAD METHODOLOGY

Since the TCAD based electro-thermal simulations of the TFET are complex, an elaborate discussion on the (a) device parameters used, (b) performance evaluation methodology followed and (c) the physical models used in our simulations are provided in this section with suitable references. The schematic cross-section of the TFET implemented in the FDSOI and bulk technologies are shown in Fig. 1 (a) and (b) respectively. The reference device (STI diode) used in the conventional on-chip ESD protection network is shown in Fig. 1 (c), the doping profiles of the STI diode are calibrated from the SIMS data of the hybrid bulk devices done by etching the buried oxide as shown in Fig. 1(d) [13].

A. DEVICE PARAMETERS

The physical dimensions of the bulk and the FDSOI TFET used in our simulations are the following: gate length (L_G) = 50 nm; effective gate oxide thickness (tox) = 3 nm; silicon film thickness (t_{si}) = 7 nm; buried oxide thickness (t_{box}) = 26 nm; source (p-type) doping = 1.5×10^{20} cm^{-3}; drain (n-type) doping = 5×10^{18} cm^{-3} (to reduce ambipolar current conduction), channel doping (p-type) = 1×10^{15} cm^{-3} and gate work function = 4.1 eV. The widths of all the devices are chosen to be 1 μm. The heat sink/substrate contact is placed 5 μm below the buried oxide in the substrate. The substrate thickness (tsub) is chosen to be 5 μm since the thermal diffusion length for 100 ns TLP pulse is 3.3 μm [14]. The junction height of the bulk TFET is taken as 80 nm.

B. PERFORMANCE EVALUATION METHODOLOGY

To benchmark the TFET for ESD applications, the following ESD device characterization methodology is adopted in this paper. The functionality of an ESD device is to provide an ideal short circuit path from the I/O pad to the ground or supply pads during ESD events and should be an open circuit during normal operation. However the ESD device introduces parasitic leakage current during functional mode and shows finite on-resistance during an ESD stress. The leakage current specification of an ESD device during the functional operation of the I/O pad is obtained from the DC characteristics, and the turn-on characteristics of the device during the ESD event is determined from its TLP/VFTLP characteristics.

TCAD based TLP and VFTLP characterization are performed to emulate the on-wafer TLP and VFTLP device characterization. The Transmission Line Pulsing (TLP) and Very Fast Transmission Line Pulsing (VFTLP) scheme gives the device level characterization methodology to predict the ESD response of the device under test (DUT) which is similar to the transient and fast transient conditions occur during the ESD stress [15]. In TCAD simulations, the TLP scheme is approximated by applying successive current pulses (ideal current source connected to the DUT) with the increasing magnitude and the resultant voltage across the ESD device is monitored. Such kind of ESD simulations where the ESD stress has a transient rise time followed by the constant amplitude and fall time for a small duration is generally referred as partly static or quasi-static simulation. For the TLP simulations, current pulses of rise time (t_r) of 10 ns and pulse width (t_{width}) of 100 ns with increasing magnitude of current is given to the DUT according to the ESDA TLP specifications (this scheme correlates to the HBM stress) [16]. For the VFTLP scheme, the rise time (tr) of 200 ps and pulse width (twidth) of 1 ns is given to the DUT according to the ESDA VFTLP specifications (this scheme correlates to the CDM stress) [17]. For both the schemes, the voltage sample is obtained by calculating the net voltage across the DUTs from 75%–95% of the twidth, this methodology (followed in this paper) is

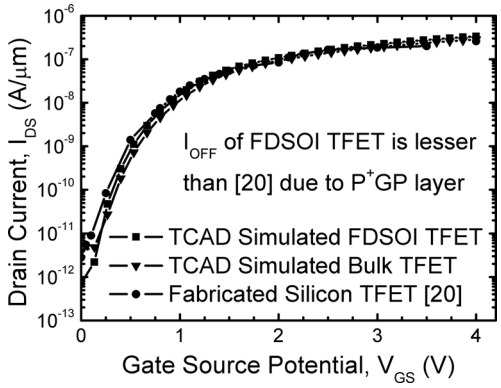

FIGURE 2. Calibrated transfer characteristics of the FDSOI TFET and bulk TFET with the experimental data.

derived in accordance with the TLP/VFTLP specifications mentioned in [16] and [17].

C. TCAD METHODOLOGY

The reference STI diode is simulated using a calibrated 3D process simulation deck of 28 nm ultra-thin body and box (UTBB) FDSOI technology using Synopsys Sentaurus TCAD tool. For the TFET, a well calibrated device simulation setup using dynamic non-local band-to-band tunneling (BTBT) is used. The Apath1 and Bpath1 parameters used in our simulations are 1.5×10^{13} $cm^{-3}s^{-1}$ and 6×10^{6} Vcm^{-1} respectively. The modified parameters signify the reduced band-to-band tunneling and increased generation rate as observed in experimental results [18] compared to the default device parameters of the TCAD tool. To model the impact ionization and avalanche generation, we have chosen default VanOverstraeten model which is proven to exhibit better accuracy and simulation convergence for complex device simulations like ESD [19]. The simulated transfer characteristics matches with the experimentally demonstrated silicon TFET structure with <10 % error [20] as shown in Fig. 2. Other physical models used in the simulation are field-dependent mobility model, Slotboom band-gap narrowing (BGN) model and Hurkx trap assisted tunneling model for high field Shockley-Read-Hall recombination.

ESD simulations are electro-thermal in nature and also non-isothermal where the temperature of the charge carriers and lattice vary as a function of time and space inside the device. They are performed using TCAD tools by incorporating suitable self-heating models and thermal contact/heat sink placed in the substrate which solves the coupled thermodynamic equations along with continuity and Poisson equations as a function of time and space [21]. To cover the worst case self-heating effect, only substrate is used as heat sink and not the source, drain and gate of the TFET. The hard failure/thermal failure current (I_{T2}) of the device is taken as the current at which the voltage snapback occurs or the potential at which the hot spot in the device reaches ~800 K (to cover the worst case scenario, the failure temperature is taken to be very low compared to the actual melting point of silicon which is $T_{Crit} = 1687$ K) [22]. The choice of the physical models and parameters are done to cover the worst case scenario of the device operation. The calibration of the DC characteristics of the proposed device is done by matching the results of the device simulation as reported in [20, Fig. 2]. For the TLP and VFTLP simulations, the standard procedure and guidelines for the device simulation of ESD devices [16], [17], [19], [21] are followed.

III. RESULTS AND DISCUSSION

In this section, we first discuss the DC characteristics of the TFET followed by the quasi-static characteristics of the TFET, i.e., TLP and VFTLP characteristics.

A. DC CHARACTERISTICS

The transfer characteristics gives an estimate of the off-current and the on-current required for calculating the parasitic leakage current at the input/output I/O pad (if STI diode is replaced by TFET) during the functional operation. The transfer characteristics of the reference silicon TFET [20] taken for the calibration with the TCAD simulated bulk and FDSOI TFET's are shown in Fig. 2. We observe that the leakage current of the FDSOI TFET is lesser compared to the bulk and reference TFET for the same process and device parameters. This reduction is due to the additional work function difference created by the ground plane P^+ layer below the buried oxide (BOX) of the FDSOI transistor. The off-current of the reference, bulk and FDSOI TFETs are 4 pA/μm, 3 pA/μm and 0.7 pA/μm respectively for $V_{DS} = 1$ V and $V_{GS} = 0$ V. However, the leakage current of the STI diode is approximately $\sim 0.05 - 0.1$ pA/μm for the reverse bias potential of 1 V which is an order lesser than the TFET's leakage current. Since TFET is leaky compared to the STI diode, we have analyzed its behavior with varying gate lengths (which can be a design parameter to reduce leakage current) and bias voltages (to understand the voltage ranges where TFET can replace STI diode) are explained in the following sections.

A.1. EFFECT OF GATE LENGTH

The gate length is the only design parameter available to the ESD designer for the fixed TFET process. Hence, the effect of gate lengths on the on-current and off-current is investigated. Fig. 3 (a, b) shows the transfer characteristics of the TFET with varying gate lengths (L_G) for the FDSOI and bulk TFET respectively. It's observed that both the on-current current and the off-current are not altered with varying gate lengths for the FDSOI TFET. However for the bulk TFETs there is a small spread of leakage current (0.7 pA – 3 pA) due to the increased short channel effects compared to the FDSOI transistor. The reduced spread of the leakage current with the gate length variation indicates the superior scalability of the TFETs in the advance technology nodes and is in-line with many published results [23]–[25]. With these initial results, it is evident that the leakage current can be tuned by the process parameters only and hence cannot be a design

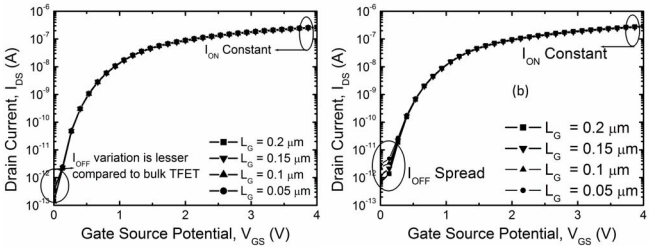

FIGURE 3. Transfer characteristics of the (a) FDSOI TFET and (b) bulk TFET with varying gate lengths.

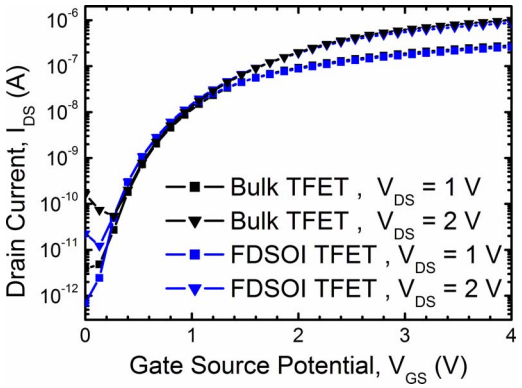

FIGURE 4. Transfer characteristics of the Bulk and FDSOI TFET with varying drain to source voltages.

parameter. But on the positive side, TFET can be designed with minimum gate lengths for ESD applications and hence may reduce ESD device footprint in the I/O pad.

A.2. EFFECT OF DRAIN VOLTAGE

Fig. 4 shows the transfer characteristics of both the FDSOI and the bulk TFETs for $V_{DS} = 1$ & 2 V, the leakage current characteristics of the FDSOI TFETs is increased from 0.7 pA/μm to 20 pA/μm and the leakage current of the bulk TFET increases from 3 pA/μm to ∼0.3 nA/μm for the bulk TFETs. The leakage mechanism with varying drain voltages can be understood from the Fig. 5. Fig. 5 shows the schematic cross section of FDSOI and bulk TFET showing increase in the band-to-band generation parameter for the increase in V_{DS} from 1 V to 2 V. This additional tunneling current at the higher drain potential is the root cause of the increased leakage current. Unlike MOSFETs, this additional current doesn't scale down when increasing the gate lengths since tunneling current is not a function of the gate length for both FDSOI and bulk TFET. Hence TFET may find its application only in the low voltage I/O pads or in low power/voltage ICs where the maximum supply voltage can be ∼ 2 V.

A.3. EFFECT OF DEVICE MODELS

Since the TFET is targeted for low power logic applications, the TCAD simulation methodology available in [15] includes only the band to band tunneling models along with the carrier statistics and mobility models. However, ESD

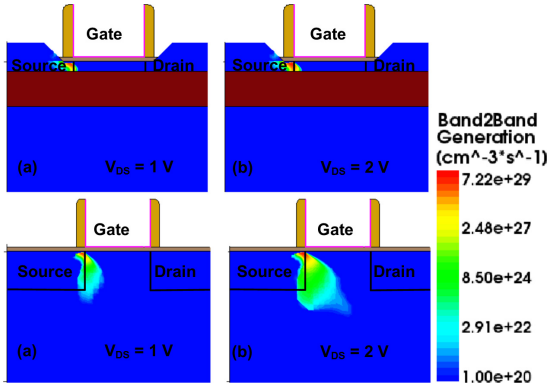

FIGURE 5. Band to Band Generation Contours of the FDSOI and bulk TFET with varying V_{DS} from 1 V to 2 V.

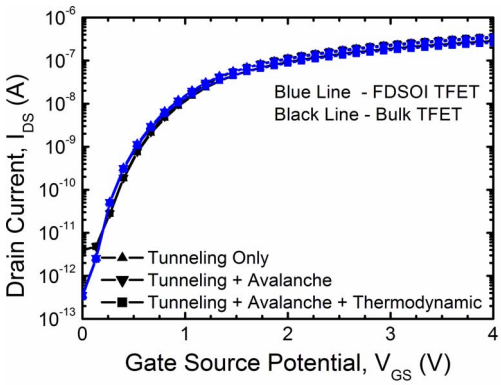

FIGURE 6. Transfer characteristics of the bulk and FDSOI TFET with different physical models.

phenomenon is electro-thermal in nature, hence we have studied the transfer characteristics of the TFET with the addition of impact ionization models and thermodynamic models for both the FDSOI and bulk TFETs. From the Fig. 6, it can be observed that the off-current is unaltered. There is only a marginal increase of the on-current compared to the simulation results (a) using tunneling and avalanche models and (b) using tunneling, avalanche and thermodynamic models. Hence the effect of avalanche and thermodynamic models are not observed in the DC characteristics.

B. QUASI-STATIC CHARACTERISTICS

The transient characteristics of the TFET are obtained through TCAD based TLP and VFTLP scheme explained in detail in Section II. ESD stress is given to the drain and gate connected together and the source connected to the ground (this diode connected TFET configuration gives the device behavior of the single device in the proposed ESD network discussed in Section V). For the STI diode, ESD stress is given at the cathode with its anode grounded. To have a complete understanding of the quasi-static behavior of the TFET and the reference STI diode, both positive and negative ESD stresses are given. The detailed discussion of the same is as follows.

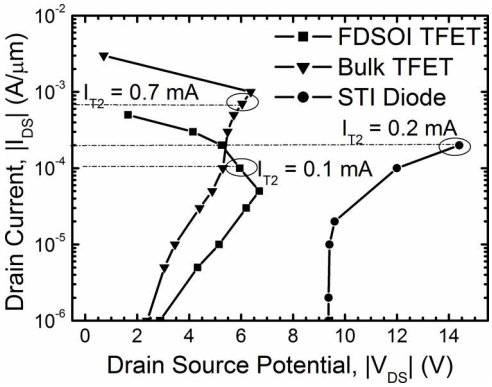

FIGURE 7. **TLP characteristics of FDSOI TFET, Bulk TFET and STI Diode during positive ESD stress at the drain of the TFET and cathode of the STI diode.**

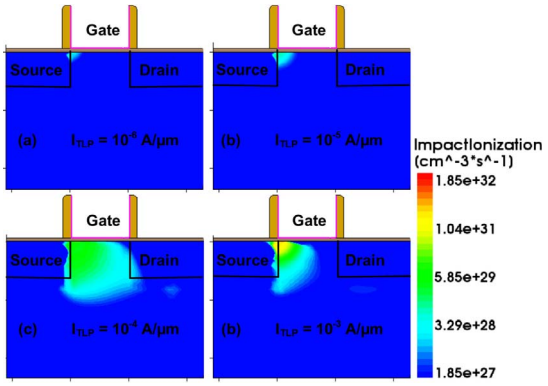

FIGURE 9. **Impact Ionization Rate Contours of the bulk TFET for various TLP currents.**

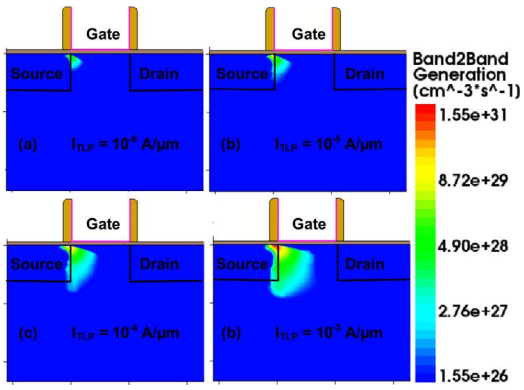

FIGURE 8. **Band to Band Generation Contours of the bulk TFET for various TLP currents.**

B.1. TLP CHARACTERISTICS

TLP characteristics of the TFET (bulk and FDSOI) and the reference STI diode for the positive ESD stress are shown in Fig. 7. The STI diode is reverse biased during positive ESD stress and exhibits hard breakdown even at low current levels. Hence the potential difference between the anode and cathode of the STI diode is its breakdown voltage of $\sim$ 9.4 V. At high current levels, increased charge carriers results in increased phonon scattering which results in mobility degradation and increased joule heating subsequently leading to the hard failure of the device. The failure current (I_{T2}) and voltage (V_{T2}) of the reference STI diode is 0.2 mA/μm and 14.5 V respectively.

The positive TLP characteristic of the TFET shown in Fig. 7 is similar to the reverse bias diode characteristics; however the additional tunneling current results in the reduction of the net on-resistance. Fig. 8 and Fig. 9 shows the band to band generation parameter and impact ionization parameter of the bulk TFET with increasing amplitude of the TLP current pulses. At low current levels ($\sim 10^{-6}$ A/μm), the onset of the point tunneling current at the source-channel junction is observed (Fig. 8 a) and also no impact ionization phenomenon (Fig. 9 a) is observed. This tunneling current introduces a low impedance current path from drain to source and hence preventing the potential build-up. From Fig. 7, it is observed that the potential difference across the bulk and FDSOI TFET at 10^{-5} A/μm are 3.5 V and 5 V respectively which is considerably less compared to the potential difference of STI diode at 9.5 V.

At higher current values ($> 10^{-5}$ A/μm), the impact ionization phenomenon is initiated resulting in the additional generation of carriers which is seen in Fig. 9 b. The band to band generation and impact ionization parameter increases with the increase in the amplitude of the TLP current pulse. Both these generation mechanisms augment each other until the failure threshold is reached as shown in the Fig. 8 d and Fig. 9 d. Another important observation about the physics of the tunneling current with increasing TLP current pulses is that, at low current levels, the band to band tunneling mechanism is observed near the channel region (Silicon-SiO_2 interface) only. However with the increase in the TLP current pulse, the band to band generation current extends even below 10 nm from the channel. This phenomenon is similar to the tunneling mechanism observed in the Zener diodes. Hence there is a small current range (from 10^{-4} A/μm to 5×10^{-4} A/μm) where the potential across the diode is pinned to the Zener breakdown voltage of around $\sim$5.5 V. At higher current levels avalanche effect dominates resulting in the increase of phonon scattering. This reduces the mobility of the carriers and hence the potential increases across the TFET leading to the physical damage. However this Zener tunneling phenomenon is not seen in the FDSOI TFET (charge carriers are generated only by point tunneling mechanism) due to the higher self-heating effects. Self-heating effect also increases the on-resistance of the FDSOI TFET (in addition to the increased source/drain resistances of the thin body compared to bulk TFETs) and reduces the failure current of the FDSOI TFET to $\sim 10^{-4}$ A/μm which is an order of magnitude lesser compared to the bulk TFET ($\sim 10^{-3}$ A/μm). The failure current is measured when the hotspot temperature reaches 800 K as shown in Fig. 10.

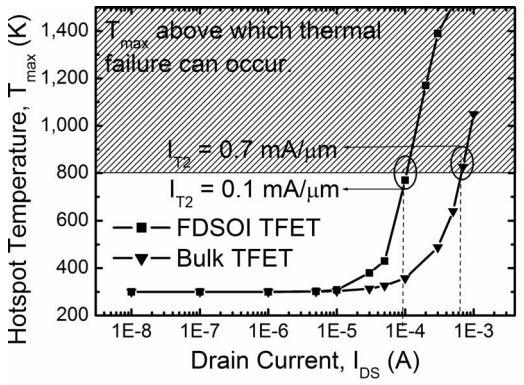

FIGURE 10. Hotspot temperature as a function of the drain current for the FDSOI and bulk TFETs.

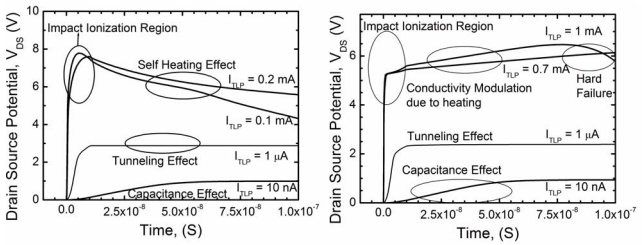

FIGURE 11. TLP Chronograms of the (a) FDSOI TFET and (b) bulk TFET for varying TLP currents.

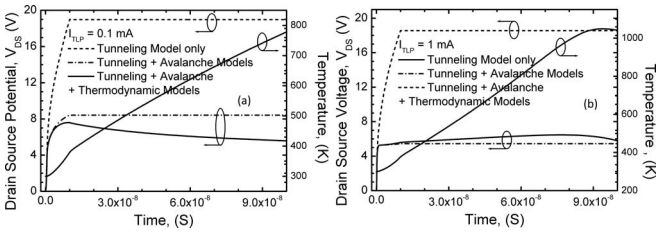

FIGURE 12. TLP Chronograms of the (a) FDSOI TFET and (b) bulk TFET for different physical models combination.

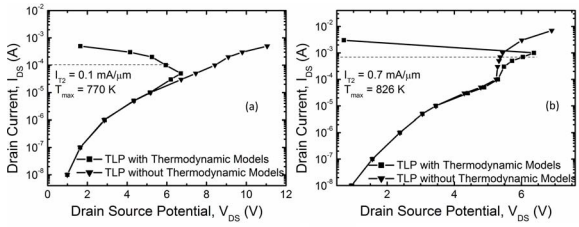

FIGURE 13. TLP Chronograms of the (a) FDSOI TFET and (b) bulk TFET with and without thermodynamic models.

To gain additional insights on the physical phenomenon happening during the TLP stresses, the TLP chronograms of the FDSOI TFET and bulk TFET are shown in the Fig. 11 (a) and (b) respectively. At current values less than 10 nA, the drain source voltage of the TFET settles around 50 ns instead of 10 ns rise time. This indicates the current is too low to charge parasitic capacitances completely in 10 ns rise time. This behavior is similar for both bulk and FDSOI TFETs. At 1 μA TLP stress, the voltage response remains flat after the rise time of 10 ns, the final drain source potential is determined from the tunneling current and is approximately same for both bulk and FDSOI TFETs. At higher current levels during the failure current level (I_{T2}), we observe a higher initial overshoot in the FDSOI TFET compared to bulk TFET due the reduced junction area. With the increase in time, generation current dominates leading to the reduction in drain-source voltage. The increase in temperature finally results in the physical failure. In the case of bulk TFET, the drain-source voltage of the TFET is pinned to the Zener tunneling voltage, however with the increase in time the mobility reduction effect (due to phonon scattering) dominates leading to an increase in the drain-source voltage. In 1 mA/μm TLP chronogram at 75 ns, the hotspot temperature is high enough to generate additional charge carriers resulting in the snapback or the physical failure of the device.

To confirm whether the failure is due to the thermal heating only, we have conducted one experiment, in which we ran three TLP simulations with different physical models, in the first case only tunneling models are included, in the second tunneling and avalanche models are included and finally in the third case, tunneling, avalanche and thermodynamic models are included at their failure current I_{T2}. The TLP chronograms of the FDSOI and bulk TFET are shown in Fig. 12 a and b respectively. First, for both FDSOI and bulk TFET only with tunneling models, we get an unrealistic settling voltage of $\sim 18-19$ V. With the avalanche and tunneling models, the voltage settles at $\sim$ 8 V for FDSOI TFET and $\sim$5.5 V for bulk TFET indicating that the tunneling current component and avalanche current component are approximately same at failure current regime. Another interesting observation is that the settling voltage is flat for the complete TLP duration. With the inclusion of the thermodynamic models, we see an initial overshoot voltage of 8 V and then the voltage snapbacks to failure in the FDSOI TFET. In the case of bulk TFET, the initial overshoot is pinned to the Zener tunneling voltage. However there is an incremental increase in the voltage response due to the mobility reduction at the higher temperature. When the generation component of the current overtakes the mobility reduction, we see the physical failure. The same can be reconfirmed from the TLP characteristics of the FDSOI and bulk TFET with and without thermodynamic models shown in Fig. 13 a and b respectively. Hence it's evident that the inclusion of the thermodynamic models resulted in the snapback and the hard failure is due to the increase in the hotspot temperature.

In forward bias mode, i.e., when the drain is given negative ESD stress, the TFET becomes a simple forward biased gated diode and exhibits the forward bias diode characteristics as shown in Fig. 14. The bulk TFET shows 30% lesser on-resistance compared to the STI diode at the TLP current of 1 mA/μm. The failure current of the FDSOI TFET is

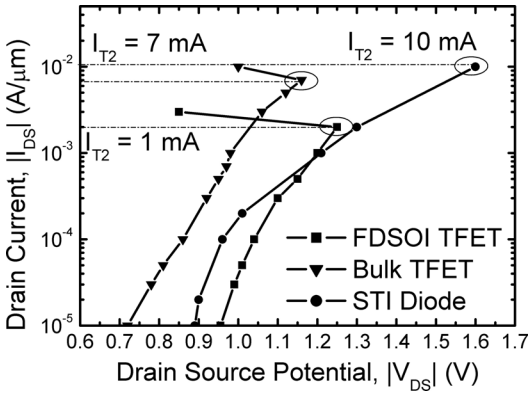

FIGURE 14. TLP characteristics of FDSOI TFET, bulk TFET and STI Diode during negative ESD stress at the drain of the TFET and cathode of the STI diode.

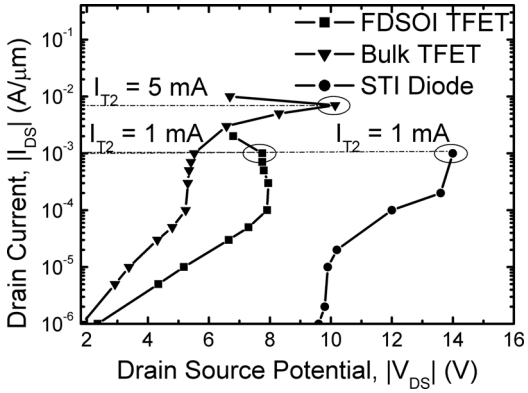

FIGURE 15. VFTLP characteristics of FDSOI TFET, bulk TFET and STI Diode during positive ESD stress at the drain of the TFET and cathode of the STI diode.

$\sim$ 1 mA/μm and is the least among bulk TFET and STI diode. The lower failure current is due to the higher thermal resistance of the buried oxide. The failure currents of the bulk TFET and STI diode are almost comparable at 7-10 mA/μm.

B.2. VFTLP CHARACTERISTICS

Since achieving CDM target is more critical than HBM target in advanced CMOS technologies, we have explored VFTLP characteristics of the TFET also in detail. The VFTLP characteristic during the positive ESD stress at the drain is shown in Fig. 15. In the case of STI diode, the V_{T1} and the on-resistance are similar to TLP characteristics. However the failure current is 5X higher compared to the TLP characteristics due to the reduction in heating (the pulse width of VFTLP is 1 ns which is significantly lesser compared to the TLP characteristics which has 100 ns pulse width). In the case of FDSOI TFET, the on-resistance is similar to the TLP characteristics at lower current levels ($< 10^{-5}$ A/μm). However with the increase in the VFTLP current pulse, the following differences with respect to the TLP characteristics are seen (a) on-resistance is higher which is due to the inability of the device to settle to final value from the initial overshoot discussed in Fig. 11 a (b) Zener tunneling effect and the steep current curve is observed due to the delayed joule heating effects (c) Both failure current (I_{T2}) and failure voltage (V_{T2}) increases by 10 X and 1.2 X respectively. In the case of bulk TFET, the on-resistance is similar to the TLP characteristics until $I_{VFTLP} < 10^{-3}$ A/μm. However due to reduce heating effects, the V_{T2} across the TFET increases to 10 V compared to $\sim$ 6 V of the TLP case. The failure current I_{T2} also increases by 5 X times compared to the TLP case. Fig. 16 shows the current density and hotspot of the FDSOI TFET and STI diode. To understand the failure mechanism, we have performed 3D TCAD simulations of the TFET and STI diode. For FDSOI TFET, the current density is at the surface indicating the failure current takes where the point tunneling from source-channel happens, the hotspot is also located in the tunneling junction. Also the

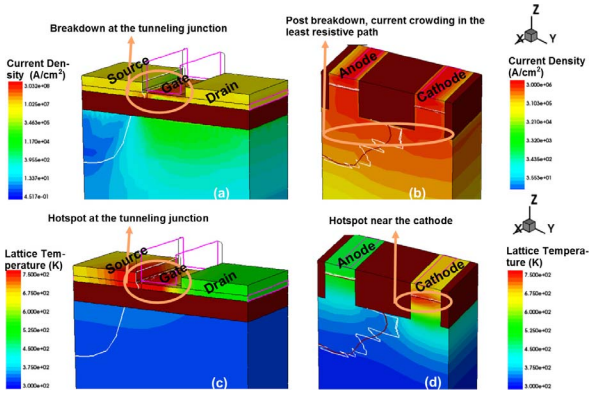

FIGURE 16. 3D process and device simulated structures showing current density and hot spot location in FDSOI TFET and STI diode during positive VFTLP pulse at the drain of the FDSOI TFET and cathode of the STI diode.

hotspot is seen more at the edges than the center of the TFET indicating non-uniform thermal resistance, the physics and behavior of this non-uniform filamentation is similar to the failure mechanism mentioned in [26]. The failure mechanism of the bulk TFET is exactly same as the FDSOI TFET and hence not shown. In the case of STI diode, the current is more uniform indicating higher failure current compared to the FDSOI TFET, and the hotspot location is in the P^+/Psub junction which is in-line with the physics available in [27].

During the negative ESD stress at the drain, the TFET becomes a forward biased diode with lower on-resistance compared to the STI diode as shown in Fig. 17. At higher VFTLP current pulse, high injection and mobility degradation effects leading to higher on-resistance are observed in the bulk TFET and the STI diode. The failure current of the VFTLP is 3–7 times more compared to the TLP characteristics indicating the time dependency on the hard failure. The failure current of the STI diode and bulk TFET are similar, however the mobility reduction due to carrier heating is more pronounced in the STI diode. The current density plots shown in the Fig. 18 depict the forward biased diode conduction mechanism, i.e., injection current. The lattice

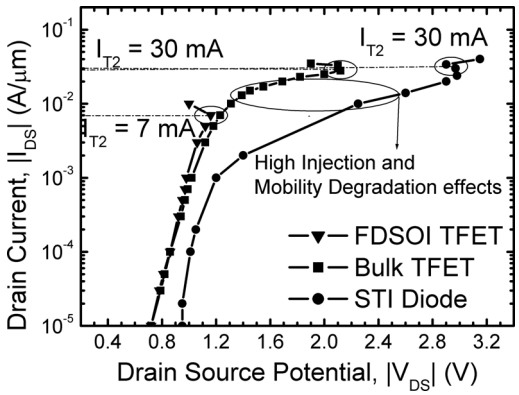

FIGURE 17. VFTLP characteristics of FDSOI TFET, bulk TFET and STI Diode during negative ESD stress at the drain of the TFET and cathode of the STI diode.

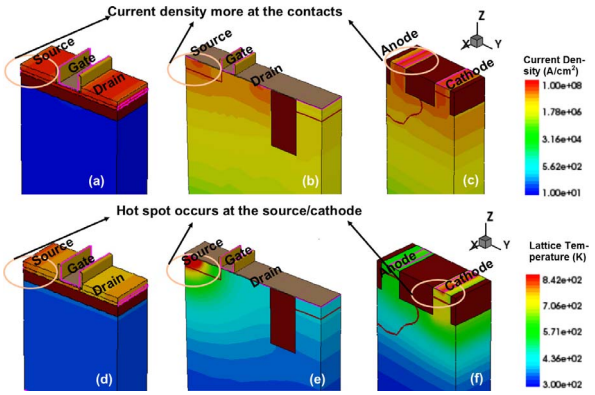

FIGURE 18. 3D process and device simulated structures showing current density and hot spot location in FDSOI TFET, bulk TFET and STI diode during negative VFTLP pulse at the drain of the TFET and cathode of the STI diode.

temperature shown in Fig. 18 (d, e, f) indicates the failure mechanism is due to contact melting, hence the robustness of the TFET and STI diode are limited to the number of contacts and the uniformity of layout.

IV. ADVANTAGES OF TFET IN ESD

Advantages of the TFET from ESD perspective can be analyzed from two dimensions (1) TFET as a load to be protected from an ESD event (2) TFET itself as an ESD device. TFET is an excellent load compared to the CMOS load for three reasons. First, the failure voltage (V_{T2}) of the TFET is 6-7 V even in the on-state because of the reverse bias diode breakdown mechanism compared to the parasitic bipolar turn-on of NMOS load. This voltage is 2-3 V higher compared to the V_{T1} of the parasitic bipolar turn-on mechanism of NMOS in 28 nm and below technology nodes [28]. Hence the ESD design window is increased compared to the MOSFET based load as shown in the Fig. 19 which provides the good margin for ESD engineers. Second, TFET based CMOS logic contains stacked PTFET and NTFET which is two gated diodes connected from the internal net to the supply voltage and ground respectively. This if properly designed can act as a self-protected ESD driver. Third, for the

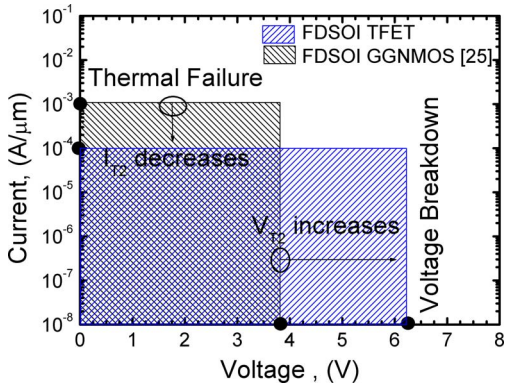

FIGURE 19. ESD design window available for the designers for the FDSOI TFET and NMOS as the load.

TFET based logic used in core of the IC, the charges stored in the internal nets during a CDM event gets discharged efficiently due to the gated diode architecture compared to the parasitic diode conduction in the CMOS logic circuits.

TFET cannot be used as primary ESD device in the conventional ESD network nor as a static ESD protection device like gate grounded TFET similar to gate grounded NMOS for the failsafe applications because of the poor drive current and low failure current per unit area. Hence there can be only novel or unconventional ways of using this device in the ESD network. We have proposed one way of using TFET utilizing the bi-directional current conducting nature and fast turn-on mechanism of the TFET which would be explained in the next section.

V. PROPOSED ESD NETWORK

Fig. 20 shows the proposed TFET based ESD network and the conventional STI diode based ESD network. In the proposed TFET based ESD network, the gate signals of the TFET's are connected to the trigger signal of the supply clamp circuit through a separate trigger rail. The trigger circuit, the supply clamp and the ESD network are explained in [29]. When the positive ESD stress is given at the I/O pad, the TFET connected between pad and supply (VDD) rail of Fig. 20 conducts in diode mode turning on the trigger circuit placed in the supply pad, this further polarizes the trigger rail and hence turning on all the TFETs. For the three pad configuration shown in the Fig. 20, we obtain three additional current paths compared to the single current path of the conventional STI diode based ESD network. The ESD characterization and network functionality will be discussed as follows.

A. HBM/CDM CHARACTERISTICS

Fig. 21 shows the HBM and CDM test circuit [12] used in the simulations, the DUT mentioned is the conventional and proposed ESD network with the I/O pad and ground to be stressed as shown in Fig. 20. Both the standards differ by the resistor, inductor and capacitor values used. CDM test

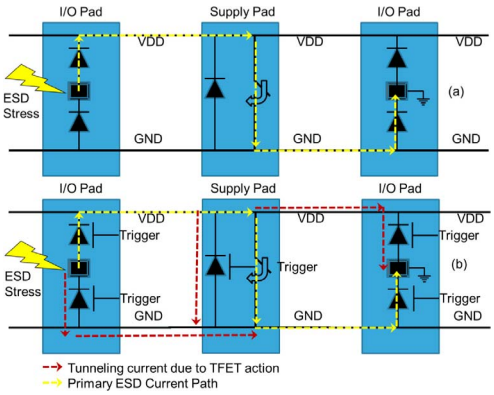

FIGURE 20. ESD current paths of the (a) conventional ESD network (b) proposed TFET based ESD network in three I/O pad configuration.

circuit have lesser resistance (∼ 20 Ω) which gives a damped oscillatory response, whereas HBM response is completely damped because of 1.5 k Ω resistor. Please note that the CDM test circuit used in our simulation is indicative and used only for the purpose of performance comparison. The exact test circuit used to ESD qualification will be different for different test-chips and its R, L, C parameters are package dependent [12]. The network optimization, diode size and clamps are designed to qualify 2 kV HBM target. Fig. 22 shows the HBM response of the TFET and STI based ESD network. The graph is plotted in the logarithmic scale to have clear understanding of triggering behavior during nano-second regime. For the duration lesser than 100 ps, TFET based ESD network show lesser stress voltage compared to STI diode based ESD network for both 2 kV and 3 kV HBM stresses. The faster turn-on behavior and higher leakage current of the TFET results in the reduction in the maximum voltage seen at the I/O pad. However, the peak voltage is same for 2 kV HBM stress and a 0.5 V reduction of the peak voltage is observed for 3 kV HBM stress indicating only the marginal improvement compared to STI diode based ESD network. This is because of the low drive current silicon TFETs used in our simulations. Higher drive current TFETs [30] are expected to provide better HBM response. The advantage of TFET based ESD network is clearly observed in the CDM response shown in the Fig. 23. For both 125 V/3.5 A CDM and 250 V/7 A CDM, we see a peak voltage reduction 3-4 V in the TFET based ESD network. We also observe the voltage increase of 5 V at the I/O pad from 125 V CDM to 250 V CDM stress for STI diode based ESD network and the voltage increase of only 2 V is observed in the case of TFET based ESD network, hence a voltage regulation mechanism is observed in the latter case explained in detail in the following section.

B. TLP/VFTLP CHARACTERISTICS

The TLP and VFTLP response of the conventional and proposed ESD network are shown in the Fig. 24 and Fig. 25 respectively. When the positive ESD stress is applied

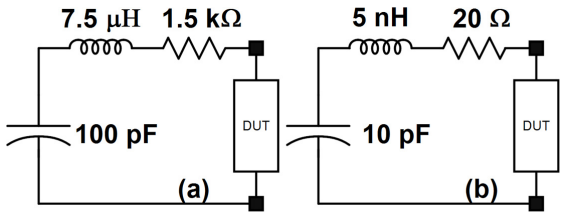

FIGURE 21. (a) HBM Test circuit (b) CDM Test Circuit used in our simulations.

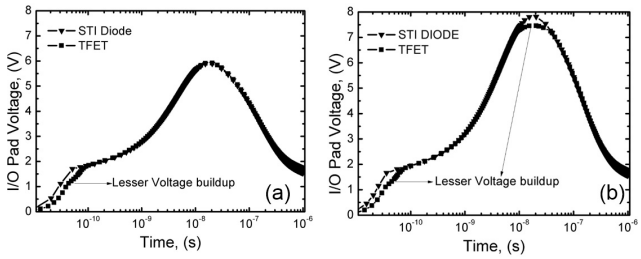

FIGURE 22. (a) 2 kV HBM response (b) 3 kV HBM Response of STI Diode and TFET based ESD networks.

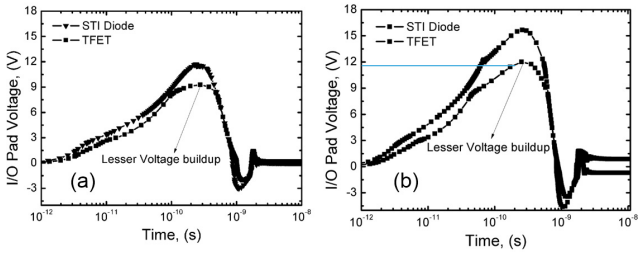

FIGURE 23. (a) 125 V CDM response (b) 250 V CDM Response of STI Diode and TFET based ESD networks.

on I/O pad P1 with the I/O pad P2 grounded, the following current paths can be possible for both STI diode and TFET based ESD network, the primary current path is (T1, C1 and T4) which is called as current_path_1. Additional secondary current paths include (T1, T3) and (T2, T4) which are called as current_path_2 and current_path_3 respectively. The magnitude of the current carried by the different current paths and its ESD implications are discussed in detail below,

B.1. I_TLP = 1.5 A

In this case, we have given a TLP current pulse of 1.5 A to the pad P1 with pad P2 grounded. This current level approximately corresponds to 2 kV HBM stress. From Fig. 24, we observe a maximum voltage at the pad P1 (6.8 V) is same for both STI diode and TFET based ESD network. This is due to the lower drive current of the silicon TFETs used in our work. The secondary current_path_2 and current_path_3 carries only 1.3 mA and 3.8 mA respectively. Hence the TFET based ESD network is not advantageous for the targeted HBM specification of 2 kV. Another important observation from the simulation results is that the current through the T3 is higher compared to the T2 though the V_{DS} is same for both the transistors. This is due to the higher overdrive

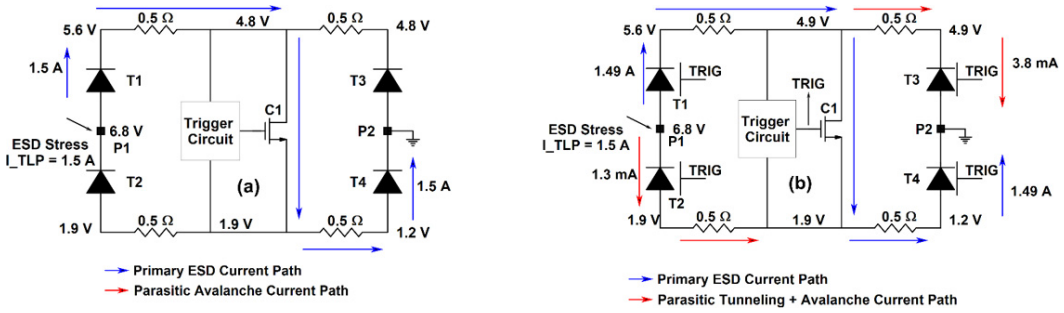

FIGURE 24. 1.5 A TLP response of (a) STI Diode and (b) TFET based ESD network.

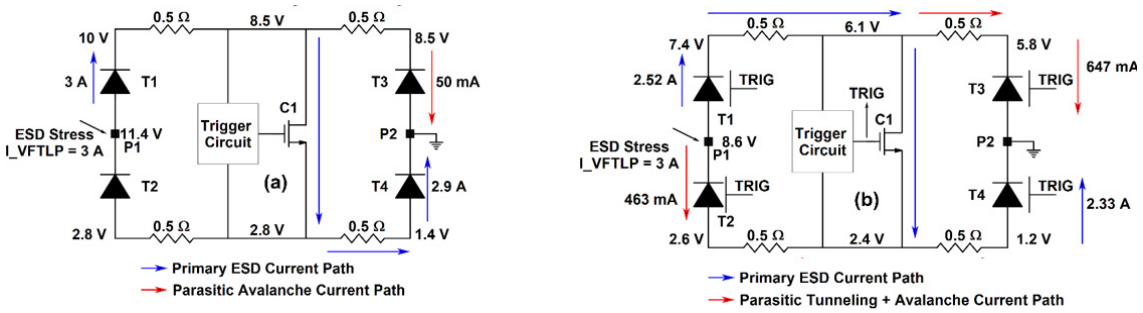

FIGURE 25. 3 A VFTLP response of (a) STI Diode and (b) TFET based ESD networks.

voltage (V_{GS}) seen at the gate of the T3 ($\sim$ 4.9 V) compared to the gate of the T2 (4.9V − 1.9V = 3 V).

B.2. I_VFTLP = 3 A

In this case, we have given a VFTLP current pulse of 3 A which corresponds to 125 V CDM stress. From Fig. 25, we observe a maximum voltage of 11.4 V and 8.6 V at the pad P1 of the STI diode and TFET based ESD network respectively. This 2.8 V reduction in the maximum voltage is due to the increased current flow in the secondary current paths. The T2 and T3 carries 463 mA and 647 mA. The V_{DS} and V_{GS} of 5.8 V is exactly at the Zener tunneling assisted avalanche generation regime. It should be noted that the triggering voltage of the load is assumed to be greater than 6 V, hence this additional current paths safely discharge the CDM current. However, in the case of STI diode, the maximum voltage difference across two nodes is greater than 8.6 V which may lead to CDM failure. Even with 250 V CDM stress, the maximum voltage difference across two nodes is less than 7.1 V. In the real scenario, with multiple I/O pads in the chip, there can be multiple tunneling current paths which clamp the voltage to Zener voltage of 5.5 V – 7 V. Hence it's clearly evident that the TFET based ESD network is advantageous at higher current levels especially during the CDM regime which is a major reliability concern in the advanced technology nodes.

VI. CONCLUSION

In this paper, we have discussed the quasi-static behavior of the bulk and FDSOI tunnel field effect transistor (TFET) during electrostatic discharge (ESD) stress conditions. From DC characteristics, we have shown that the TFET exhibits higher leakage current compared to STI diode. The better scalability of TFETs can be advantageously used for area optimization. During positive ESD stress at the drain, tunneling current reduced the potential build up resulting in reduced on-resistance. During negative ESD stress, TFET characteristics are similar to forward biased gated diode and hence exhibits lesser on-resistance compared to STI diode. The bulk TFET showed enhanced ESD behavior compared to FDSOI TFET because of reduced thermal resistance. The proposed TFET based ESD network is shown to exhibit enhanced CDM performance. With evergreen research interests in novel TFET device for improved figure of merit, we believe our proposed TFET based ESD network brings a significant value proposition in designing the ESD solutions for the future SOCs.

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