Received 19 September 2017; revised 5 January 2018 and 30 January 2018; accepted 13 February 2018. Date of publication 16 February 2018; date of current version 2 March 2018. The review of this paper was arranged by Editor K. E. Moselund.

Digital Object Identifier 10.1109/JEDS.2018.2806930

Current Collapse-Free and Self-Heating Performances in Normally Off GaN Nanowire GAA-MOSFETs

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This work was supported in part by the National Research Foundation of Korea funded by the Korea Government under Grant 2013R1A6A3A04057719, and in part by the 2214-A Coded International Doctoral Research Fellowship Program from TUBITAK, Turkey.

ABSTRACT Normally off lateral GaN nanowire gate-all-around MOSFETs have been fabricated on the GaN-on-insulator substrate. The dynamic measurement proved that the devices with various nanowire heights exhibit current collapse-free characteristics implying that the electrons in the isolated nanowire channel do not suffer from trapping effects. However, the dc current level measured at high drain and gate voltage is reduced to approximately one half of the value measured in dynamic mode. This is attributed to the difficulty in heat dissipation because the suspended lateral nanowire channel is thermally isolated from the substrate. However, the heat dissipation is mitigated as the nanowire size increases.

INDEX TERMS GaN, MOSFET, nanowire, gate-all-around, GaN-on-insulator, dynamic mode, self-heating.

I. INTRODUCTION

AlGaN/GaN-based high electron mobility transistors (HEMTs) have shown great advantages for high power and high frequency applications due to the superior material properties such as wide bandgap, high critical electric field, and high two dimensional electron gas density (2DEG) formed at the heterointerface [1]. High 2DEG density is induced by spontaneous polarization of III-nitride semiconductor itself and piezoelectric polarization caused by large strain due to large lattice mismatch between AlGaN and GaN. The polarization-induced 2DEG can be sensitively changed by external force, which is very useful for sensing applications, such as pressure sensor or inertial sensor [2]–[4]. In addition, the 2DEG density can be changed according to the surface charge states of the AlGaN/GaN HEMTs, which explains that the AlGaN/GaN HEMTs can be used as a good chemical or bio-sensor [5]–[8].

Recently, three dimensional (3D) gate structures, such as triple-gate [9]–[12], omega-gate [13], [14], and gate-all-around (GAA) [15], [16], have been demonstrated. These GaN-based 3D transistors have exhibited greatly improved performance compared to those of the conventional planar AlGaN/GaN HEMTs mainly due to the better gate controllability [9]–[14], even though they require additional fabrication processes. The fabricated 3D GaN transistors have many advantages, such as the normally-off operation, low knee voltage, and extremely low off-state leakage current, even though they suffer from relatively low on-current because the electron mobility of the nanowire channel is lower than that of the 2DEG channel. The current drivability of the devices can be improved with optimally designing the nanowire arrays, such as increasing the size of the nanowire or increasing the number of the nanowires which can be simply achieved by the device layout.

Lateral-type GaN nanowire GAA-MOSFET has been successfully fabricated by our group using GaN-on-insulator (GaNOI) wafer [15]. The nanowire channel of the device was completely suspended from the sapphire substrate

with selective removal of the underlying buried oxide layer and was wrapped with the gate insulator and the gate metal. This nanowire channel with GAA structure has no parasitic buffer layer and hence may completely resolve the problems related to the trapping effects. The trapping effects in the buffer layer of the conventional planar AlGaN/GaN-based HEMTs occasionally lead to a severe current collapse, which is one of the major reliability issues, because it severely reduces the drain current and subsequently increases the on-resistance of the device [17].

In this work, the static and the dynamic I-V characteristics were measured to discuss the trapping and thermal effects for the GaN nanowire GAA-MOSFETs fabricated on GaNOI [15]. Both trapping and self-heating effects are very important for the reliable device operation, because the trapping and the self-heating effect can cause reduction in the drain current due to the decrease in 2DEG density and due to mobility degradation, respectively.

II. GROWTH AND DEVICE FABRICATION

The schematic configuration of the fabricated GaN nanowire GAA-MOSFET is shown in Fig. 1(a). The device fabrication process with top-down approach was similar to that described in [15]. The starting GaNOI wafer, prepared by Smart Cut technology from SOITEC, consists of 150 nm-thick GaN layer and 800 nm-thick buried SiO_2 layer deposited on the sapphire substrate [18]. The 150 nm-thick GaN layer was defined by electron-beam lithography and patterned by inductively-coupled plasma-reactive ion etching. The nanowire array became suspended after removing the buried SiO_2 layer in buffered oxide etchant. Selective regrowth of 50 nm-thick undoped GaN layer and 20 nm-thick $Al_{0.3}Ga_{0.7}N$ layer in metal-organic-chemical deposition (MOCVD) reactor was then performed on the region outside the patterned nanowire array to form 2DEG (the inset of Fig. 1(a)). The 2DEG in the source and drain regions is beneficial for reducing the series resistance of the device, which results in low on-resistance of the device. Hall effect measurement showed 2DEG density of 9.75×10^{12} cm^{-2} and electron mobility of 1630 $cm^2 \cdot V^{-1} \cdot s^{-1}$. The sequential atomic layer deposition (ALD) of 20 nm-thick Al_2O_3 gate insulator and 10 nm-thick TiN gate metal was applied to complete the GaN nanowire GAA channel (Fig. 1). The fabricated nanowire devices have 64 triangle-shaped fingers with nanowire height from 114 nm to 56 nm as shown in TEM images of Fig. 1(c). The conventional planar AlGaN/GaN MISHEMT with gate length of 4 μm and width of 27 μm as a reference device was also fabricated on the different GaNOI wafer which was not patterned, but has same regrown layers described above.

III. RESULTS AND DISCUSSION

Fig. 2 show the output I_{ds} - V_{ds} curves in static and dynamic modes for the fabricated GaN nanowire GAA-MOSFET with V_{th} of 3.5 V (56 nm nanowire height). For the measurement

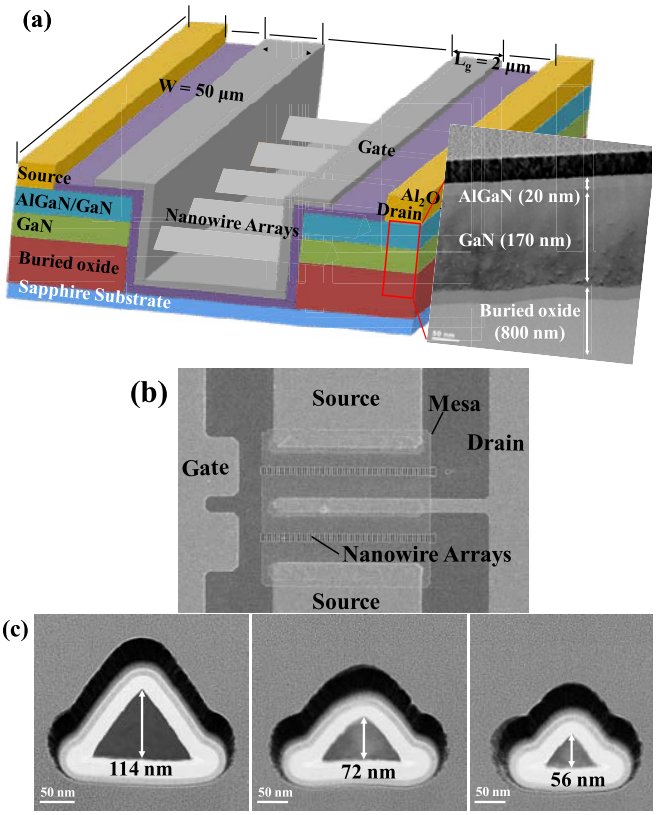

FIGURE 1. (a) Schematic illustration and device dimension of the proposed GaN nanowire GAA-MOSFET. Inset is the cross-sectional TEM image of AlGaN/GaN stack layers on buried oxide deposited on the sapphire substrate. (b) The overall SEM image of the real device. The nanowire arrays are fully covered with 20 nm-thick Al_2O_3 gate dielectric and 10 nm-thick TiN gate metal. (c) TEM images of GaN nanowire GAA structure with various nanowire heights from 114 nm to 56 nm.

in dynamic mode, pulses with 1 ms duration and 0.5 ms separation were applied to the gate and the drain. The reason why the short pulse width was not used for the measurement is because the minimum pulse width in our pulse measurement set up (Agilent B1501) was 1 ms. To evaluate the gate and drain lag, the drain voltage was swept from 0 to 10 V at different $V_{gs} = 0 \sim 8$ V (1 V step). Three different bias-point conditions were set at (1) $V_{gs,Q} = V_{ds,Q} = 0$ V, (2) $V_{gs,Q} < V_{th}$ and $V_{ds,Q} = 0$ V, and (3) $V_{gs,Q} < V_{th}$ and $V_{ds,Q} = 10$ V. However, no gate and drain lag were observed from the fabricated GAA-MOSFET, as shown in Fig. 2(b). The normalized maximum drain current ($I_{d,max}$) values for static and dynamic mode at V_{gs} of 8 V, divided by the source and drain pad width of 50 μm, are 2.2 mA/mm and 4.2 mA/mm, respectively.

The static and dynamic I_{ds} - V_{ds} curves of the nanowire devices with 72 nm and 114 nm nanowire height are presented in Fig. 3. The devices also exhibit negligible current collapse with normally-off operation with V_{th} of 2.5 and 1.5 V for the device with nanowire height of 72 and 114 nm, respectively. The normalized $I_{d,max}$ values with 72 nm nanowire device at V_{gs} of 8 V are

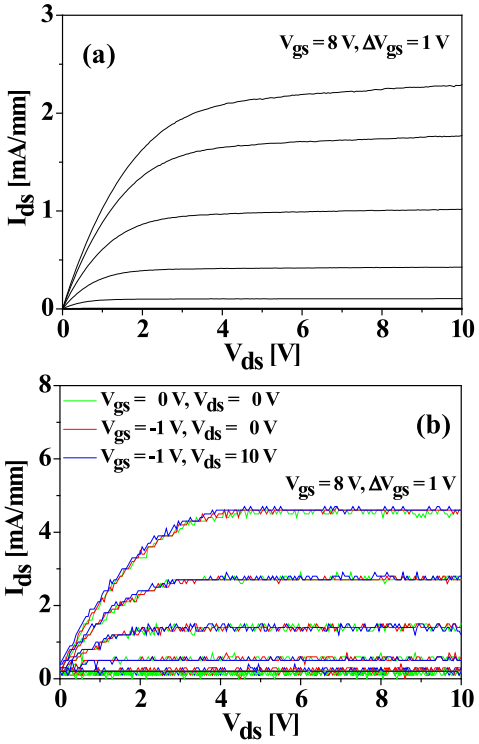

FIGURE 2. (a) Static I_{ds} - V_{ds} curve of a 56-nm-height GaN nanowire at various V_{gs} values (from 0 to 8 V). (b) Dynamic mode I_{ds}-V_{ds} characteristics of the GaN nanowire GAA-MOSFET. Red line: dynamic drain current at $V_{ds,Q} = V_{gs,Q} = 0$ V. Green line: dynamic drain current at $V_{ds,Q} = 0$ V and $V_{gs,Q} < V_{th}$. Blue line: dynamic drain current at $V_{ds,Q} = 10$ V and $V_{gs,Q} < V_{th}$.

8.1 mA/mm and 11.2 mA/mm and increases to 13.7 mA/mm and 17.7 mA/mm for static and dynamic mode, respectively, as the nanowire height increases to 114 nm. This indicates that the current capability of the nanowire device can be improved with increasing the size of the nanowire with maintaining a normally-off operation. This current collapse-free performance for the proposed devices can be expected from the fact that the suspended nanowire channel has basically buffer-less structure and hence the electrons in the channel do not suffer from the trapping into the buffer layer.

On the other hand, the normalized $I_{d,max}$ for the reference AlGaN/GaN planar MISHEMT at V_{gs} of 0 V is 38.5 mA/mm (divided by the total gate width of 27 μm), as shown in Fig. 4(a). The normalized $I_{d,max}$ for dynamic mode is 43 mA/mm at $V_{gs,Q} = V_{ds,Q} = 0$ V and drastically deceases to 10 mA/mm at $V_{gs,Q} < V_{th}$ and $V_{ds,Q} = 10$ V (Fig. 4(b)), showing that the reference device suffers from severe gate and drain lag due to significant trapping effects in buffer layer.

Although the trapping effects are, in general, detected with short pulse width (< 2 μs), we could observe the trapping effect with longer pulses [19]. While the nanowire device does not experience current collapse due to the trapping effect (Fig. 2(b), 3(b), and 3(d)), the reference AlGaN/GaN

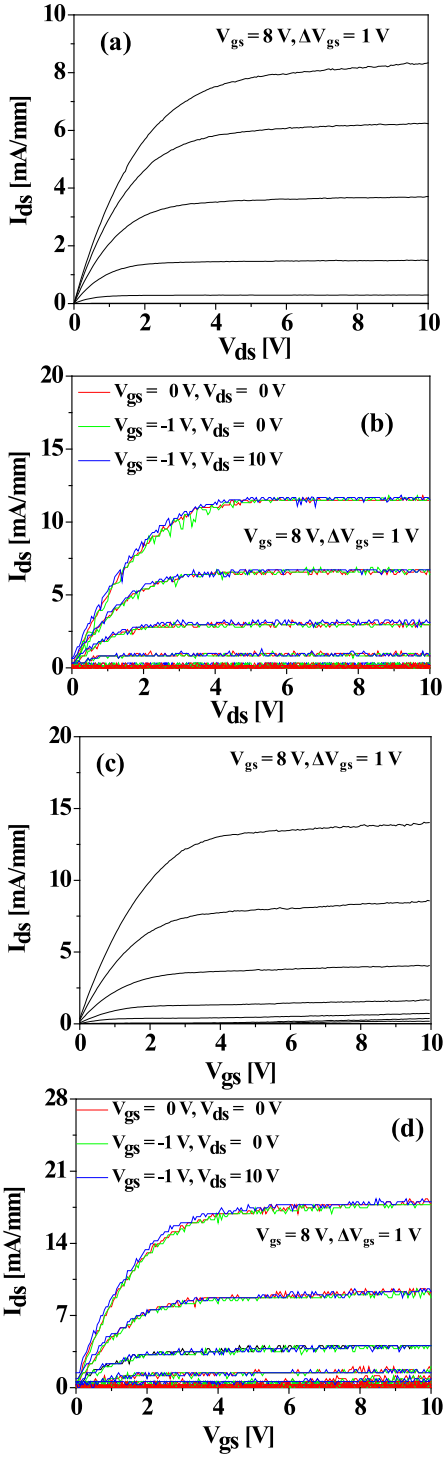

FIGURE 3. (a) Static and (b) dynamic mode I_{ds} - V_{ds} curve of a 72-nm-height GaN nanowire at various V_{gs} values (from 0 to 8 V). (c) Static and (d) dynamic mode I_{ds} - V_{ds} curve of a 114-nm-height GaN nanowire at various V_{gs} values (from 0 to 8 V). Red line: dynamic drain current at $V_{ds,Q} = V_{gs,Q} = 0$ V. Green line: dynamic drain current at $V_{ds,Q} = 0$ V and $V_{gs,Q} < V_{th}$. Blue line: dynamic drain current at $V_{ds,Q} = 10$ V and $V_{gs,Q} < V_{th}$.

planar MISHFET exhibits severe current collapse (Fig. 4(b)), even though the measurement was carried out with 1 ms pulse (equipment limitation).

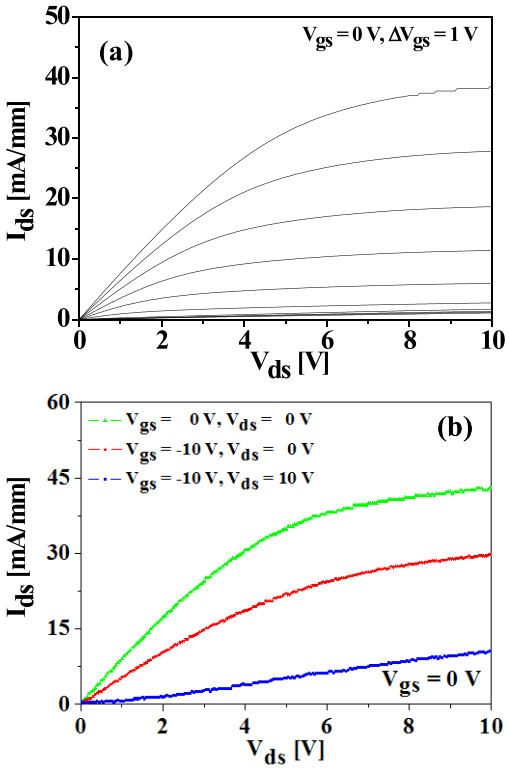

FIGURE 4. (a) DC I_{ds} - V_{ds} curve of AlGaN/GaN planar-type MISHEMT (reference device) at various V_{gs} values (from -10 to 0 V). The reference device exhibits normally-on operation with threshold voltage of −7 V. (b) Pulsed I_{ds}-V_{ds} curves of the reference device. Green triangle circle line: dynamic drain current at $V_{ds,Q} = V_{gs,Q} = 0$ V. Red star line: dynamic drain current at $V_{ds,Q} = 0$ V and $V_{gs,Q} < V_{th}$. Blue square line: dynamic drain current at $V_{ds,Q} = 10$ V and $V_{gs,Q} < V_{th}$.

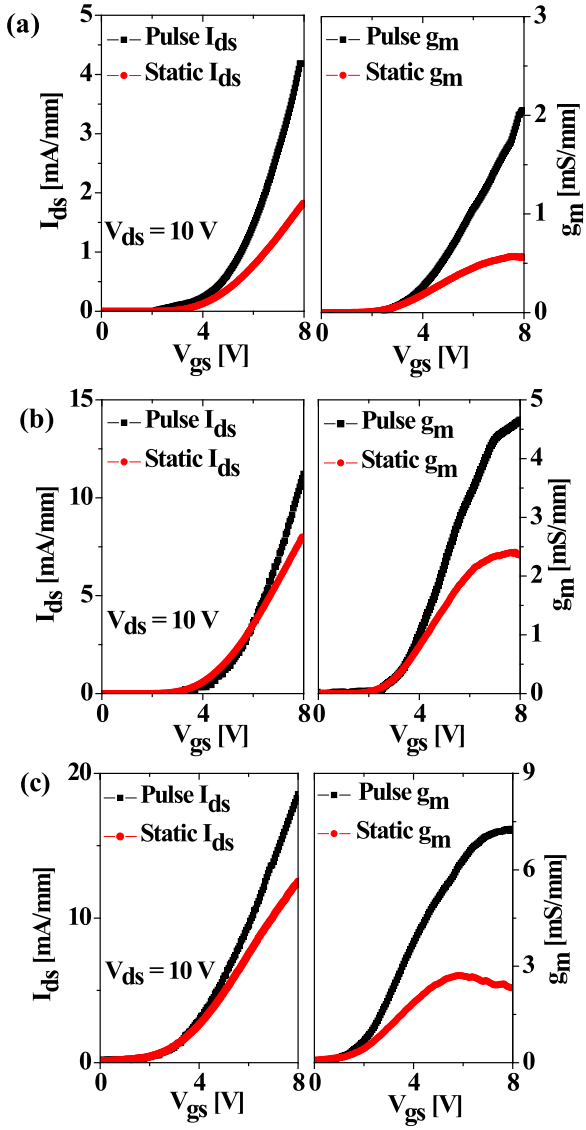

FIGURE 5. Drain current and transconductance versus gate voltage in static and dynamic modes for a GaN MOSFETs with nanowire height of (a) 56 nm, (b) 72 nm, and (c) 114 nm, respectively. ($V_{ds,Q} = V_{gs,Q} = 0$ V).

It is noticed in Fig. 2(a) and Fig. 5(a) that the maximum drain current of the nanowire GAA-MOSFETs with 56-nm-height measured in dynamic mode almost doubles that obtained in static mode, which is unusual in conventional planar-type AlGaN/GaN-based HEMTs. Furthermore, the transconductance (g_m) in dynamic mode continually increases as the gate voltage increases, whereas in static mode g_m saturates and slightly decreases at gate voltage of 8 V. This difference in device performance is attributed to heat generation caused by current flow in static mode operation. The GAA structure with 56 nm nanowire hardly dissipates the heat generated in the nanowire channel during DC measurements because the channel is thermally isolated from the substrate. Heat accumulation in the channel thus considerably increases the channel temperature which in turn decreases the electron mobility and the drain current. However, the difference of maximum drain currents in between static and dynamic mode becomes small as the nanowire size increases (Fig. 3 and Fig. 5). This tends to indicate that the heat generation due to the current flow is less critical in taller nanowires.

Numerical simulations including the self-heating effect to estimate the channel temperature were performed using Giga module of Silvaco ATLAS [20]–[22]. In the Giga module, the heat conduction equation is coupled to the Joule heating term with the drift-diffusion equations of the carriers. Poisson's equation and continuity equations for electrons and holes are solved, and a drift-diffusion model is used to solve transport equations. In addition to the drift–diffusion and Poisson equations with Fermi-Dirac statistics, carrier generation, and Shockley-Read-Hall recombination, carrier velocity saturation, and self-heating effects were also considered. The Farahmand Modified Caughey Thomas model defined in Silvaco ATLAS was also used as mobility model and details were given in [21]–[23]. In our case, the hole was not calculated. The bottom of the structure was set to a fixed temperature of 300 K but do not introduce additional thermal resistance at the bottom of the simulated structure in order to obtain temperature

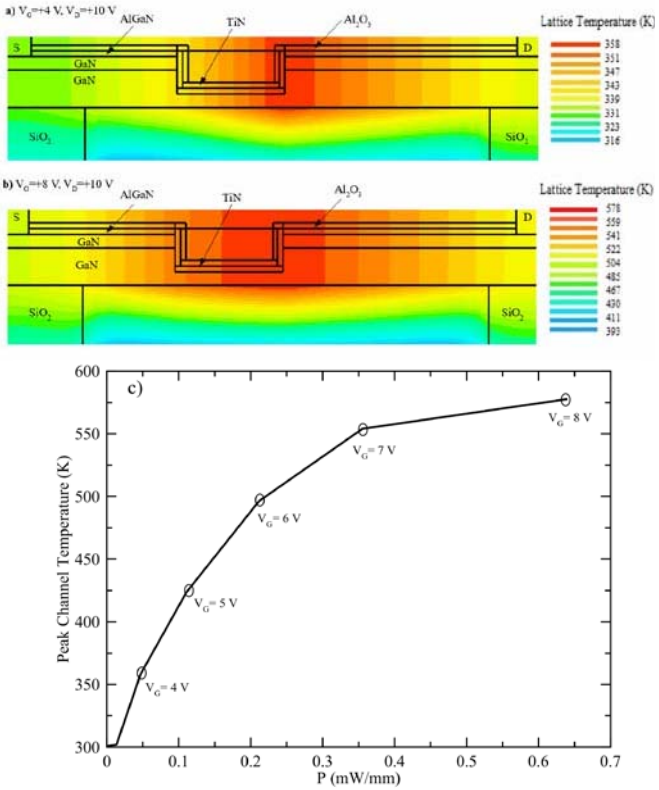

FIGURE 6. Cross sections of the lattice temperature distribution in simulated GaN nanowire GAA-MOSFET by Silvaco ATLAS at (a) $V_{gs} = 4$ V and $V_{ds} = 10$ V, and (b) $V_{gs} = 8$ V and $V_{ds} = 10$ V. (c) The peak channel temperature versus applied power.

distribution. The thermal conductivity of GaN nanowire channel layer was assumed as 1.3 W/cm·K [23]. The room-temperature thermal conductivity of sapphire, AlGaN and SiO_2 used for GaN nanowire MOSFET were 0.29, 0.3 and 0.014 W/cm·K, respectively [20]–[24]. In the simulations, it was also assumed that the interface trap density in GaN/SiO_2 is about 4×10^{11}cm^{-2} with $E_C - 0.8$ eV [25].

Fig. 6(a) and (b) show the cross-section of the simulated lattice temperature distribution for 56-nm-height nanowire device at $V_{ds} = 10$ V and $V_{gs} = 4$ V, and $V_{ds} = 10$ V and $V_{gs} = 8$ V. The simulation shows the heat dissipation pathway is limited only along the nanowire channel and hence the heat accumulation in the channel increases the channel temperature considerably. The peak channel temperature reaches 358 K and 578 K near drain edge of the gate which is responsible for the decrease of the electron mobility at $V_{gs} = 4$ V and $V_{gs} = 8$ V for fixed $V_{ds} = 10$ V [26], [27]. This temperature-dependent mobility degradation explains the experimental difference in maximum drain current and g_m between the static and the dynamic mode characteristics. It is worthy of noting that the impact of self-heating is more pronounced in the mobility drop (by a factor of 3, Fig. 5). Assuming a conventional mobility-temperature law $\mu \sim T^{-1.5}$, we obtain an average temperature rise of 300 K. Indeed, the decrease in threshold voltage at high temperature tends to increase the drain current which drops only by a factor of 2. Also, the peak channel temperature versus applied power is shown in Fig. 6(c).

IV. CONCLUSION

GaN lateral-type GAA-MOSFETs with triangle-shaped nanowire channels from 56 nm to 114 nm height have been fabricated on the GaNOI wafer. The dynamic measurement proved that the devices demonstrate current collapse-free characteristics due to the fully depleted and isolated wrapped gate structure without buffer layer regardless of nanowire height. It was also found that the device suffers from self-heating, which is mitigated by the increased nanowire size. The difference between static and dynamic measurement for 56-nm-hegiht nanowire device was confirmed by the thermal simulations.

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