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A SPDT RF Switch Small- and Large-Signal Characteristics on TR-HR SOI Substrates

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ABSTRACT This paper evaluates the small- and large-signal characteristics of a single pole double thru (SPDT) RF antenna switch including its insertion loss, isolation, and nonlinear behavior. It is fabricated on three different types of high resistivity (HR) silicon-on-insulator (SOI) substrates: one standard (HR-SOI) and two trap-rich (RFeSI80 and RFeSI90). Using a special test structure, the contribution of substrate and active devices is separated for both in small- and large-signal. It is shown that by using trap-rich substrate technology, a reduction of over 16 dB of 2nd harmonic is achieved compared with HR SOI substrate. In off-state, it is shown that 35 dB increase of harmonic level is due to the nonlinearity of active devices. The effect of body bias on small- and large-signal FoMs of the SPDT is investigated and discussed. It is illustrated that trap-rich HR-SOI substrates having much thinner BOX, still outperform classical HR-SOI wafer.

INDEX TERMS RF switch, SOI, trap-rich (TR), RFeSI, SPDT, harmonic distortion, insertion loss, isolation.

I. INTRODUCTION

The market of cellular components has been shifting rapidly from GaAs pHEMT or silicon-on-sapphire (SOS) [1] to silicon-based technology. CMOS (silicon-on-insulator) SOI antenna switches which are compatible with multimode GSM/EDGE, TD/WCDMA and LTE systems exhibit higher integration levels and became the fastest growing mobile phone submarket [2]–[6]. High volume Si CMOS and SiGe BiCMOS provide economy of scale over the III/V group semiconductor technology like GaAs pHEMT and silicon-on-sapphire (SOS) [7]. High resistivity (HR) SOI decouples FET body terminals enabling MOSFET stacking, allowing the design of high power antenna switch. The power capability of a SPDT antenna switch can be improved by stacking MOSFETs (placing them in series or cascoded). By applying this topology, the source/drain voltage will be divided on the number of the transistors which are in series and hence, the breakdown voltage increases. By using this configuration, total parasitic capacitance in off-state (C_{off}) dramatically decreases. However, more number of stacked results in an increase of the parasitic series resistance in on-state (R_{on}). An ideal RF antenna switch has low insertion loss in the signal path and high isolation from other paths and thus exhibits a time constant $R_{on}.C_{off}$ as low as possible. $R_{on}.C_{off}$ figure of merit is mainly process and device dependent and it becomes a more serious issue as the number of throw counts increases from SPDT to SP9T and beyond to meet a low C_{off} and R_{on} [8]. As reported in [9], by using the stress memorization technique (SMT), ultra-wideband RF switch performance is improved in which low measured insertion loss (IL) from DC to 50 GHz is obtained for the SPDT switch achieving low $R_{on}.C_{off}$ around 91 fs. However, the proposed SPDT in [9] shows weaker power handling compared to that in this work since the stacked topology is not applied. In [10] and [11], it is demonstrated that CMOS-SOI processes especially with thin Silicon have the potential to rival the FoM that was traditionally feasible only with GaAs technologies. This necessitates some trade-offs and optimizations in terms of FET and substrate that need to be considered in developing a high performance switch with high linearity and low $R_{on}.C_{off} < 200$ fs is achievable. Moreover, the nonlinearity of the RF switch coming from the substrate and the active devices in terms of harmonics and intermodulation distortion could be minimized by advanced substrate and

device process engineering. Advanced material engineering has been used to suppress the substrate contribution to the harmonics and intermodulation distortion. In the domain of SOI technology it is well established that introducing a trap-rich layer compatible with both the industrial SOI wafer production and with the thermal budget of standard CMOS process at the Si/SiO_2 interface is one of the most efficient techniques to overcome the problem of the substrate's effective resistivity degradation. This degradation is due to the formation of a parasitic surface conduction (PSC) region beneath the BOX because of fixed oxide charges (Q_{ox}) within it. The trap-rich layer aims at capturing the free carriers forming the PSC and thus allowing the substrate to retain its high nominal resistivity, leading to lower losses as well as improved linearity [12]–[14]. In this work, two types of trap-rich (TR) HR-SOI wafers denoted RFeSI80 and RFeSI90 as 1st and 2nd generations with 400 nm and 200 nm-thick BOX, respectively, provided by Soitec are used to study the effect of different substrates on a SPDT FoMs such as linearity and $R_{on}.C_{off}$. More characterization results of those commercialized substrates is reported in [15]. One standard HR-SOI with 1 μm BOX is also used to better show the superiority of TR technology by comparing them together. In this paper, the influences of both the transistor and the type of SOI substrate over nonlinear behavior of the studied RF switch (SPDT) are discriminated by measuring the second (H2) harmonic distortion levels achieved by large-signal characterization performed on the switch itself as well as on its special test structure counterparts. $R_{on}.C_{off}$, insertion loss and isolation are extracted from small-signal measurements and compared on 3 studied SOI substrates as well. In this way, the impact of different SOI substrates including classical HR-SOI and trap-rich (TR) HR-SOI having different nominal resistivities and buried oxide layer (BOX) thicknesses on RF switch figure of merits describing its performance is demonstrated. It is also shown that by using highly linear trap-rich HR-SOI substrates, for which the device itself is the dominant source of non-linearity (especially in off-state), the overall linearity of the full switch can be decreased by appropriately adjusting the body bias voltage of the transistors. It is shown that in comparison this is not the case for the same switches on HR-SOI wafers, as the dominant source of non-linearity is then the substrate.

II. TECHNOLOGY DESCRIPTION

In this work, the SPDT RF antenna switch and its special test structure counterparts are fabricated using TowerJazz's 1st generation 0.18 μm, 4-metal layer SOI CMOS process (CS18 2.5 V) on top of 3 different types of RF-SOI substrates. This process is a thin-SOI partially depleted process supporting floating body and body contacted devices. They are characterized and compared for $R_{on} - C_{off}$ and harmonic distortion levels. Since in this layout design we have an access to the body contact, the effect of body bias on small- and large-signal FoMs of the switch is demonstrated and their correlation is presented.

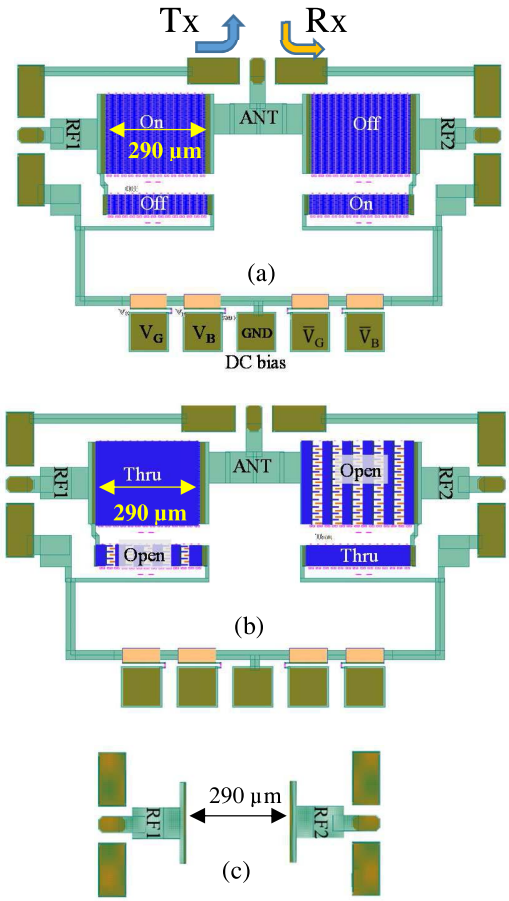

FIGURE 1. Layout of (a) SPDT switch, (b) Open/Thru test structure and (c) simple open-pad.

III. RF ANTENNA SWITCH (SPDT)

The SPDT switch has one transmit port (Tx) and one receive port (Rx) which are symmetrical (Fig. 1a). The on-state (NMOS) branches are biased with $V_G = 2.5$ V at the gate and $V_B = 0$ V at the body whereas the off-state (NMOS) branches are biased with $\overline{V}_G = \overline{V}_B = -2.5$ V at the gate and body to have minimum C_{off} and robust power handling in this condition [8]. It will be shown that in those bias conditions, the optimum results in terms of the main small- and large-signal FoMs, e.g., R_{on}, C_{off} and linearity could be achieved.

The designed layout of the SPDT RF switch is shown in Fig. 1a. Because of the symmetry in the SPDT structure (identical Tx and Rx parts), we only measure and investigate the Tx part in on- and off-state. As illustrated in Fig. 1b, a special test structure named "Open/Thru" is designed and fabricated on the same chip as the SPDT. In this design, the transistor's intrinsic parts are removed to eliminate their contribution and bring forward the substrate effect in measured characteristics. The on-state is simulated by replacing the devices active layer with metal-1 lines. The off-state is emulated by an open structure where all source-drain fingers are kept to better account for the extrinsic parasitic effects.

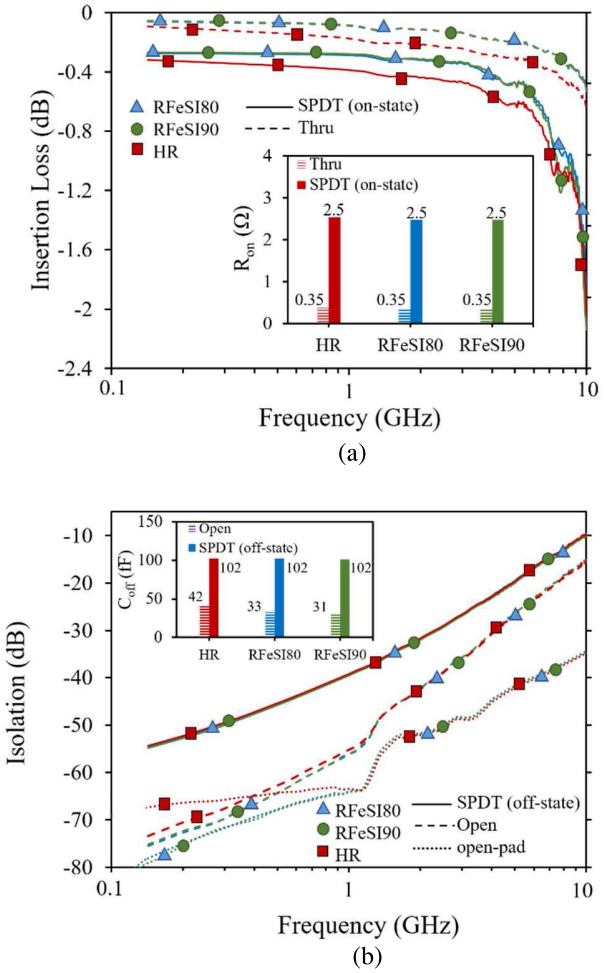

FIGURE 2. Comparison of (a) insertion loss and (b) isolation of the SPDT, Open/Thru and open-pad (only for isolation) structures on HR and TR wafers. The extracted R_{on} and C_{off} at 900 MHz are shown in the insets of the figures.

Finally, as can be seen in Fig. 1c, a simple open-pad structure with a pad distance of 290 μm is designed and included among the test structures. This pad distance is equal to that in the series branch of the SPDT and Open/Thru structures. By measuring open-pad, the pure effect of the substrate is extracted and compared with other test structures.

IV. MEASUREMENT DESCRIPTION AND RESULTS

A. SMALL-SIGNAL MEASUREMENT

On-wafer small-signal measurements of all test structures are performed in the frequency range between 10 MHz and 26.5 GHz.

To eliminate the effects of cable losses and connections from S-parameters, the off-wafer line-reflect-reflect-match (LRRM) right angle calibration method is used [16]. The RF insertion loss and isolation of the SPDT in on-state and Thru structure on HR and TR wafers are plotted in Fig. 2. The transmit insertion loss (Fig. 2a) is slightly higher in the SPDT than in the Thru structure because of higher transistor channel resistivity compared with metal-1.

At 900 MHz, the transmit insertion loss (S_{21}) in the SPDT switch is −0.38 dB and −0.28 dB for HR and TR substrates, respectively. The extracted R_{on} ($1/\mathrm{Re}(-Y_{12})$) in the SPDT (2.5 Ω) and Thru structure (0.35 Ω) is identical for all substrates. In fact, R_{on} mainly depends on transistor geometry and specification, i.e., channel parameters (length, width, doping, strain and etc.) and the bias condition. Lower insertion loss shown in the RFeSI wafer compared with HR confirms lower substrate losses even if the BOX thickness of the RFeSI wafers are up to 5 times thinner than in the case of HR. Beyond 5 GHz, the insertion loss increases dramatically which is due to the off capacitances corresponding to the shunt branches. Bigger C_{off} in the SPDT shunt branch compared with Thru/Open structure, results in sharper increase of insertion loss versus frequency as can be seen in Fig. 2a. In Fig. 2b, one can see that isolation of the SPDT (solid-lines) is substrate independent and the extracted C_{off} ($\mathrm{Im}(-Y_{12})/2\pi f$) for HR and TR substrates at 900 MHz are identical. Therefore, it can be observed that the high level of transistor C_{off}, dominates over the substrate's capacitance network thus the substrate coupling effect is not observable. Actually, C_{off} in transistors is mainly dominated by the top Si thickness and not the substrate. Indeed an off-capacitance value of around 102 fF is observed on all wafers. The weaker isolation of the SPDT switch compared with the Open structure or the open-pad structure is explained by the signal passing through the larger drain-source capacitances of the stacked transistors in the series branch (see inset of Fig. 2b). These capacitances correspond to relatively thin depleted regions between the source/drain of the device and the transistor body. Indeed, in the off state the entire channel is not depleted, but rather in a state of accumulation defined by $V_G = -2.5$ V. This is detailed further in Section V in which an analysis of the substrate's influence on C_{off} is discussed. The Open structure however has the active channel regions completely removed, and so only the device's extrinsic capacitances are contribute to the coupling. For these reasons the off-capacitance measured in the Open structure is far less.

By moving to the Open and open-pad structures the impact of the devices becomes partially and completely eliminated, respectively. In fact, by moving from SPDT to its Open structure counterpart, by decreasing the transistor's capacitive effect, the signal passes partially through the substrate and therefore a clear difference in C_{off} between classical and TR high resistivity SOI substrates is visible. Off-capacitances of 42 fF, 33 fF and 31 fF are extracted in the Open structure at 900 MHz for HR, eSI80 and eSI90 substrates, respectively. Still, for the Open structure most of the fields remain concentrated between the electrodes of the stacked switches (only active layer is removed) because the distance between two such electrodes is of the same order as the device length (280 nm), which in turn is of comparable size to the BOX thicknesses (1 μm, 400 nm and 200 nm), meaning that the fields only penetrate partially into the Si substrates. It is for this reason that only small differences between the HR and

TR options are observed. We further confirm the capacitive nature of the coupling by the slope of the isolation curve over frequency which remains close to 20 dB/decade. The differences become more pronounced below 1 GHz as the substrate carriers have time to respond to and follow the signal frequency (below the dielectric relaxation frequency of the substrate), and the curves start to flatten out slightly for the more conductive HR substrate (PSC effect). Even though the HR wafer has a considerably thicker BOX, it also shows an appreciably higher capacitance for the Open structure due to this high PSC effect.

On the other hand, for the open-pad structure the electrodes of the stacked devices are additionally removed. Then, the fields penetrate deeply into the silicon volume as the distance between the two pads is 290 μm. Below the substrate's dielectric relaxation frequency (around 1 GHz) the effect of the substrate becomes clearly visible, as illustrated in Fig. 2b. HR shows its parasitic conduction effect whereas TR presents its capacitive coupling behavior and differences of more than 10 dB (around 100 MHz) are observed between both types of substrate.

From all observations shown above in this part, it can be seen that the superiority of RFeSI substrates performance in terms of system isolation and insertion loss is well demonstrated even though the BOX is much thinner compared to the HR substrate.

B. LARGE-SIGNAL MEASUREMENT (HD)

Large-signal measurements are performed at the fundamental frequency of 900 MHz up to 40 dBm input power. By analyzing the results of Fig. 3a, it appears that both the substrate and the SPDT biased in on-state contribute independently to the overall non-linearity. The difference in H2 levels between the on-state switch and the Thru structure, on TR wafers or on HR-SOI, evidences a contribution of the transistors to the non-linearity of about 15 or 9 dB. Both the on-state SPDT and the Thru structure on RFeSI substrates exhibit significantly lower H2 levels than on HR-SOI.

At $P_{in} = 20$ dBm the RFeSI substrates present 16 dB and 19 dB improvements over HR for both the SPDT and Thru structure, respectively. From these observations we conclude that both the active device and the substrate are significant sources of non-linearity that are independent and add together in the on-state to yield the total non-linear distortion levels. It should be noted that the H2 levels remain below the standard −85 dBc curve all the way up to $P_{in} = 40$ dBm for the SPDT switches on both types of RFeSI substrates, making these designs compatible with RFIC standards.

By analyzing the results of Fig. 3b, it appears once again that both the substrate and the SPDT biased in off-state contribute independently to the overall non-linearity. The difference in H2 levels between the off-state switch and the Open structure, on TR wafers or on HRSOI, evidences a contribution of the transistors to the non-linearity of about 35 ∼ 38 dB. Both the off-state SPDT and the Open structure on RFeSI substrates exhibit slightly lower H2 levels than

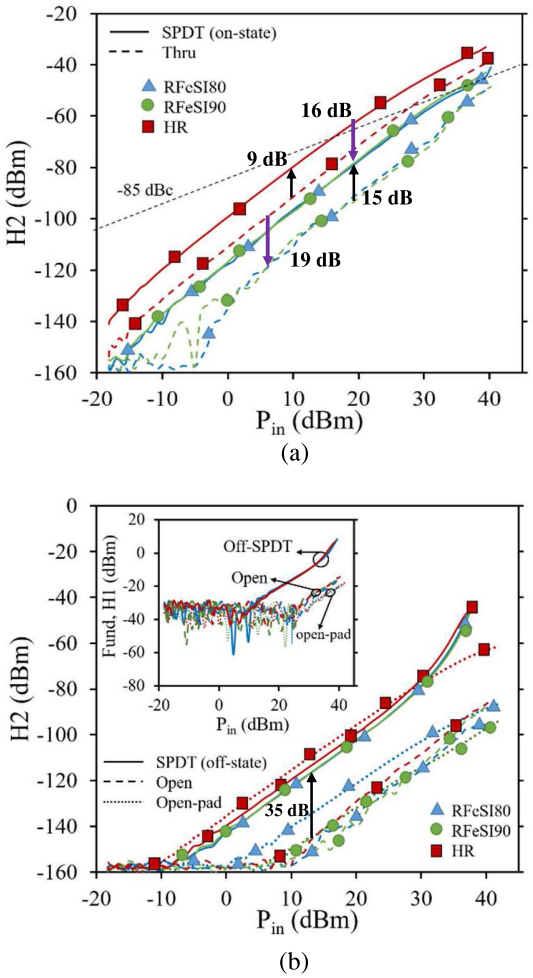

FIGURE 3. Measured H2 in (a) on-state and (b) off-state of the studied SPDT, Open/Thru and open-pad (only for off-state) structures on HR and two TR SOI substrates (RFeSI80 and RFeSI90) at 900 MHz. The fundamental output in off-state SPDT, Open and open-pad is shown in the inset.

on HRSOI. The reasons for which this difference is low are the same that explained the low differences in isolation between the TR and HRSOI options (presented in Section IV-A relative to Fig. 2b): for both the off-state SPDT and the Open structure almost all of the fields remain concentrated in or above the BOX because the device length (280 nm) is of significant size compared to the BOX thickness (1 μm, 400 nm or 200 nm), therefore explaining why the choice of the underlying substrate impacts very little on the measured non-linearity for these devices.

However for the open-pad structure, as shown in Fig. 3b, (dotted-lines) the electrodes of the stacked devices are additionally removed. Then, the fields penetrate deeply into the silicon volume as the distance between the two pads is 290 μm. These fields can then significantly modulate the electrical properties of the HR substrate, while those of the RFeSI substrates are fairly field-insensitive due to the large number of traps at the interface that effectively pin the Fermi-level to a narrow range of energies. We then observe a much higher linearity for both generations of RFeSI substrates over

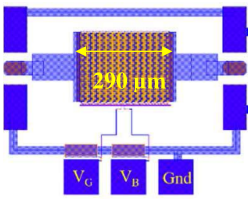

FIGURE 4. The layout of series branch used in the SPDT including 14 stacked transistors each one having 0.28 µm and 15 µm of channel length and width, respectively, with 267 fingers.

the HR substrate, with the most advanced RFeSI90 showing the highest linearity.

The inset in Fig. 3b illustrates the output fundamental signal (H1) in off-state, showing the incident signal wave leak to the output in SPDT and Open structure due to the parasitic off capacitances and in open-pad through the substrate. As illustrated in Fig. 3b, however, the lowest level of output signal is passed through the substrates by open-pad structure, the highest level of H2 is generated by the highly non-linear HR substrate even slightly more than that in the SPDT. This is translated to higher non-linearity of the HR substrate compared with active devices. Whereas, in TR wafers this is not the case and it can be seen that active devices generate much higher harmonics than the substrate.

As illustrated in Fig. 3b the lowest harmonic level is generated by Open structure in which we have only linear extrinsic capacitances of the transistors and signal is mainly bypassed by them. In this case, in eSI80 and eSI90, H2 stays always below −100 dBm since both the devices and substrate are linear. Finally, one can see that in open-pad structure which only monitors the substrate, RFeSI90 having the thinnest BOX of 200 nm shows a harmonic level identical to that of Open structure including linear extrinsic capacitances.

C. BODY BIAS EFFECT ON SMALL- AND LARGE-SIGNAL FOMS

TowerJazz's 0.18 µm technology offers an access to the body terminal of the transistors, and in this section of the paper the effect of body bias V_{body} on small- (R_{on} and C_{off}) and large-signal (linearity) FoMs in on- and off-states is investigated. For simplicity, the presented analysis is conducted on the main series branch of the SPDT which dominates the switch behavior. This dedicated test structure is designed on HR and both RFeSI substrates and is shown in Fig. 4.

Fig. 5 shows that in the on-state by increasing V_{body}, R_{on} decreases which directly correlates with a decrease of V_{th} (inset of Fig. 5). By changing the body bias from −4.5 V to 4.5 V, R_{on} varies by ∼ 9 %. The value of R_{on} depends on device geometry and not on the substrate type. In off-state, C_{off} shows a direct trend with V_{body}, i.e., by increasing the body bias from negative to positive values, C_{off} increases. Actually, off-mode transistors include parallel intrinsic and extrinsic parasitic capacitances which are parallel with the substrate capacitance network. Intrinsic capacitances of the transistors in off-mode are depletion capacitances which are

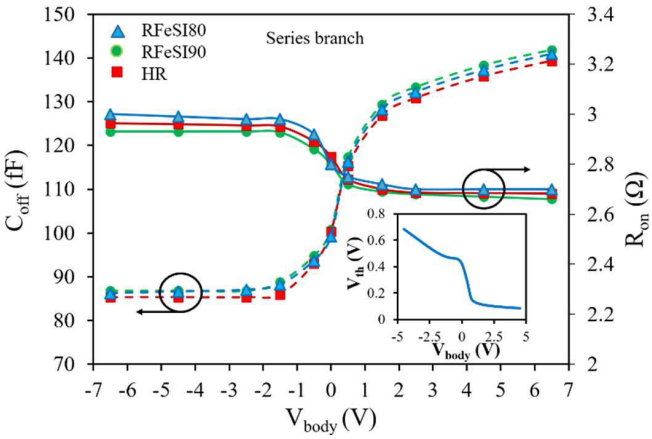

FIGURE 5. Extracted R_{on} and C_{off} versus V_{body} for series branch used in the SPDT switch on HR and two TR SOI substrates (RFeSI80 and RFeSI90). The threshold voltage (V_{th}) variation with the body bias is shown in the inset.

strongly dependent on V_{body} whereas, extrinsic ones are linear. As it is shown in the inset of Fig. 2b, C_{off} in SPDT is not substrate dependent since the capacitance network of the active devices are dominant. By varying V_{body} from 4.5 V down to −4.5 V, C_{off} decreases by 64 %. This is because the depletion regions of the PN junctions from n-type source/drain to p-type body are widened when a reverse bias is applied across them (by negative V_{body}), leading to a lower intrinsic capacitance of the transistor. From all above observation, it can be said that $V_{body} > 0$ V in on-state and $V_{body} < -0.5$ V in off-state lead to achieve low R_{on} and C_{off}.

In Fig. 6, the effect of body bias on non-linearity of the series branch in on- and off-state for HR and TR substrates is illustrated. The 2nd (H2) harmonic is recorded at an input power of 20 dBm and compared. The measurement results for on-state series branch on three studied substrates are shown in Fig. 6.a.

As can be seen in Fig. 6a, the body bias has no big impact on the non-linearity of the series branch in on-state on HR substrate where the substrate non-linearity is dominant. In highly linear TR substrates, the non-linearity is under the control of active devices and it is observed that H2 varies with body bias. For TR wafers, in on-state, the lowest level of non-linearity could be achieved at low level body bias $-0.5\text{V} < V_{body} < 0.5$ V. In off-state, as shown in Fig. 6b, negative values of V_{body} show dramatically decreased levels of harmonics. From Fig. 6b it can be observe that for $V_{body} < -1.5$ V, point at which the off devices becomes more linear, the substrate's effect becomes more pronounced. Above −1.5 V on the body the non-linearities appear to be dominated by the device itself, whereas below −1.5 V the substrate appears as the dominant source of non-linearity, and the two RFeSI substrates show more than 10 dB linearity improvements over HR, with the latest generation RFeSI90 showing the best characteristics.

However, in SPDT this difference becomes less due to the harmonic level increase originating from the shunt branch

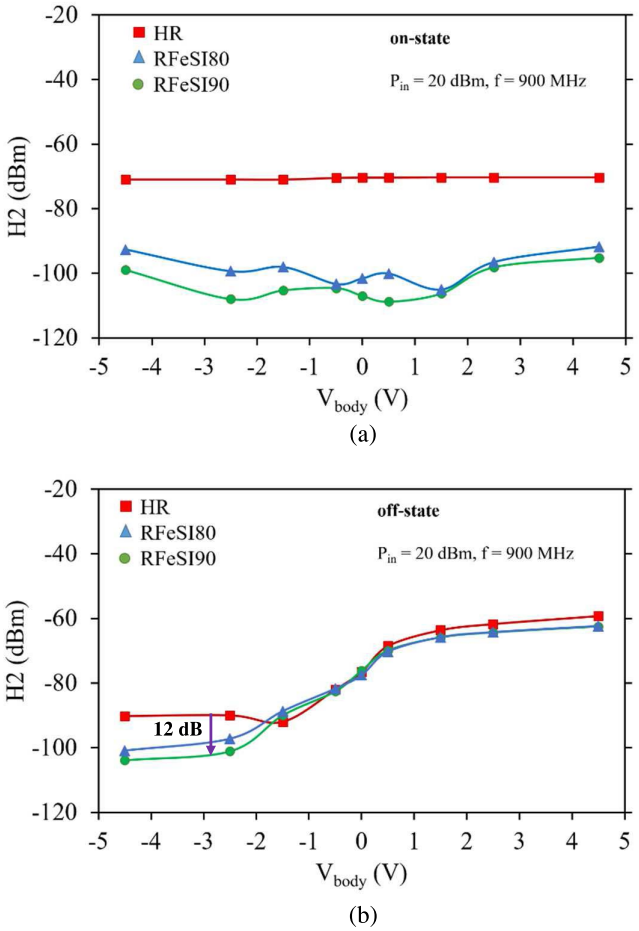

FIGURE 6. **The 2nd Harmonic measurement on the series branch used in the SPDT switch for different V_{body} on HR and two TR SOI substrates (RFeSI80 and RFeSI90) in (a) on-state and (b) off-state at 900 MHz and P_{in} = 20 dBm.**

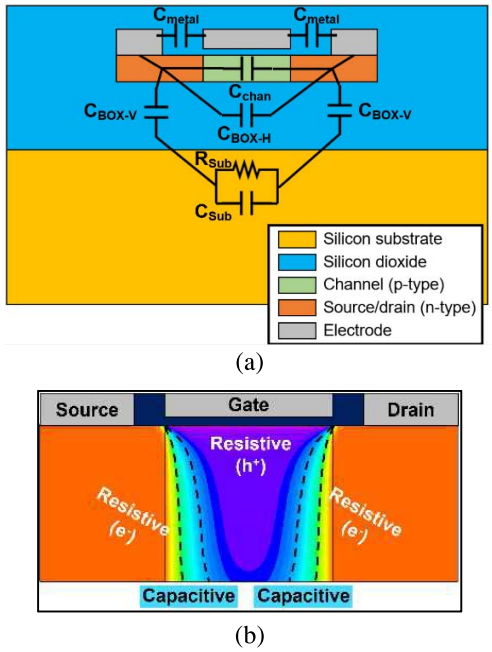

FIGURE 7. **(a) SOI transistor architecture overlaid with the parasitic coupling network between source and drain. (b) 2D carrier concentration distribution in the simulated SOI transistor with $V_G = -2.5$ V and $V_D = V_S = V_{body} = 0$ V.**

that will also contribute to the total system non-linearity. In the off-state, one can see that C_{off} and the non-linearity of the device change with the same trend versus V_{body}, i.e., higher C_{off} results in higher harmonic levels. Because the non-linear depletion capacitances in the device between the n-type source/drain regions and the p-type top channel are reduced for $V_{body} < 0$ V (Fig. 5), it makes sense for the harmonic to be reduced as the overall non-linear impedance is increased. As illustrated in Fig. 6b, in highly linear TR substrates, by continuing to decrease V_{body}, the non-linearity of the active devices, and therefore total second harmonic distortion level (H2), continues to decrease. In the HR wafer this is not the case because the non-linearity is dominated by the substrate. Therefore, by more decreasing V_{body} to negative values beyond −2.5 V, H2 does not decrease anymore and is stopped at around −90 dBm. Thus, in trap-rich substrates, the non-linearity of the switch in on- and off-state is under the control of the body bias.

V. ANALYSIS OF SUBSTRATE IMPACT

In this section we will investigate the impact of the substrate on RF switch performance. Trap-rich SOI and HRSOI (with high PSC) will be compared for several BOX thicknesses. Small-signal simulations using the finite element simulation tool Atlas from Silvaco [17] enable us to generate and compare electrical device parameters, such as C_{off}, taking into account PSC, traps, body effects and transistor dimensions. Fig. 7 shows a profile view of an SOI transistor upon which the capacitance network between the source and drain electrodes has been superposed.

In the off-state the main coupling path is through C_{chan}, which represents the depleted portion of the channel region. For the substrate's properties to influence on the total value of C_{off}, the conductance path seen in parallel with ωC_{chan} must be of the same order as (or higher than) ωC_{chan}. For SOI type substrates, the parallel conductance channel through the bulk is at most equal to $\omega C_{BOX-V}/2$. This means that if $C_{BOX-V}/2$ is significantly lower than C_{chan} then the properties of the substrate influence very little on the coupling from source to drain and on the C_{off} capacitance.

This is the hypothesis explaining why the same value of C_{off} is measured on all substrates, HR and both RFeSI, presenting different effective resistivities as well as different BOX thicknesses. To investigate this hypothesis, a single transistor of the RF switch stack is simulated using Atlas, using the same device dimensions and doping levels as the physically measured transistors of the stack. The simulations were run for varying BOX thickness on both a HR wafer including PSC induced by fixed charges in the BOX, as well as on an RFeSI trap-rich wafer, including a poly-silicon layer beneath the BOX in which a large trap density was

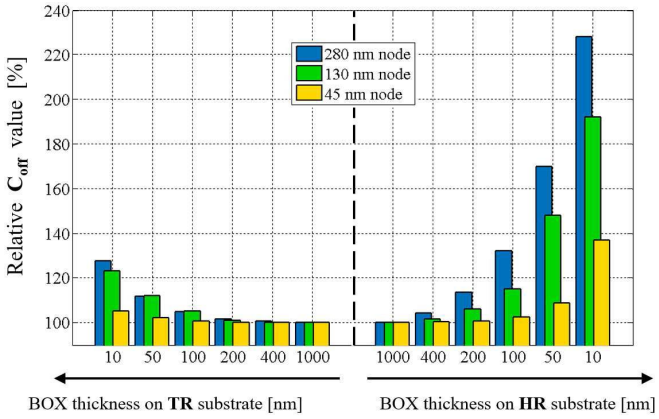

FIGURE 8. Impact of BOX thickness and substrate on the relative and normalized value of C_{off} at 900 MHz three technology nodes on HR SOI (with PSC) and TR substrates.

defined in order to effectively pin the Fermi-level near mid-gap in a highly resistive state. The results are plotted in Fig. 8 as the relative capacitance variation normalized to the capacitance value on a 1μm-thick BOX. The analysis versus BOX thickness is made on HR (right side of graph) and on TR-RFeSI (left side of graph) as the underlying substrate, for all considered BOX thicknesses from 10 nm to 1 μm and for all three technology nodes.

The results relative to the 280 nm node from TowerJazz are plotted in blue in Fig. 8. We can observe from these results that the impact of the substrate on the C_{off} coupling in our 280 nm switch device only becomes significant when the BOX thickness is below approximately 200 nm. This result can be analyzed roughly by considering that, for the substrate to play a role on C_{off}, the following inequality should be respected:

$$\frac{C_{BOX-V}}{2} \geq C_{chan} \cdot 10\% \tag{1}$$

This inequality is verified if the AC coupling current running through the bulk is ≥ 10% of that running through the off channel region. When this inequality is verified, C_{off} contains a non-negligible contribution of the substrate's electrical properties. By writing out the expressions of C_{BOX-V} and C_{chan} as parallel plate capacitors, and by assuming $\varepsilon_{Si}/\varepsilon_{ox} \approx 3$, the above inequality reduces to:

$$t_{BOX} \leq \frac{5}{3} \cdot \frac{2 \cdot L_{depchan} \cdot L_{SD}}{t_{chan}} = \frac{5}{3} \cdot \frac{2 \cdot 35 \cdot 250}{145} \approx 201 \text{ nm} \tag{2}$$

where t_{BOX} is the BOX layer thickness, t_{chan} is the active silicon channel thickness (145 nm), L_{SD} is the length of the source and drain regions (250 nm), and $L_{depchan}$ is the length of each depletion region separating the channel from the source or drain. $L_{depchan}$ is not equal to the entire length of the device's channel, as in off-state, a gate voltage of −2.5 V biases the channel region in accumulation. Fig. 7b shows the carrier concentration distribution in our device with $V_G = -2.5$ V and $V_D = V_S = V_{body} = 0$ V. Two depletion regions are shown that isolate the p-type body region, biased in accumulation, from the n-type source and drain regions. These depletion regions are depicted in a turquoise color that represents low carrier concentrations. $L_{depchan}$ depends mainly on the doping levels of the source/drain regions and of the channel itself, and for the technology under consideration should be in the 25-75 nm range. In the simulation results shown in the Fig. 7b the depletion regions were 35 nm wide. Then, for this value, Eq. (2) tells us that very little substrate effect is expected to impact C_{off} while the BOX is thicker than approximately 200 nm, which is in agreement with the simulation results of Fig. 8, which shows that a significant substrate impact on C_{off} only occurs when the BOX thickness drops below a few hundred nanometers. Furthermore, this critical BOX thickness is expected to reduce at more advanced nodes (i.e., at shorter gate lengths). And so, because the three considered substrates have thicker BOXes (200 nm, 400 nm and 1 μm) than the depletion regions of the off-state device (< 100 nm), the measured C_{off} values on all substrates are identical as the fields do not penetrate deeply enough through the BOX into the substrates. It is for this reason that the extracted C_{off} values on HR with 1 μm BOX was the same as on both RFeSI substrates (see Fig. 2b).

The green and orange data of Fig. 8 present the same study at lower technology nodes, i.e., shorter gate length and source/drain lengths, as well as a thinner active channel region. For the 130 nm node the source/drain lengths were considered to be 100 nm, and the active layer was considered to be 90 nm-thick. According to Eq. (2) the critical BOX thickness at which the substrate impacts on the performance of C_{off} is approximately 130 nm. This result is consistent with the simulated green data of Fig. 8. The results for the 45 nm are shown as the orange data of Fig. 8. At this node the source/drain lengths were considered to be 45 nm, and the active layer was considered to be 60 nm-thick. Eq. (2) then gives the critical BOX thickness as approximately 55 nm, which is consistent with the simulation data. Fig. 8 demonstrates that shorter node devices become less sensitive to substrate effects as the fields concentrate in the BOX, which is usually of much thicker dimensions.

Atlas simulations also enabled us to verify the impact of body bias on the electrical characteristics of the SOI devices. Simulations showed that applying a negative bias to the transistor body had the effect of increasing the depletion widths $L_{depchan}$. This potential adds itself to the built-in potential across the PN junction, increasing the depletion width and lowering C_{off}. The opposite is true for positive values of the applied body bias, that tend to oppose the built-in potential of the PN junctions and reduce the depletion widths, therefore increasing the overall value of C_{off}, as was shown in the measurements of Fig. 5.

VI. CONCLUSION

In this paper, the relative contribution of active devices and substrate to the RF switch performance in terms of

small- and large signal parameters is presented. The use of RFeSI substrates significantly reduces the 2nd harmonic level in on-state. The harmonic levels in off-state mainly originate from the non-linear behavior of the active devices. However, in trap-rich technology, the level of non-linearity originating from active devices, and therefore the total system non-linearity can be reduced further by carefully controlling the body bias voltage. It is shown that RFeSI having a 2.5 or 5 times thinner BOX still outperforms HR substrate, and that a thinner BOX does not impact on the overall performances of SOI switches in terms of C_{off}, especially those implemented in advanced technology nodes. It is worth mentioning that in SOI technology, BOX thinning is desired to achieve better thermal properties (lower self-heating effect) or back-gate control scheme in the transistors while maintaining low substrate cross-talk and losses.

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