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Analysis and Validation of Low-Frequency Noise Reduction in MOSFET Circuits Using Variable Duty Cycle Switched Biasing

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ABSTRACT In MOS transistors, low-frequency noise phenomena such as random telegraph signal (RTS), burst, and flicker or $1/f$ noise are usually attributed to the random nature of the trap state of defects present at the gate Si-SiO_2 interface. In a previous work, theoretical modeling and analysis of the RTS and $1/f$ noise in MOS transistor was presented and it was shown that this $1/f$ noise power can be reduced by decreasing the duty cycle (D) of switched biasing signal. In this paper, an extended analysis of this $1/f$ noise reduction model is presented and it is shown that the RTS noise reduction is accompanied with shift in the corner frequency (f_c) of the $1/f$ noise and the value of shift is a function of continuous ON time (T_{on}) of the device. This $1/f$ noise reduction is also experimentally demonstrated in this paper using a circuit configuration with multiple identical transistor stages which produce a continuous output instead of a discrete signal. The circuit is implemented in 180 nm standard CMOS technology, from UMC. According to the measurement results, the proposed technique reduces the $1/f$ noise power by approximately 5.9 dB at switching frequency (f_s) of 1 KHz for 2 stage, which is extended up to 16 dB at f_s of 5 MHz for six stage configuration.

INDEX TERMS Low-frequency noise, RTS noise, $1/f$ noise, stochastic process, CMOS image sensors, random process, cyclostationary process, autocorrelation, CMOS.

I. INTRODUCTION

The $1/f$ noise is a dominant noise source in the low-frequency region and is one of the major bottlenecks in applications like CMOS image sensors. The high noise limits the dynamic range of an image sensor. The primary sources of noise affecting the performance of a CMOS imager are the thermal noise from the switches and the low-frequency $1/f$ noise from the in-pixel buffer. The thermal noise can be efficiently reduced using correlated double sampling (CDS) and an image sensor with $0.7e^-$ noise has been reported [1]. The major limiting factor for the dynamic range now is the $1/f$ noise from the source follower (SF) which is used as a buffer in the active pixel sensor (APS), to isolate photo-diode (PD) node from the readout circuit. The low-frequency noise has an inverse relationship with frequency and aspect ratio of the device [2], which becomes more prominent as small size transistors are needed to increase the spatial resolution of an image sensor.

There are a few models available which define the $1/f$ noise conditionally but no model exists that can explain the $1/f$ noise phenomena completely [3]–[15]. Hooge's $\Delta\mu$ model [14] considers that the $1/f$ noise is caused by fluctuation in carrier mobility inside the bulk of MOS device. Carrier density fluctuation (ΔN) model by McWhorter [15] is based on the variation in the number of charge carriers inside the channel due to random behavior of the trap states present at the interface. This model states that the $1/f$ noise is a resultant of the RTS noise components from each trap. These traps are bias voltage dependent and have widely distributed emission/capture rates [16], [17]. Due to time-varying biasing conditions, the non-stationarity is introduced in the behavior of the trap state, which makes the RTS noise and consequently the $1/f$ noise non-stationary.

The $1/f$ noise in MOS transistor can be reduced by rapidly switching the device between accumulation and strong inversion region, which is introduced first time in [18] and further investigated by many researchers. To model the noise for systems with time-varying biasing conditions, a proper stochastic model for trap state is required [18]–[26]. Tian *et al.* [27], [28] and Mahmutoglu and Demir [29], [30] modeled the random activity of a single trap as a stochastic process and presented the non-stationary RTS noise model for switched biasing using autocorrelation analysis of trap states in the time domain. The model in [27]–[30], predicted that the noise reduction is independent of switching frequency ($f_s = 1/T$, where T is the time period of the switched biasing signal) and concluded that the corner frequency (f_c) of the $1/f$ noise is independent of time-varying emission/capture rates. In these and other papers on the low-frequency noise reduction [18]–[21], [23], [27]–[34] the transistors are switched with either 50% or 25% duty cycle rectangular waveform and without multiple stages thereby leading to a discontinuous output for the circuits like buffers/amplifiers.

In [35], we have proposed to use variable duty cycle switched bias signal with multiple stages of transistors for continuous output and have shown that such configuration can lead to $1/f$ noise reduction. The $1/f$ noise is modeled for a complete range of duty cycle (0 to 100%) of the switched biasing signal and its effect on the overall noise is studied. Decreasing the duty cycle reduces the overall low-frequency noise by reducing the time for which the trap states are correlated. It is additionally shown that if multiple transistors are used with the same duty cycle (so as to ensure a continuous output), the total noise would still be less than what is obtained by using a single transistor which is ON all the time. Thus, if n transistors are ON for time T/n (only one transistor is ON at any given time so as to ensure a continuous output), the total noise keeps decreasing as n increases. This was shown using a mathematical model in our previous paper [35]. In this paper, an extended analysis of this $1/f$ noise model is presented and conclusions are verified with experimental results. A source follower implementation using multiple transistors, is presented to verify the noise reduction while maintaining a continuous time output.

The paper is organized as follows: The proposed mathematical model [35] for the RTS and $1/f$ noise power spectral density (PSD), and the $1/f$ noise reduction method using multiple transistors with variable duty cycle switched biasing is briefly presented in Section II. In Section III a circuit level implementation of the multistage SF with variable duty cycle switched biasing is presented for CMOS imager with standard 3T or 4T active pixel sensors. The experimental measurement results are presented in Section IV. The paper is concluded in Section V.

II. RTS AND 1/*F* NOISE MODELING AND ANALYSIS WITH REDUCTION TECHNIQUE

As described in our previous work [35], the RTS noise modeled in a time-varying biasing condition for a more general case, where the duty cycle of switched bias signal varies between 0 and 100 %. As the variable biasing condition is periodic, the electron capture statistics of a single trap can be modeled by considering its behavior as a cyclo-stationary stochastic process [36]–[38]. The capture and emission processes are random and governed by Poisson statistics. This Poisson process is inhomogeneous and exhibits non-stationarity, due to the dependency of capture rate (λ_c) and emission rate (λ_e) on voltage-dependent variables like mean time before emission (τ_e) and mean time before capture (τ_c). Similar to other proposed models [16], [20], [27], [30], [41], the RTS noise modeling presented in this work considers the ideal trap model. The model is based on the assumption that for switched biasing, $\lambda_e = \lambda_c = \lambda_{on}$ for ON state and $\lambda_e = \lambda_{off}$, $\lambda_c \approx 0$ for OFF state of the device. As shown in [35] the trap state autocorrelation is almost zero during the OFF state of the device. Switching the transistor OFF between consecutive ON time period, for sufficient time ($>> \lambda_{off}^{-1}$), resets the probability of trap occupancy (PTO) to zero. During OFF state of the device the value of the probability of trap occupancy (if $\lambda_{off} T_{off} >> 1$) is close to zero (during OFF state of the device) due to very high emission rate and negligibly small capture rate in the absence of conduction [16], [20], [31], [39]–[41].

If the periodic ON time (T_{on}) is less than $1/\lambda_{on}$, then the trap state are reset in every time interval $T_{rst} = T_{on} + \lambda_{off}^{-1} \approx T_{on}$ (for $\lambda_{off}^{-1} << T_{on}$). Thus, the trap states separated by $T_{rst} \approx T_{on}$ time interval or more, have zero correlation. As ideal trap model is considered in this work, the real factor for this zero correlation is in the condition of $\lambda_{off} T_{off} >> 1$. That is, every trap state becomes zero when the transistor is switched OFF.

Considering the trap state $N(t)$ as a cyclo-stationary random process [42], the double sided RTS noise PSD of a single trap, for ON state of the device, is calculated as:

$$S_{\lambda,on}(\omega) = \frac{1/4T}{\left(4\lambda_{on}^2 + \omega^2\right)} \left[\frac{4T\lambda_{on}}{n} - A - \frac{Be^{\frac{-2\lambda_{on}T}{n}}}{4\lambda_{on}^2 + \omega^2} \right], \quad (1)$$

$$A = a^2 4e^{\frac{-4\lambda_{on}T}{n}} + \frac{\left(16a^2 + 8\right)\lambda_{on}^2 + a^2 4\omega^2 - 2\omega^2}{\left(4\lambda_{on}^2 + \omega^2\right)},$$

$$B = \left(40a^2 + 6\right)\lambda_{on}^2 cos\left(\frac{\omega T}{n}\right) - 8\omega\lambda_{on} sin\left(\frac{\omega T}{n}\right),$$

where 'a' is a constant which is dependent on the PTO at initial condition ($t = 0$) of the ON state, ω is angular frequency, and n is used to define continuous ON time $T_{on} = T/n$ and later part of the paper n is again used to define number of stages.

In this work, a variable duty cycle is used for biasing signal in which OFF time is higher. As OFF time increases

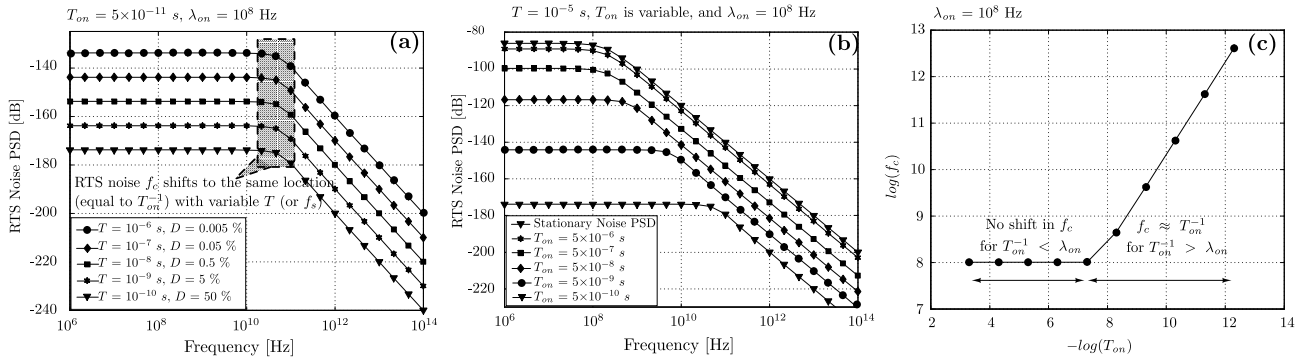

FIGURE 1. **The switched bias random telegraph signal (RTS) noise power spectral density (PSD) for single transistor, calculated from derived model given in Eq. (1) using MATLAB tool, with variable duty cycle (D) to demonstrate that (a) The RTS noise corner frequency (f_c) of a trap under switched biasing, shifts to a new value and the new location of f_c is $\approx T_{on}^{-1}$. For all graphs T_{on} ($= T \times D/100 = 5 \times 10^{-11}$ s and $T_{on}^{-1} > \lambda_{on}$) is kept same however, switching frequency (f_c) or time period (T) of switched biasing signal are variable. This shows the dependency of corner frequency shift only on T_{on}. The downwards shift in the flat potion of the RTS noise PSD is only due to the higher OFF time. (b) The trap RTS noise f_c shifts at different locations ($\approx T_{on}^{-1}$ with the condition of $T_{on}^{-1} > \lambda_{on}$)) with different values of variable T_{on} however, time period of switched biasing signal (T) or switching frequency ($f_s = 1/T$) are kept same for all graphs, and (c) Relationship between f_c and T_{on} to show that the switching action affects the corner frequency of the traps only when $T_{on}^{-1} > \lambda_{on}$.**

the probability of trap to be empty is high due to higher λ_{off} and to get filled again is very low as λ_{on} is very low [39], [40]. Thus, the noise in OFF state of the device can be neglected and the RTS noise PSD can be given as:

$$S_{\lambda}^{s}(\omega) \approx S_{\lambda,on}(\omega). \tag{2}$$

The $1/f$ noise is calculated by superposition of the noise generated by individual traps with different capture/emission rates. The overall $1/f$ noise PSD is given by [16]:

$$S(\omega) = \int_{\lambda_L}^{\lambda_H} S_{\lambda}^{s}(\omega)\, g(\lambda)\, d\lambda, \quad g(\lambda) = \frac{4k\theta A t_{ox} N_t}{\lambda \log\left(\frac{\lambda_H}{\lambda_L}\right)}, \tag{3}$$

where $g(\lambda)$ is the distribution function of the emission and capture rate. θ is the absolute temperature in Kelvin, k is Boltzmann constant, A is the channel area ($1\ \mu m^2$), t_{ox} is the effective gate oxide thickness ($10\ nm$), N_t is the trap density, λ_H and λ_L are the fastest and slowest transition rates, respectively. These rates are related to t_{ox} through the equation $\log(\lambda_H/\lambda_L) = \gamma t_{ox}$, where γ is the tunneling constant.

The $1/f$ noise voltage PSD [27] is given by:

$$S_{1/f}(\omega) = \left(\frac{q}{AC_{ox}}\right)^2 S(\omega), \tag{4}$$

where C_{ox} is the unit area channel capacitance and q is electron charge.

The derived model is also validated as higher RTS noise reduction can be obtained with an increase in the values of 'n', as per Eq. (1). Multiple transistors are connected between the input and the output wherein the noise contribution of each transistor is assumed to be non-correlated. Thus overall $1/f$ noise PSDs would be the summation of the noise PSDs of each source follower and is given as:

$$S_{\lambda}^{o/p}(\omega) = n \times S_{1/f}(\omega), \tag{5}$$

where $S_{1/f}(\omega)$ is the worst case noise PSD of each stage.

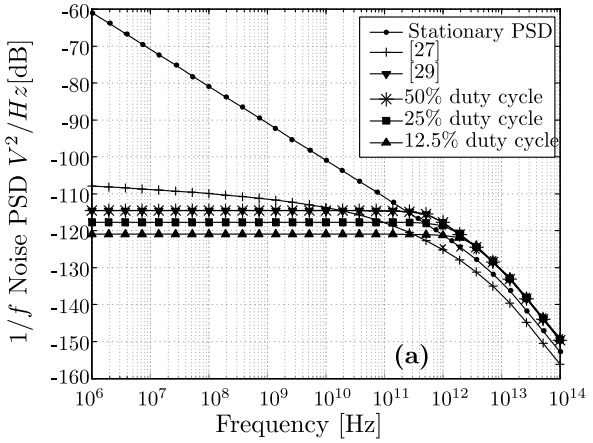

FIGURE 2. **Comparison of total $1/f$ noise PSD ($n \times S_{1/f}(\omega)$) at the output, given by Eq. (5), calculated using MATLAB tool, between the existing noise models and this work with variable duty cycle (D) and multiple ('n' number of) stages [35].**

Equation (1) is evaluated using MATLAB tool to demonstrate reduction in the RST noise. It is evident from the evaluated results, shown in Fig. 1(a), that RTS noise corner frequency (f_c) of a trap under switched biasing, shifts to a new value and the new location of f_c is $\approx T_{on}^{-1}$. For all graphs T_{on} ($= T \times D/100 = 5 \times 10^{-11}$ s and $T_{on}^{-1} > \lambda_{on}$) is kept same however, switching frequency (f_c) or time period (T) of switched biasing signal are variable. This shows the dependency of corner frequency shift only on T_{on}. The downwards shift in the flat potion of the RTS noise PSD is only due to the higher OFF time. For calculations the value of λ_{on} has been chosen as 10^8 Hz. The RTS noise is plotted for T varying from 10^{-6} s to 10^{-10} s and for each value of T, T_{on} is kept equal to 5×10^{-11} s by adjusting the value of n. The downwards shift in the flat potion of the RTS noise PSD in Fig. 1(a) is only due to the higher

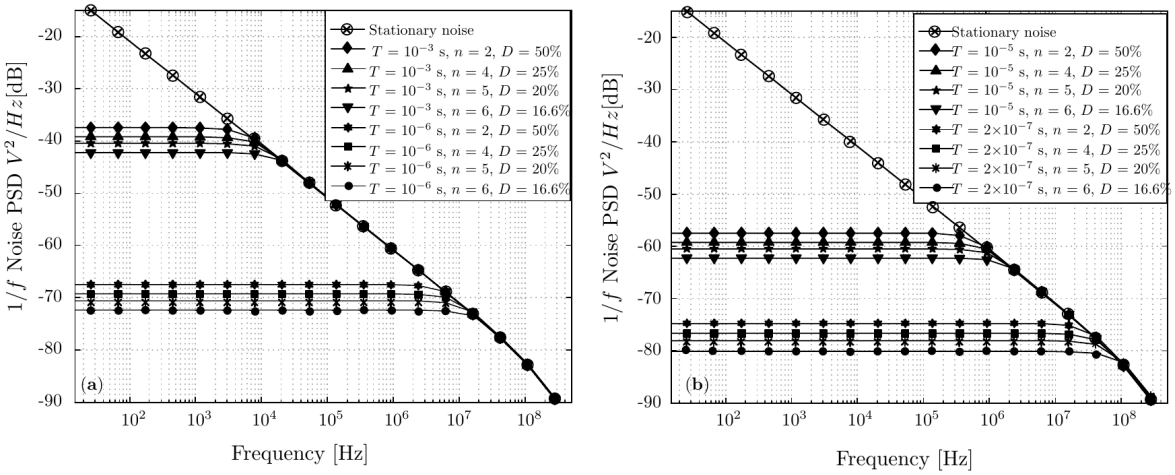

FIGURE 3. **(a) The $1/f$ noise PSD [$n \times S_{1/f}(\omega)$] at the output, calculated from Eq. (5) using MATLAB tool, for switched biasing with a variable duty cycle (D) and multiple ('n' number of) stages with (a) $T = 10^{-3}$ s and $T = 10^{-6}$ s, (b) $T = 10^{-5}$ s and $T = 2 \times 10^{-7}$ s.**

OFF time. From the results, it can be observed that for each case the f_c is shifted to approximately T_{on}^{-1}, which shows the dependency of corner frequency shift only on T_{on}. This explains the RTS noise reduction only depends on T_{on} and does not get affected from variable switching frequency.

In Fig. 1(b), the RTS noise evaluated from Eq. (1) is plotted for varying values of T_{on} from 5×10^{-7} s to 5×10^{-10} s while keeping $T = 10^{-5}$ s. As can be seen in this graph, for the noise plots with $T_{on}^{-1} < \lambda_{on}$, the corner frequency doesn't shift and remains approximately equal to λ_{on} (10^8 Hz). For these plots the noise power reduces by 'n' time as compared to stationary noise, which is only due to higher OFF time of the device. Hence, there is no reduction in the RTS noise. While for the plots with $T_{on}^{-1} > \lambda_{on}$ the corner frequency (f_c) shifts to T_{on}^{-1} and the reduction in noise is n times as compared to stationary noise. A higher shift in the f_c accompanies a higher reduction in the low-frequency noise. It can be concluded from the results that the noise reduction depends on the T_{on} rather than T or f_s. Thus, the same reduction can be achieved by switching the transistor at a comparatively lower frequency by decreasing the duty cycle of switching signal. The relation between T_{on}^{-1} and f_c is plotted in Fig. 1(c). It can be seen that f_c stays at λ_{on} (= 10^8 Hz), for all values of T_{on}^{-1} less than λ_{on}, while shifts to approx. T_{on}^{-1} for all values of $T_{on}^{-1} > \lambda_{on}$.

In Fig. 2, the $1/f$ noise PSD evaluated from Eq. (5) with the multiple stages is compared with the 1/f noise PSD from the standard model (stationary noise model), and other models reported in [27] and [29]. Higher $1/f$ noise reduction is obtained, as shown in Fig. 2, as compared to other models while the output is still continuous in nature. The $1/f$ noise evaluated from Eq. (5) is shown in Fig. 3 for varying time period from 1 KHz to 5 MHz and the number of transistor stages from 2 to 6. The stationary noise has also been plotted in Fig. 3 for comparison. As T_{on} decreases with increase in the number of stages and f_s, it can be concluded that $1/f$ noise reduction depends on the T_{on} and independent of f_s when T_{on} is kept constant.

From the above analysis, it can be stated that the noise reduction increases with a decrease in value of T_{on} or duty cycle of the switched biasing signal and following conclusions can be derived.

- Decrease in the $1/f$ noise power for sampling frequencies above T_{on}^{-1} is due to the increasing correlation between trap states. Here, the term sampling frequency (in Hz) denotes the number of samples of the noise power spectral density (in dB) per second. Due to switching action, the correlation between the samples, separated by more than T_{on} time, becomes very weak. This makes the noise PSD "flat" for the sampling frequencies T_{on}^{-1}. Hence, The corner frequency is shifted to a new value of T_{on}^{-1} for $T_{on} < \lambda_{on}^{-1}$, which causes reduction in the noise power.
- For the trap states of a single transistor sampled during ON time and separated by time interval less than T_{on}, have the same correlation as DC biasing condition. Hence, the noise power for sampling frequencies above the T_{on}^{-1} is 10log(n) dB less than the noise power of the stationary noise PSD (reduction of 10log(n) dB in the noise power is due to OFF state of the device).
- A higher noise reduction can be achieved by lowering the value of T_{on} either by increasing f_s or decreasing duty cycle, as compared to the model presented in [27], [29], and [37]. If T_{on} is kept constant by suitably varying the duty cycle, the obtained noise reduction is also constant for varying f_s.
- The noise reduction is observed only for frequencies below the corner frequency. Above the corner frequency, the noise remains 10log(n) dB less than the stationary noise due to OFF state.
- Device ON and OFF time may not be equal, as the OFF time of the device (T_{off}) increases as duty cycle decreases. The PTO before commencement of ON time

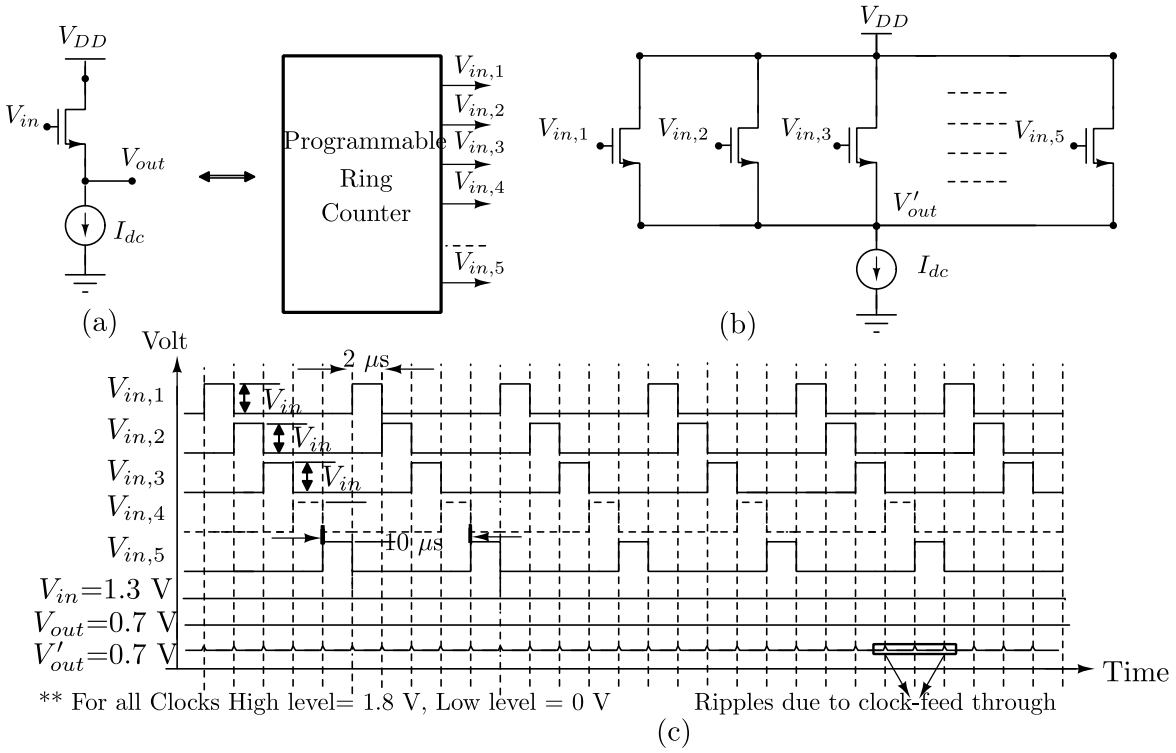

FIGURE 4. **(a) Single transistor source follower (SF), (b) SF action achieved through multiple (5 transistors in this example) transistors with programmable ring counter which produces periodic output signals ($V_{in,1}$, $V_{in,2}$, $V_{in,3}$ ... and $V_{in,n}$) with amplitude of V_{in} = 1.3V equal to the amplitude of the continuous time input of the single stage source follower (V_{in}), and (c) Timing diagram, generated from Cadence Spectre Simulator, for single transistor SF and 5 stage SF action with f_s = 100 KHz, D = 20 % and T_{on} = 2μs.**

becomes negligibly small ($P_{on}(0) \approx 0$), where $P_{on}(0)$ is the initial value of PTO function for ON time of the device. As λ_{off} is very high the PTO at time equal to $T(n-1)/n$ during OFF state, is negligibly small (considered as zero). Thus, OFF time PSD can be considered as negligible. Other assumptions taken to derive the noise PSD are $\lambda_{on}T_{on} << 1$ and $\lambda_{off}T_{off} >> 1$ as in [39] and [40].

III. DETAILED CIRCUIT IMPLEMENTATION

Based on the above analysis, a circuit level noise reduction technique is proposed for the source follower transistor in standard CMOS image sensors. The source follower, shown in Fig. 4(a) is used to show the reduction of $1/f$ noise reduction in an active pixel sensor (APS). A conventional APS employs three or more transistors where all transistors, except the SF, act like a switch. The switches mostly contribute to the thermal noise, while the SF contributes to the low-frequency noise. The SF low-frequency noise is becoming more evident as transistor sizes are becoming smaller with technology scaling. Thus, the $1/f$ noise, as a dominant source of the noise at the imager output must be reduced to improve the overall signal-to-noise ratio [1], [20], [41], [43], [44].

The switching activity makes the output discrete in nature, which is not suitable for image sensor applications. Complementary switches are used to obtain a continuous output in [45]. The two MOSFET switches are periodically switched between strong inversion and cut-off regions which lead to a reduction in the low-frequency noise. The circuit in [9] is limited to two switches, which is extended to multiple transistors configuration (in this work), with higher noise reduction.

To achieve the action of single stage buffer/amplifier shown in Fig. 4(a) with reduced low-frequency noise, circuit shown in Fig. 4(b) is implemented with multiple and identical SF stages. Individual source followers, among the multiple paths, are selected periodically for a small interval of time as shown in Fig. 4(c). Thus, among multiple paths, only one path from input to the output is ON at a given time. Since one path is always ON between the input and the output, the output remains continuous. If each transistor is ON for $T_{on} = T/n$ time in a time period T, to achieve a continuous output, 'n' number of stages would be required such that one stage is ON at a time. Thus, in this paper 'n' is number of stages and used for $T_{on} = T/n$, duty cycle $(D) = 100 \times T/n\%$.

The single transistor source follower in Fig. 4(a) has $V_{in} = 1.3V$ as continuous input signal. For switched biasing, a programmable ring counter is used which produces non-overlapped output waveforms ($V_{in,1}$, $V_{in,2}$, $V_{in,3}$ ... and $V_{in,n}$) where each output amplitude is set to V_{in} (= 1.3 V), as shown

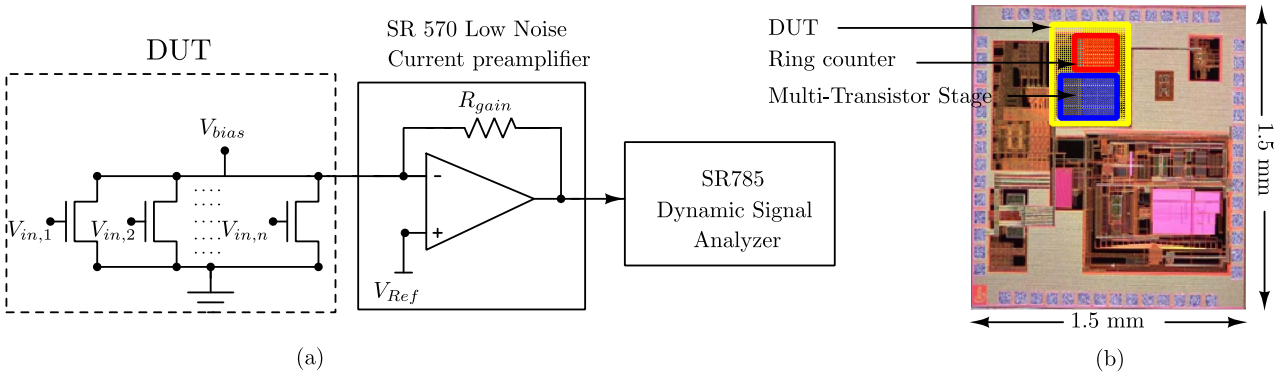

FIGURE 5. **[Color online] (a) Measurement setup for design under test (DUT) (b) Chip microphotograph.**

in Fig. 4(b) and (c). These outputs of programmable ring counter act as inputs to the multistage source follower. Each output has amplitude equal to $V_{in} = 1.3V$ as high level (to turn the transistor ON) and 0 V as low level (to turn the transistor OFF). This way only one transistor, at a time, is getting voltage equal to V_{in} at its gate terminal, while rest other are getting 0 V and remain at OFF state. This makes each transistor is ON only for a small time period which is controlled by ring counter. As one of the transistors is always ON, the output is always available and which is same as the output of single source follower transistor. This way every transistor is switching ON and OFF periodically while output remains continuous and thus, this structure functions as buffer. The frequency of the counter can be controlled by an external clock, thus, allowing for varying the duty cycle of each transistor, externally. As only one transistor is ON at a time in the input to the output path, the noise generated from each stage is non-correlated. Thus, the overall noise at the output is equal to the addition of the noise power of each stage transistor. This non-correlated noise sampling is one of the major keys behind the total noise reduction. All transistors in the programmable ring counter work as a switch, adding only thermal or white noise to the output. The ring counter does not contribute $1/f$ noise and thus, overall low-frequency noise remains unaffected.

IV. MEASUREMENT RESULTS

To validate the proposed method, the low-frequency noise measurements have been carried out on circuit implemented in 180 nm standard CMOS technology, from UMC. The measurement setup is shown in Fig. 5(a) while the microphotograph of the test circuit, fabricated in 0.18 μm standard 1P6M CMOS process, is shown in Fig. 5(b). The DUT has employed an array of nMOS transistors and a configurable ring counter to generate periodic switched biasing signals for turning the MOS transistors ON and OFF, periodically. The devices used in test circuit are nMOS transistors with $W = 1\ \mu m$ and $L = 1\ \mu m$. The target application of the proposed method is to reduce the $1/f$ noise in CMOS image sensors. The device dimensions for noise characterization are chosen to be small to maximize the fill factor of a pixel and maintain the smaller area of the pixel for higher spatial resolution.

The measurement setup is similar to that reported in [46] and [47]. The low noise SR570 current preamplifier is used to provide the biasing current to the test circuit and to amplify the noise power. As shown in Fig. 5(a) the drain to source voltage V_{DS} (or V_{bias}) of test transistors, is equal to V_{ref} of the preamplifier. The value of V_{DS} can thus be set to a desired value by varying V_{ref} to keep transistors in saturation region during ON state. The noise current generated from the test circuit is amplified by the load resistance R_{gain}, to produce the noise voltage at the output of the preamplifier. The noise power at the output node of the circuit shown in Fig. 5 (a) can be calculated by MOSFET noise current ($I_{DS,n}$) and the load resistance (R_{gain}, which is a feed-back resistance present in the SR570 current to voltage preamplifier). The current to voltage sensitivity of the preamplifier was set at 10 $\mu A/V$ to get amplified noise voltage at the output. The input referred noise of current preamplifier is as low as 5 fA/$\sqrt{Hz}$, which makes it quite suitable for precise noise measurement. The load resistance only contributes thermal noise, thus $1/f$ noise can be analyzed by measuring $I_{DS,n}$ at low-frequencies. $I_{DS,n}$ flows into R_{gain} and is amplified by the preamplifier, the amplified noise voltage is analyzed using Dynamic Signal Analyzer (DSA - SR785). The DSA plots the Fourier transform of the noise voltage signal from the preamplifier. The reduction in the noise current of DUT, is shown in Fig. 5 (a). The input noise of the SR785 inputs is about 10 $nV_{rms}/\sqrt{Hz}$. The input noise of the analog to digital (A/D) converter in SR785 is about 300 $nV_{rms}/\sqrt{Hz}$ (referenced to a full scale of 1 V_{pk}) and the bandwidth is 102.4 KHz.

In the SR785 the input signal passes through an analog anti-aliasing filter that removes all frequency components above 102.4 kHz and then the incoming data samples are digitally filtered and down-sampled to increase the resolution. The noise PSD is plotted with 400 line fast Fourier transform (FFT) resolution and 400 Hz span to set 1 Hz frequency resolution. As the maximum frequency was 400 Hz,

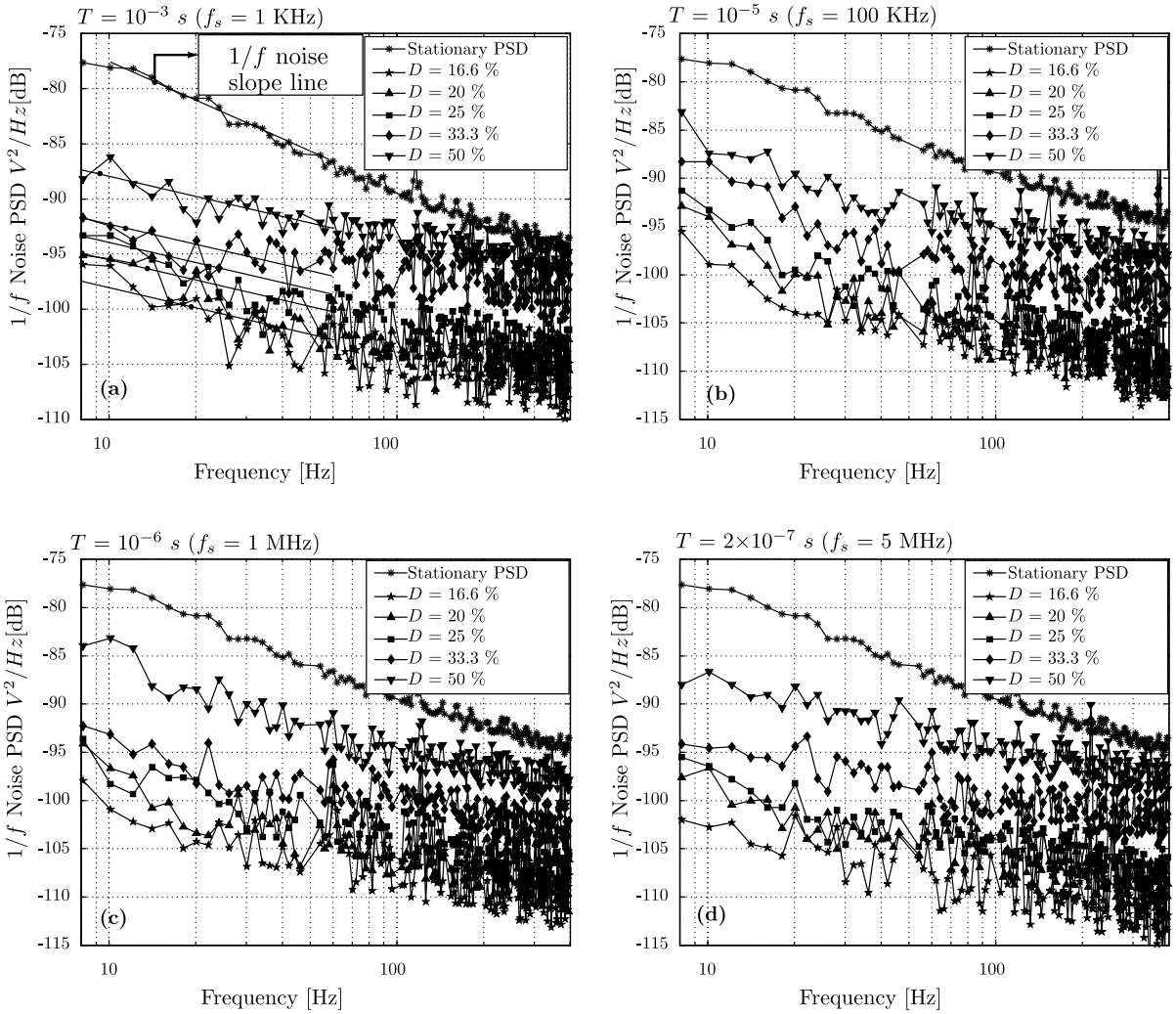

FIGURE 6. Measurement results for the switched bias $1/f$ Noise PSD for single stage configuration with a variable duty cycle (D) or continuous ON time (T_{on}) with (a) $T = 10^{-3}$ s , (a) $T = 10^{-5}$ s, (a) $T = 10^{-6}$ s, and (d) $T = 2 \times 10^{-7}$ s.

the sampling rate is 1024 samples/sec with 1024 number of points in a time record. In the measurement cutoff frequency of the digital low-pass filter contained is set as 512 Hz with flat response upto 400 Hz and roll-off from 400 Hz to 512 Hz. To improve the measurement accuracy, each noise PSD curve is plotted after taking an RMS average of 100 measured samples.

The DUT has a configurable ring counter which generates non-overlapping signals ($V_{in,1}$, $V_{in,2}$, $V_{in,3}$ . . . , and $V_{in,n}$) to select one MOS transistor at a time, as described in Section III. Non-overlapping clocks make sure that the noise components from different stages are non-correlated. The noise measurements for DC biasing are carried out with $V_{DS} = V_{GS} = 1$ V for nMOS transistors. For switched biasing, $V_{DS} = V_{GS}$ is set to 1 V during ON time to keep transistors in the saturation region while $V_{GS} = 0$ V for OFF time to keep the transistor in cutoff region. First, the noise measurements are carried out on a single transistor with constant biasing. Then measurement are carried out for single as well as multiple transistors, with switched biasing and a variable duty cycle (D).

The measured noise power of a single stage transistor with constant and switched biasing is shown in Fig. 6. The noise plots, shown in Fig. 6(a), (b), (c), and (d) demonstrates the reduction in the low-frequency noise power of single transistor, switched bias at $f_s = 1$ KHz, 100 KHz, 1 MHz, and 5 MHz respectively. For each f_s, the duty cycle is taken as 16.6 %, 20 %, 25 %, and 50 %. The average reduction in $1/f$ noise power for single stage configuration with varying duty cycle, (for sampling frequency up to 40 Hz and $f_s = 1$ kHz) evaluated from Eq. (3), using MATLAB simulation, is 29.57 dB, when the duty cycle varies from 100 % (DC biasing) to 50 %. After which when the duty cycle reduces to 25 %, 20 % and 16.6 % the average noise reduction increases to 35.5 dB, 37.6 dB, and 39.11 dB, respectively. While the measurement results (Fig. 6) shows an average reduction obtained in $1/f$ noise, for $f_s = 1$ KHz is 7.02 dB when the duty cycle varies from 100 % to

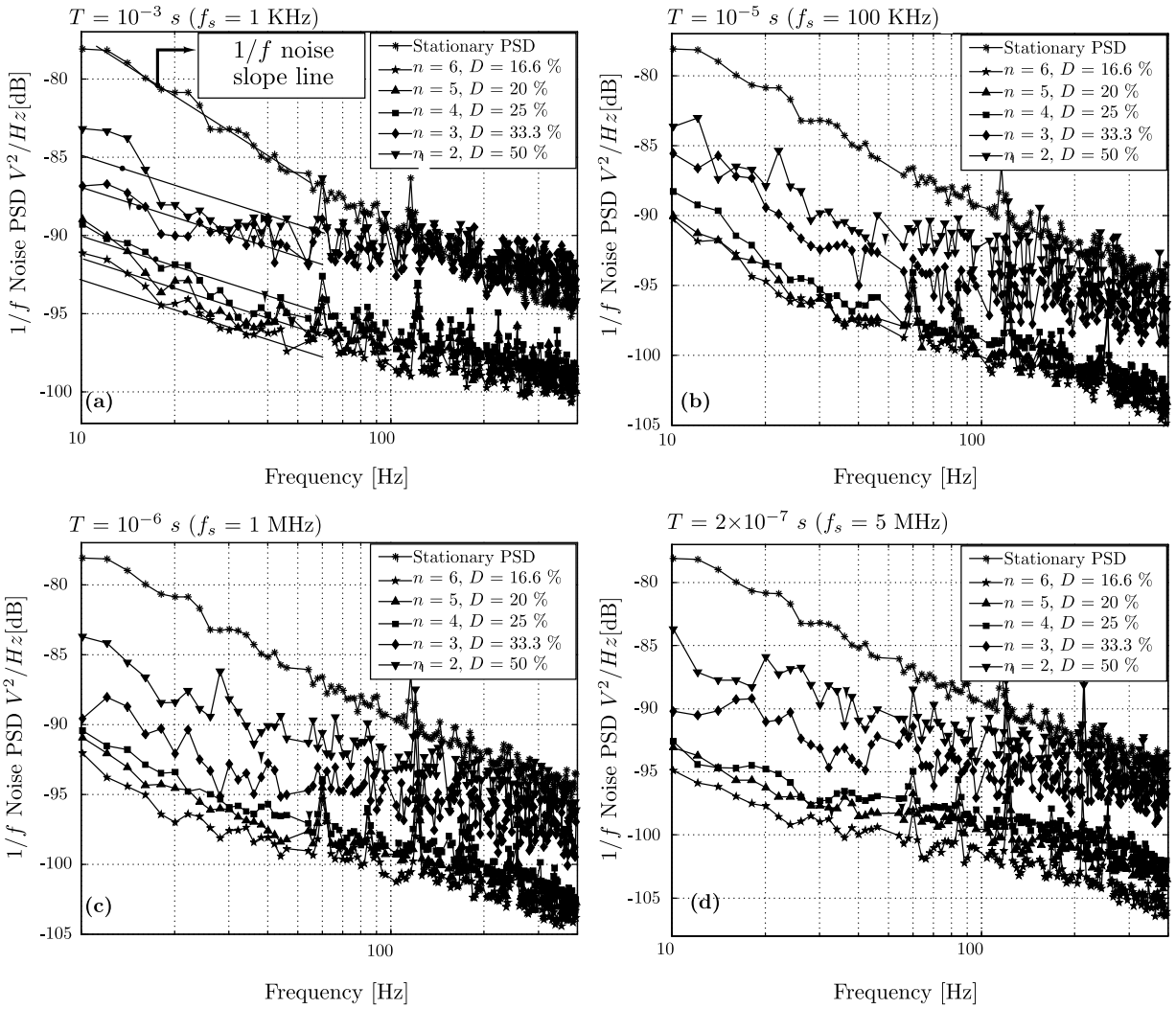

FIGURE 7. **Measurement results for the switched bias $1/f$ noise PSD for multiple ('*n*' number of) stages and a variable duty cycle (*D*) or continuous ON time (T_{ON}) with (a) $T = 10^{-3}$ *s* , (a) $T = 10^{-5}$ *s*, (a) $T = 10^{-6}$ *s*, and (d) $T = 2 \times 10^{-7}$ *s*.**

50 %. As the duty cycle further reduces to 25 %, 20 % and 16.6 %, the noise reduction increases to 15.5 dB, 17.3 dB, and 18.72 dB respectively. The sampling frequency has been chosen only up to 40 Hz, to show the low-frequency noise reduction.

The measured noise power of single stage nMOS with constant biasing and multiple nMOS transistors with switched biasing, for a varying duty cycle, is shown in Fig. 7. The output noise power for 2 to 6 stages, switched with $f_s = 1$ KHz, 100 KHz, 1 MHz, and 5 MHz are presented in Fig. 7 (a), (b), (c), and (d), respectively. For the measurements, the ring counter is configured to select 2 to 6 transistor stages, as shown in Fig. 4(b). f_s is varied from 1 KHz to 5 MHz for a variable number of stages. The duty cycle is varied from 50 % to 16.6 % for 2 to 6 transistor stages. From the measured results variation can be seen in the integrated noise reduction (for sampling frequency up to 40 Hz) from 5.9 dB, for 2 stages to 12.3 dB, for 6 stages, with $f_s = 1$ KHz. Reduction in the noise is increased with increase in a number of stages (or decrease in the duty cycle) and f_s. In both the cases, the noise reduction is increased due to the decrease in continuous ON time of the transistor, as predicted by Eq. (1).

The average reduction in the $1/f$ noise power (for sampling frequency up to 40 Hz) is summarized in Fig. 8, for $f_s = 1$ KHz, 100 KHz, 1 MHz, and 5 MHz. The $1/f$ noise power calculated by Eq. (5) (the noise PSD shown in Fig. 3) predicts the average reduction varies from 24.8 dB to 31.32 dB when the number of stages vary from 2 to 6, for $f_s = 1$ KHz. It can be concluded from results that the $1/f$ noise power depends on the continuous ON time of the device rather than f_s. For higher sampling frequencies the switched bias noise PSD is approximately equal to the stationary noise PSD, as the thermal noise start dominating above the $1/f$ noise corner frequency.

One drawback of using multiple transistors with switched biasing is that switching action of the transistors introduces ripples at the output. These ripples are generated due to clock

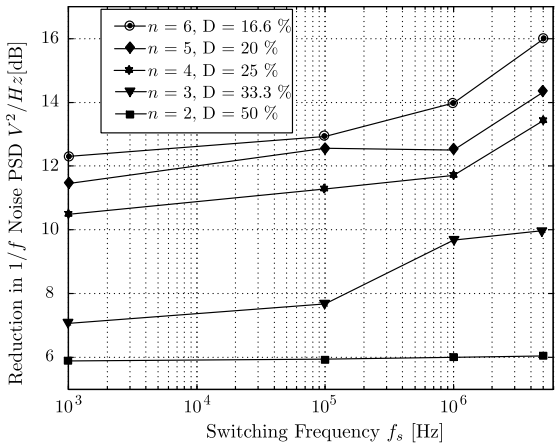

FIGURE 8. Average reduction in the measured $1/f$ noise power for sampling frequency range from 10 Hz to 40 Hz, with multiple ('*n*' number of) stages, duty cycle (*D*), and switching frequency f_s (or T^{-1}).

feed-through of the overlapping capacitance present between drain and gate of the switching transistor. The ripples can be filtered out through a switched capacitor low-pass filter. The low pass filter can be placed in the column of the CMOS image sensor, which will not affect the fill factor of the pixel. The mismatch of the source followers would increase the column fixed pattern noise (FPN). The column FPN needs to be characterized with an imaging array in place. The focus of this work is to show the noise reduction obtained using multiple stages as compared to simply duty cycling a single device. In future, an imaging array with the proposed low-frequency noise reduction method will be fabricated and the effects of multiple source followers on the column FPN and other imaging performance will be characterized.

V. DISCUSSION AND CONCLUSION

In this paper, a mathematical model of the RTS noise, for a MOSFET device with time-varying biasing conditions, is presented. It is concluded that the RTS noise and consequently the $1/f$ noise of a MOS transistor decreases with a decrease in the T_{on}. It is shown that reduction in the noise occurs due to varying correlation between trap states which is a function of T_{on} rather than switching frequency. Based on this conclusion a circuit level low-frequency noise reduction technique is presented. It is observed by measurement that the noise reduction which is 5.9 dB with $f_s = 1$ KHz for 2 stage is extended up to 16 dB for 6 stages with $f_s = 5$ MHz. The proposed technique and measurement results are shown in Fig. 6 and 7 do not indicate the suppression of mechanism of the 1/f noise generation. The present technique only exploits the properties that the switching ON and OFF (with conditional T_{on} and T_{off}) alters the correlation of the trap states of a MOS transistor and the noise components from different transistors are uncorrelated, to achieve the low-frequency noise reduction. There is no correlation between fluctuating traps in different transistors.

The nature of the low-frequency noise measurement results presented in this paper is similar to the results given in literature. There is some discrepancy in the low-frequency noise behavior between the measurement results shown in Fig. 6 and Fig. 7, and the theoretical results shown in Fig. 3. As per the theoretical results the noise PSD is flat for low-frequencies while, the measurement results show a decreasing profile. There are two possible reasons for the discrepancy between theoretical and measured results. Firstly, the autocorrelation function (ACF) calculated in the theory (Eq. (19)) and the autocorrelation obtained from the measurements are different. Secondly, there is a reappearance of $1/f$ noise in the low-frequency region.

The theoretical autocorrelation is calculated by time average value of ACF given in Eq. (19). In Fig. 9 (a) the values of time averaged ACF is plotted for a device which is ON for T_{on} time period during a time interval of T. This graph has been compared with the ACF calculated for the experimentally measured noise data with 50% and 25% duty cycles. The measurement ACF is obtained from the measured noise samples. There are mainly two important differences between these ACF plots which could be the reason for the discrepancy observed between the theoretical and measured FFT plots;

- The experimentally obtained curve is not as smooth as the theoretically obtained curve which also causes discrepancy in the nature of PSD plots.
- It can be seen that the theoretical correlation plot has non-zero values only for time samples between $-T_{on}$ to T_{on}. However, the experimentally obtained correlations are non-zero beyond this range.

The other reason for the discrepancy is the reappearance of the $1/f$ noise. This effect has been discussed in [29]–[32]. Our model is based on the assumption that $\lambda_{off} T_{off} >> 1$, as λ_{off} is very high for all traps. However, this condition need not be true for all traps, and thus all traps might not be affected uniformly in OFF condition during switching [31], [32]. The distribution of λ_{off} depends on a space dependent parameter 'm' [32]. Emission rate during off time is not uniform and can be given as:

$$\lambda_{off}(emission) = m.\lambda_{on}(emission) \tag{6}$$

The value of 'm' needs to be ∞ to ensure that the trap is empty during OFF state. However 'm' is not uniform among all traps as it depends on the location of the trap with respect to the surface of the channel [31], [32]. The value of 'm' is less for slow traps which are located away from the channel surface. If 'm' for a trap is small enough to make sure that $\lambda_{off} T_{off} << 1$, then it's state (filled or empty) does not change with switching and hence, the noise PSD from these traps represents the noise similar to the stationary case which decreases with increase in frequency. Hence, another factor is added in the expression of the noise PSD to take

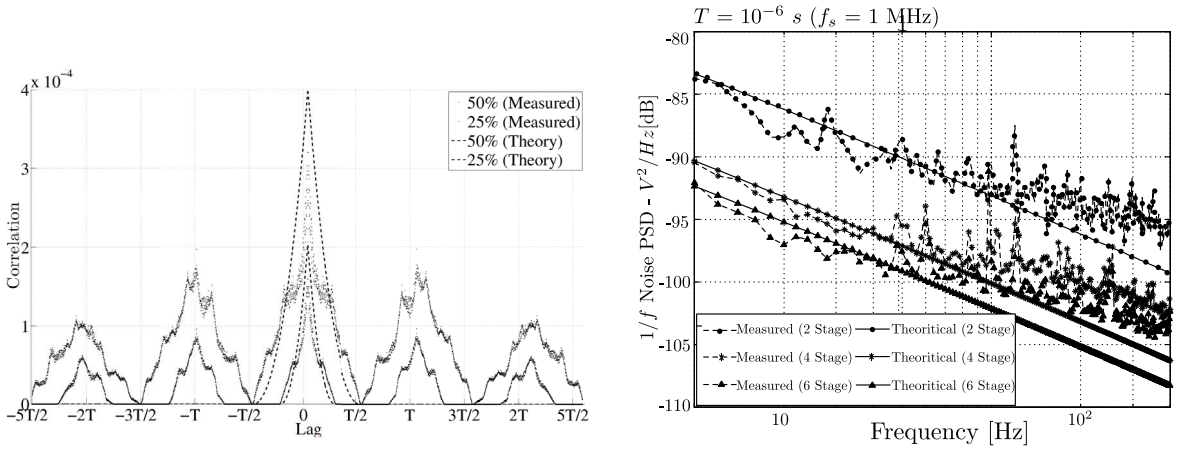

FIGURE 9. **(a) Autocorrelation function (ACF) plots for the theoretical calculated and measurement data. (b) The $1/f$ noise PSD [$S'_{1/f}(\omega)$] at the output, calculated from Eq. (7) [MATLAB simulation], for switched biasing with a variable duty cycle (D) and multiple number of stages (n).**

account of the reappearance of the $1/f$ noise. The modified $1/f$ noise can be given as:

$$S'_{1/f}(\omega) = n\int_{\lambda_L}^{\lambda_H} S^s_{\lambda,on}(\omega)g(\lambda)d\lambda + \int_{\lambda'_L}^{\lambda'_H} \frac{\gamma\lambda}{\lambda^2+\omega^2}g(\lambda)d\lambda, \tag{7}$$

where n is number of stages, λ'_L and λ'_H are the minimum and maximum transition rates, respectively among the slow traps during OFF state. γ is the fitting factor used to match the measured results with theory. The noise PSD calculated from Eq. (7), is plotted in Fig. 9 (b) and shows a similar behavior as the measured noise PSD. In first region of the curves (sampling frequency up to λ'_H), the noise decreases with increase in the sampling frequencies. In this region, the stationary noise part of Eq. (7) dominates over the switching noise PSD. In the remaining portion (sampling frequencies higher than λ'_H), the noise is from the switched noise PSD as given in Eq. (3) and first part of the Eq. (7).

In this work, a previously reported and standard measurement setup has been used, however, a possible third reason for the discrepancy between measured and theoretical results could be artifacts resulting from the measurement setup it's surrounding like internal noise (from DSA) and external noise (from near electric and magnetic field) interference.

Although, the potential reasons behind the discrepancies in the proposed noise model and measured results have been extensively discussed in this section, the exact reasoning of these inconsistencies requires more analysis. This could be the future scope of this work.

APPENDIX
TIME DOMAIN AUTOCOVARIANCE ANALYSIS TO DERIVE THE RTS NOISE PSD IN A VARIABLE DUTY CYCLE SWITCHED BIASING CONDITION

As the trap state $N(t)$, for periodic biasing conditions, is considered as a cyclo-stationary process, here time averaged ACF function, for $N(t)$, is derived for one time period. A pulsed wave with time period T with ON time of T/n, is applied to the gate of MOS transistor as the biasing signal. Let's suppose $p_{on}(t)$ is the PTO at time t during ON time of the device. As $p_{on}(t)$ is a time varying function, the probability of any event in very small time interval Δt, can be given as: As the trap state $N(t)$, for periodic biasing conditions, is considered as a cyclo-stationary process, here time averaged ACF function, for $N(t)$, is derived for one time period. A pulsed wave with time period T with ON time of T/n, is applied to the gate of MOS transistor as the biasing signal. Let's suppose $p_{on}(t)$ is the PTO at time t during ON time of the device. As $p_{on}(t)$ is a time varying function, the probability of any event in very small time interval Δt, can be given as:

$$\begin{aligned} p_{on}(t+\Delta t) &= p_{on}(t)\,.(\text{probability of zero emission event in } \Delta\text{t}) + (1-p_{on}(t))\,.(\text{probability of acapture event in } \Delta\text{t}), \\ &= p_{on}(t)\,.(1-\lambda_e\Delta t) + (1-p_{on}(t))\,\lambda_c\Delta t. \end{aligned} \tag{8}$$

As for ON state of transistor $\lambda_c \approx \lambda_e \approx \lambda_{on}$, the probability of a capture or emission event in Δt time is equal to $\lambda_{on}\Delta$t and if Δt is infinitesimally small, (17) can be simplified as:

$$\frac{dp_{on}(t)}{dt} + 2p_{on}(t)\,\lambda_{on} = \lambda_{on}. \tag{9}$$

$$P_{on}(t) = 0.5 + ae^{-2\lambda_{on}t}, 0 \le t < T/n, \tag{10}$$

where 'a' is a constant which is dependent on the PTO at initial condition ($t = 0$) of the ON state.

Similarly $p_{off}(t)$ is the PTO at time t, during OFF time of the device. As $p_{off}(t)$ is also a time-varying function, the probability of any event in infinitesimally small time interval Δt, can be given as:

$$\begin{aligned} p_{off}(t+\Delta t) &= p_{off}(t)\,.(\text{probability of zero emission event in } \Delta\text{t}) + \left(1-p_{off}(t)\right).(\text{probability of a capture in } \Delta\text{t}), \\ p_{off}(t+\Delta t) &= p_{off}(t)\,.(1-\lambda_e\Delta t) + \left(1-p_{off}(t)\right)\lambda_c\Delta t. \end{aligned} \tag{11}$$

For OFF state of transistor, the probability of trap to capture an electron is almost zero, as the number of charge carriers are negligible, then $\lambda_c \approx 0$ and $\lambda_e = \lambda_{off}$,

$$p_{off}(t+\Delta t) = p_{off}(t).(1-\lambda_{off}\Delta t). \quad (12)$$

$$dp_{off}(t)/dt = -p_{off}(t)\lambda_{off}. \quad (13)$$

$$P_{off}(t) = be^{-\lambda_{off}t}, \text{ for } T/n \le t < T, \quad (14)$$

where 'b' is the constant depends on the PTO at initial condition of the OFF state of transistor.

$$a = -(1-\beta)/(1-\alpha\beta); b = (1-\alpha)/(1-\alpha\beta), \quad (15)$$

where $\alpha = e^{-2\lambda_{on}\frac{T}{n}}$, $\beta = e^{-\lambda_{off}\frac{(n-1)T}{n}}$.

In order to calculate the ACF function for trap state $N(t)$, it is necessary to calculate condition probability of trap to be filled at time $(t+\tau)$, with the condition that $p(t) = 1$ (applicable for both ON as well as OFF time). This way conditional probabilities for trap occupancy at some arbitrary time $(t+\tau)$, with the condition that trap is full at time t, is:

$$P_{on,11}(t) = \frac{1}{2}\left(1 + e^{-2\lambda_{on}|\tau|}\right), 0 \le t < T/n, t \ge 0. \quad (16)$$

$$P_{off,11}(t) = e^{-\lambda_{off}|\tau|}), 0 \le t < (T-1)/n, t \ge 0. \quad (17)$$

Derivation of time averaged ACF function $C_\lambda(t,\tau)$ of $N(t)$ for ON and OFF time of transistor:

$$C_\lambda(t,\tau) = \mathbb{E}\left[N(t-\tau/2).N(t+\tau/2)\right] - \mathbb{E}\left[N(t-\tau/2)\right].\mathbb{E}\left[N(t+\tau/2)\right]. \quad (18)$$

ACF function $C^\tau_{\lambda,on}(t,\tau)$ for ON time

$$\begin{aligned} C_{\lambda,on}(t,\tau) &= p_{on}(t-\tau/2)\,p_{on,11}(\tau) \\ &\quad - p_{on}(t-\tau/2)\,p_{on,11}(t+\tau/2), \\ &= 0.25e^{-2\lambda_{on}|\tau|} - a^2e^{-4\lambda_{on}t}, \\ &\text{for } |\tau/2| \le t < T/n - |\tau/2| \text{ with } |\tau| \le T/n. \end{aligned} \quad (19)$$

Time average of $C^\tau_{\lambda,on}(t,\tau)$ for ON state of the transistor:

$$\begin{aligned} C^s_{\lambda,on}(\tau) &= \frac{1}{T}\int_{\left|\frac{\tau}{2}\right|}^{\frac{T}{n}-\left|\frac{\tau}{2}\right|} C^\tau_{\lambda,on}(t,\tau)\,dt, \\ &= (1/4T)\left[e^{-2\lambda_{on}|\tau|}\left(T/n - a^2/\lambda_{on} - |\tau|\right)\right. \\ &\quad \left. + \left(a^2/\lambda_{on}\right)\left(e^{-\frac{4\lambda_{on}T}{n}}.e^{2\lambda_{on}|\tau|}\right)\right], \\ &\text{for } |\tau| \le T/n. \end{aligned} \quad (20)$$

The RTS noise PSD for ON state of switched bias transistor is calculated by the Fourier transform of time averaged ACF, $C^s_{\lambda,on}(\tau)$:

$$S^{on}_\lambda(\omega) = \mathcal{F}\left(C^s_{\lambda,on}(\tau)\right) = \int_{-\frac{T}{2}}^{\frac{T}{2}} C^s_{\lambda,on}(\tau)\,e^{-j\omega\tau}d\tau. \quad (21)$$

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