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Investigation of Channel Doping Concentration and Reverse Boron Penetration on P-Type Pi-Gate Poly-Si Junctionless Accumulation Mode FETs

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ABSTRACT In this paper, the influence of channel doping concentration and reverse boron penetration on p-type Pi-gate (PG) poly-Si junctionless accumulation mode (JAM) FETs has been experimentally investigated and discussed. Effective carrier concentration (N_{eff}) and threshold voltage (V_{TH}) are found to be sensitive to doping concentration. Moreover, the positive shift in V_{TH} and the degradation in the subthreshold behavior for PG JAM FETs are observed after an additional source/drain (S/D) activation process. Using a low thermal-budget S/D activation process, PG JAM FETs with a suitable channel doping concentration can show excellent electrical characteristics: 1) steep subthreshold swing of 86 mV/dec.; 2) low average subthreshold swing (A.S.S.) of 96 mV/dec.; and 3) high ON/OFF current ratio (I_{ON}/I_{OFF}) of 7.7×10^7 (I_{ON} at $V_G - V_{TH} = -2$ V and $V_D = -1$ V).

INDEX TERMS 3-D integrated circuits (ICs), channel doping concentration, reverse boron penetration, Pi-gate (PG), poly-Si, junctionless accumulation mode (JAM).

I. INTRODUCTION

Recently, junctionless nanowire transistors (JNTs) have been proposed and demonstrated as promising new devices, featuring simple fabrication processes and best possible short-channel effect (SCE) immunity [1]–[3]. Based on the utilization of poly-Si junctionless (JL) transistors for 3-D integrated circuit (IC) applications [4]–[8], the evolution of p-type poly-Si JL transistors is essential to combine with n-type poly-Si JL transistors forming CMOS devices. Until now, only a few p-type poly-Si JL transistors [9], [10] and junctionless accumulation mode (JAM) transistors [11] have been demonstrated. To acquire excellent gate-to-channel controllability, a hybrid P/N channel was introduced to effectively turn the p-type poly-Si JL transistors off by an inherent depletion width [9]. However, this results in an increase in fabrication complexity and the occurrence of intermixing within the hybrid P/N channel.

Recently, JAM transistors have been proposed and developed to overcome several drawbacks in JL transistors regarding a more severe threshold voltage (V_{TH}) fluctuation [7], [12]–[15] and a higher S/D series resistance (R_{SD}) [11], [16] by simultaneously reducing the channel doping concentration (N_{ch}) and enhancing the S/D doping concentration ($N_{S/D}$). Compared with the channel region in JL transistors with the same homogeneously doping types and heavily doping concentration as the S/D region [2], [8], the channel region in JAM transistors has a lower doping concentration (higher channel resistance) than that of the S/D region [2]. Furthermore, in the ON-state, based on the use of an identical work function gate, the current transport mechanism for JAM transistors is similar to surface conduction under a high electric field rather than bulk conduction, which is the current transport mechanism of JL transistors under a low electric field [2], [3].

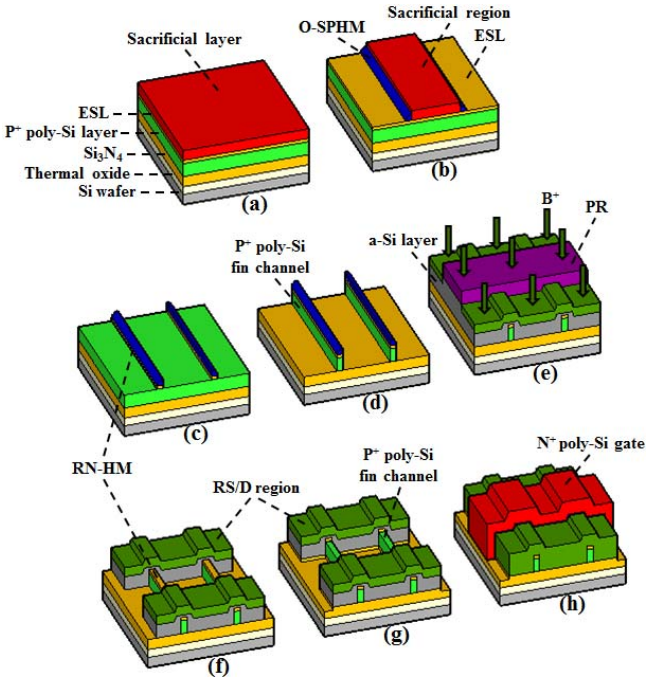

FIGURE 1. **(a)-(h) Schematic 3-D structure of a PG JAM FET for the key fabrication steps.**

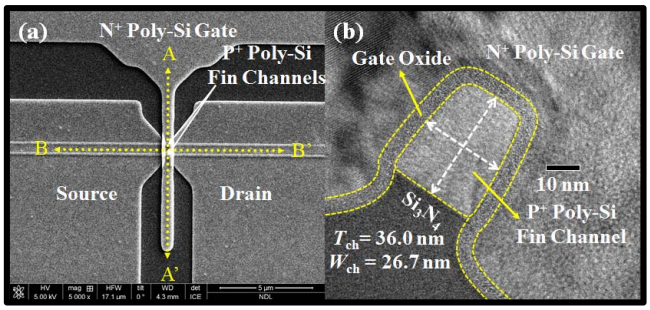

FIGURE 2. **(a) Top view SEM image of PG JAM FETs with the p^+ poly-Si fin channels at channel length $L_C = 0.35$ μm. (b) Cross-sectional TEM image of PG JAM FETs with a Pi-gate configuration along A-A′ marked in Fig. 2(a).**

For p-type JL or JAM transistors with a heavily doped p^+ channel, it is expected that the boron atoms will significantly penetrate through the gate oxide from the p^+ channel toward the n^+ gate electrode during a high thermal-budget process, namely, reverse boron penetration. This accompanies the degradation in the electrical characteristics of p-type JL or JAM transistors. This is similar to the phenomenon (boron penetration) in p-type inversion-mode (IM) transistors with a heavily doped p^+ poly-Si gate [17]–[19]. As a result, in this study, we explore the influence of N_{ch} and the thermal budget of the S/D activation process on device performance to further evaluate the optimum N_{ch} and mitigate the reverse boron penetration.

II. DEVICE FABRICATION

The schematic 3-D structure of a PG JL FET for the key fabrication steps is shown in Fig. 1. First, the silicon nitride (Si_3N_4) layer with a film thickness of 150 nm was deposited on the 500-nm-thick thermal oxide grown on a Si wafer. Next, the 40-nm-thick undoped amorphous-Si (a-Si) layer was deposited by low-pressure chemical vapor deposition (LPCVD) and then crystallized during the solid-phase crystallization (SPC) process at 600°C for 24 h in N_2 ambient. Subsequently, the undoped poly-Si layers were implanted with 18-keV boron difluoride ions (BF_2^+) to doses of 4×10^{12} cm^{-2}, 2×10^{13} cm^{-2}, 8×10^{13} cm^{-2}, and 4×10^{14} cm^{-2}. After the dopant activation, an 11-nm-thick etching stopping layer (ESL) and a 50-nm-thick sacrificial layer (n^+ poly-Si) were continuously deposited by LPCVD [Fig. 1(a)]. After the patterning of the sacrificial regions, the 50-nm-thick tetraethoxysilane (TEOS) oxide was deposited by LPCVD and then etched to form the oxide-spacer hard masks (O-SPHMs) [Fig. 1(b)]. Subsequently, the O-SPHMs were left in the left-hand and right-hand sides of the sacrificial regions after they were completely removed. Next, the O-SPHMs were utilized as the first hard masks to define the rectangular silicon nitride-hard masks (RN-HMs) [Fig. 1(c)]. After the p^+ poly-Si fin channel formation [Fig. 1(d)], an undoped a-Si layer of 100 nm was deposited by LPCVD. Following the patterning of the gate-shaped photoresist (PR), the undoped a-Si layer of 100 nm was implanted with boron ions (B^+) to a dose of 2×10^{15} cm^{-2} [Fig. 1(e)]. By means of the RN-HMs as the second hard masks, the p^+ poly-Si fin channels and the raised source/drain (RS/D) regions were concurrently patterned by anisotropic dry etching [Fig. 1(f)]. The Si_3N_4 adjacent to and above the p^+ poly-Si fin channels was removed partially and entirely, respectively, using a hot phosphoric acid (H_3PO_4) etchant to enhance the gate controllability [Fig. 1(g)]. The gate stack formation was composed of 5-nm-thick TEOS oxide and 200-nm-thick n^+ poly-Si gate. Then, the p^+ RS/D regions were further activated by an additional S/D activation process at 700°C for 2.5 h. The gate formation was performed to complete the PG JAM FETs [Fig. 1(h)]. For comparison, some PG JAM FETs, serving as modulated devices, were also fabricated without the additional S/D activation process. Fig. 2(a) presents the top view scanning electron microscopy (SEM) image of the PG JAM FETs with the p^+ poly-Si fin channels at channel length $L_C = 0.35$ μm, and Fig. 2(b) presents the cross-sectional transmission electron microscopy (TEM) image of the PG JAM FETs with a Pi-gate configuration along A-A' marked in Fig. 2(a). Fig. 2(b) clearly shows that the channel thickness (T_{ch}) × the channel width (W_{ch}) and the effective channel width ($W_{eff} = 2\times T_{ch} + W_{ch}$) for the PG JAM FETs are, respectively, 36.0 nm × 26.7 nm and 98.7 nm.

III. RESULTS AND DISCUSSION

The p^+ poly-Si fin channels of PG JAM FET-A, PG JAM FET-B, PG JAM FET-C, and PG JAM FET-D were separately doped with N_{ch} values of 1×10^{20}, 2×10^{19}, 5×10^{18}, and 1×10^{18} cm^{-3}, respectively. Fig. 3 presents the Hall hole concentration and the resistivity of the un-patterned p^+

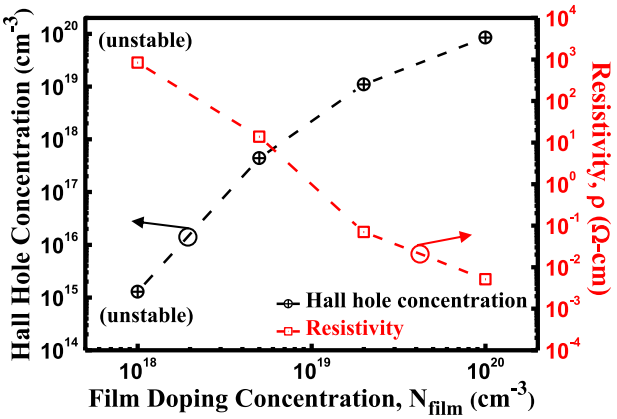

FIGURE 3. Hall hole concentration and resistivity of the un-patterned p^+ poly-Si films with different doping concentrations.

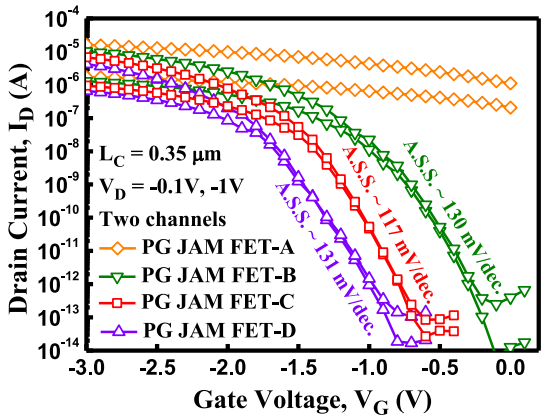

FIGURE 4. Comparison of the transfer characteristics of PG JAM FETs with different channel doping concentrations.

poly-Si films with different doping concentrations ($N_{film} = N_{ch}$). The Hall hole concentration can obviously enhance as N_{film} becomes higher than 1×10^{18} cm^{-3} in relation to the grain boundary defects that are abundantly saturated with the p-type dopants [20]. In addition, the resistivity (ρ) reduces with an increase in N_{film} [20]. As can be seen in Fig. 3, this finding implies that the careful adjustment of N_{ch} must be noted in poly-Si JAM FETs. Fig. 4 shows the transfer characteristics of the PG JAM FETs with different N_{ch}. For PG JAM FET-A with a relatively high N_{ch}, the drain current cannot be effectively modulated because W_{ch} for this device is too wide to be fully depleted. In other words, the doping level in this device is too high to acquire a fully depleted fin channel by the gate bias within a bias range of -3 V to 0 V [21]. V_{TH} values for the PG JAM FETs, defined by a constant current of 5×10^{-9} A, are -0.91 V for PG JAM FET-B, -1.31 V for PG JAM FET-C, and -1.60 V for PG JAM FET-D. The obvious variation between these values means that V_{TH} is highly sensitive to the doping concentration [12], [22]. A superior device performance for PG JAM FET-C with a suitable N_{ch} (5×10^{18} cm^{-3}) is observed in terms of both the best average

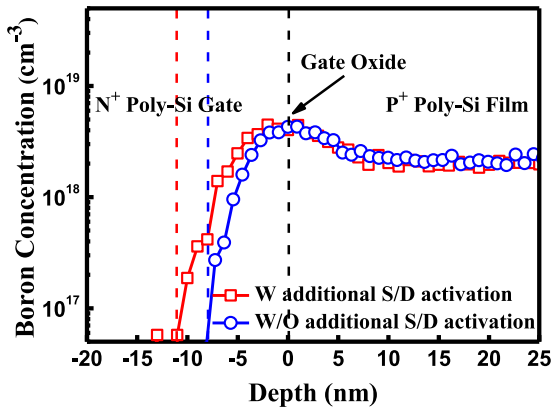

FIGURE 5. SIMS depth profiles of the un-patterned p^+ poly-Si films ($N_{film} = 5 \times 10^{18}$ cm^{-3}) with and without the additional S/D activation process after the gate stack formation.

subthreshold swing (A.S.S.) of 117 mV/dec. and highest ON/OFF current ratio (I_{ON}/I_{OFF}) of 1.1×10^8 (I_{ON} at $V_G - V_{TH} = -2$ V and $V_D = -1$ V) among these devices. It should be noted that the augmentation in N_{ch} can not only enhance the effective carrier concentration (N_{eff}) but also increase impurity scattering [23]. Consequently, I_{ON} for PG JAM FET-B with a higher N_{ch} is slightly larger than that for PG JAM FET-C.

Three simulation results were proposed in the previous literatures [3], [23], [24]. First, Liu *et al.* [24] showed that the enhancement in the carrier density near the surface of the channel for the JAM transistor with a lower N_{ch} (5×10^{17} cm^{-3}) is larger with the increase of V_G in the subthreshold region than that of the JAM transistor with a higher N_{ch} (1×10^{19} cm^{-3}). In addition, for the JAM transistor, the carrier density and current density near the surface of the channel are higher than that in the center of the channel at $V_G - V_{TH} = 1$ V [24]. Second, Akhavan *et al.* [3] and Wei *et al.* [23], respectively, showed that the drain current in the IM transistor slowly increases with an increase in V_G and the carrier mobility in the IM transistor obviously decreases with an increase in the carrier density when the IM transistor operates under strong inversion (high carrier density or ON-state). This indicates that the carriers of JAM transistors would undergo strong surface scattering and phonon scattering as JAM transistors with a low N_{ch} operate under strong accumulation (high carrier density or ON-state) [2], [3]. According to the above-mentioned analyses and explanations, the hole current in PG JAM FET-D with the lowest N_{ch} ($N_{eff} \sim 1.3 \times 10^{15}$ cm^{-3}) could suffer from more serious effects associated with the defective interface, surface scattering, and phonon scattering [2], [3]. This is because the current transport mechanism for this device tends toward surface conduction, resulting in the degradation in A.S.S. and the reduction in I_{ON}.

Fig. 5 displays the secondary ion mass spectroscopy (SIMS) depth profiles of the un-patterned p^+ poly-Si films ($N_{film} = 5 \times 10^{18}$ cm^{-3}) with and without the additional S/D activation process after the gate stack

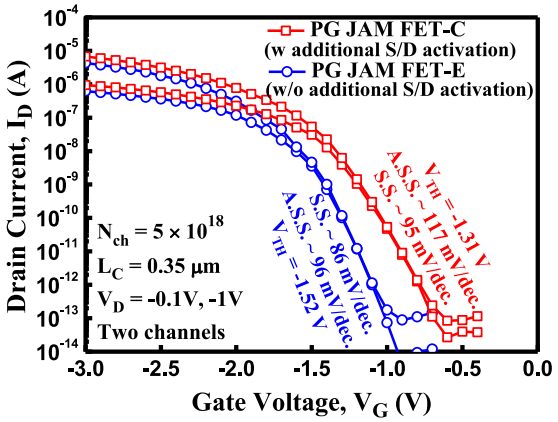

FIGURE 6. Comparison of the transfer characteristics of PG JAM FETs with and without the additional S/D activation process after the gate stack formation.

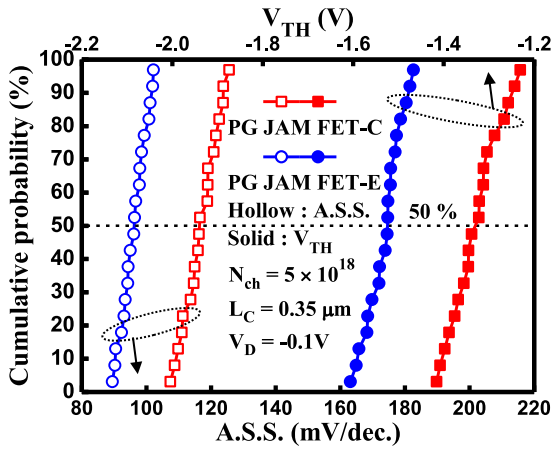

FIGURE 7. Cumulative probability of the A.S.S. and V_{TH} for PG JAM FETs with and without the additional S/D activation process after the gate stack formation.

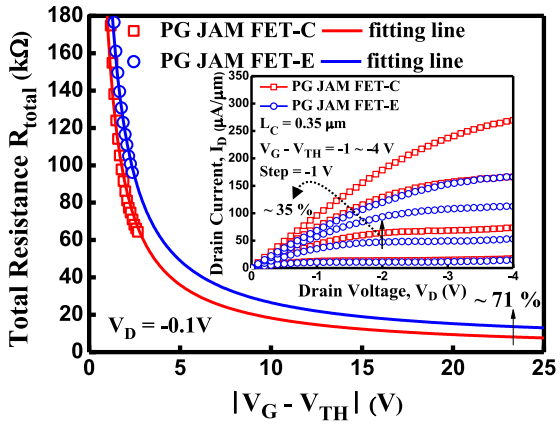

FIGURE 8. Extracted R_{total} as a function of V_G for PG JAM FETs with and without the additional S/D activation process after the gate stack formation. Inset: comparison of output characteristics for both devices.

TABLE 1. Comparison of key parameters for this study and other published P-type Poly-Si JL and JAM FETs.

	This study	Ref. [9]	Ref. [9]	Ref. [11]
Operation Mode	**JAM**	JL	JL	JAM
Gate Structure	**Pi-Gate**	Omega-Gate	Omega-Gate	Double-Gate
$T_{ch} \times W_{ch}$ (nm × nm)	**36.0 × 26.7**	12.0 × ~ 28.0	24.0 × 28.0	82.8 × 23.0
W_{eff}/L_C or L_G (μm/μm)	**0.099×2/0.35**	~ 0.052×10/1	0.076×10/1	0.166×2/2
N_{ch} (cm^{-3})	**5×10^{18}**	5×10^{19}	5×10^{19}	5×10^{19}
R_{SD} (kΩ)	**13.0**	~ 16000.0	~ 350.0	12.4
ΔV_{TH} (V)	**0.14**	0.32	0.91	0.92
S.S. (mV/dec.) (Median)	**86**	113	93	180
I_{ON} (μA/μm) (V_G-V_{TH};V_D)	**47.58 (-2V;-2V)**	0.14 (-3V;-3V)	0.75 (-3V;-3V)	10.54 (-2V;-2V)
I_{ON}/I_{OFF} (V_G-V_{TH};V_D)	**7.7×10^7 (-2V;-1V)**	3.0×10^5 (-2V;-0.4V)	1.0×10^7 (-2V;-0.4V)	5.0×10^6 (-2V;-0.5V)
Hybrid P/N Channel	**W/O**	W/O	W	W/O

formation. It is worth noting that more boron atoms can penetrate through the gate oxide from the p^+ poly-Si fin channel toward the n^+ poly-Si gate electrode after the additional S/D activation process. The transfer characteristics of the PG JAM FETs with (PG JAM FET-C) and without (PG JAM FET-E) the additional S/D activation process after the gate stack formation are presented in Fig. 6. Compared with that of PG JAM FET-C, PG JAM FET-E exhibits a steeper S.S. of 86 mV/dec., a lower A.S.S. of 96 mV/dec., and a more negative V_{TH} of -1.52 V. Fig. 7 illustrates the cumulative probability of the A.S.S. and V_{TH} for PG JAM FETs with (PG JAM FET-C) and without (PG JAM FET-E) the additional S/D activation process after the gate stack formation. For PG JAM FET-C, the A.S.S. deteriorates mainly because of an increase in the interface state density [17]–[19], and the positive shift in V_{TH} is largely attributed to the further generation of the negative fixed charge within the gate oxide [18], [19] compared with that of PG JAM FET-E. Moreover, note that I_{ON} for PG JAM FET-E is lower than for PG JAM FET-C, as shown in Fig. 7.

To better understand and analyze the decline in I_{ON} for both devices, R_{SD} is derived from $R_{total} = R_{SD} + (L_G) / [W_{eff} \times \mu_{eff} \times C_{ox} \times (V_G - V_{TH})]$ at $V_{DS} = -0.1$ V [25], where R_{total} is the total resistance, W_{eff} is the effective channel width, μ_{eff} is the effective mobility, and C_{ox} is the gate oxide capacitance. As $V_G - V_{TH}$ is close to infinity, the second term on the right-hand side of the equation can be ignored, i.e., R_{total} is equal to R_{SD}. Fig. 8 compares the extracted R_{total} as a function of V_G for PG JAM FETs with (PG JAM FET-C) and without (PG JAM FET-E) the additional S/D activation process after the gate stack formation. The extrapolated R_{SD} for PG JAM FET-E (~ 13.0 kΩ) has around 71% augmentation as compared with that for PG JAM FET-C (~ 7.6 kΩ). This shows that the S/D activation time for PG JAM FET-E may not be long enough to obtain a lower R_{SD}. The inset in Fig. 8 shows the output characteristics for both devices. The driving current augments around 35% from 47.58 μA/μm (PG JAM FET-E) to 64.10 μA/μm (PG JAM FET-C) at V_G - $V_{TH} = V_D = -2$ V, which corresponds to the result of R_{SD}, as presented in Fig. 8. Therefore, the optimization of the S/D activation condition is necessary to simultaneously improve R_{SD} and minimize the thermal

budget. Table 1 shows the comparison of the key parameters for this study and other published p-type poly-Si JL and JAM FETs. Among these devices, PG JAM FET-E exhibits not only a low R_{SD} owing to the utilization of the RS/D configuration but also the smallest threshold voltage fluctuation (ΔV_{TH}) as a result of the p^+ poly-Si fin channel with the lowest N_{ch} and PG JAM FET-E without the employment of the hybrid P/N channel. ΔV_{TH} for PG JAM FET-E can be further suppressed by the reduction of equivalent oxide thickness [7], [26]–[28] and the precise controllability of dry etching conditions [7]. In those categories of p-type poly-Si JL and JAM FETs, PG JAM FET-E displays the steepest S.S. of 86 mV/dec., the highest I_{ON} of 47.58 μA/μm, and a relatively high I_{ON}/I_{OFF} of 7.7×10^7.

IV. CONCLUSION

In this study, the influence of N_{ch} and reverse boron penetration on the electrical characteristics of p-type PG JAM FETs has been experimentally investigated and discussed. N_{eff} and V_{TH} for PG JAM FETs are highly sensitive to doping concentration. For the first time, it was found in p-type PG JAM FETs that more boron atoms can penetrate through the gate oxide from the p^+ fin channel toward the n^+ gate electrode after a higher thermal-budget process, leading to the positive shift in V_{TH} and the deterioration in the subthreshold behavior. By employing a suitable N_{ch} and a lower thermal-budget process for the S/D activation, PG JAM FETs can exhibit a steeper S.S., a lower A.S.S., and a relatively high I_{ON}/I_{OFF}, thereby becoming promising candidates for future 3-D IC applications.

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