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Heterogeneous Integration Toward a Monolithic 3-D Chip Enabled by III–V and Ge Materials

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ABSTRACT Monolithic 3-D integration has emerged as a promising technological solution for traditional transistor scaling limitations and interconnection bottleneck. The challenge we must overcome is a processing temperature limit for top side devices in order to ensure proper performance of bottom side devices. To solve this problem, we developed a low temperature III–V and Ge layer stacking process using wafer bonding and epitaxial lift-off, since these materials can be processed at a low temperature and provide extended opportunity/functionality (sensor, display, analog, RF, etc.) via heterogeneous integration. In this paper, we discuss technology for integrating III–V and Ge materials and its applicability to CMOS, thin film photodiodes, mid-infrared photonics platforms, and MicroLED display integration for creating the ultimate 3-D chip of the future.

INDEX TERMS Heterogeneous integration, monolithic 3D, sequential 3D, layer transfer, wafer bonding, epitaxial lift-off, III-V-OI, GOI, thin film PD, mid-IR photonics, microLED.

I. INTRODUCTION

Chip stacking is commonly used in recent commercialized products. Using vertical interconnection enabled by through Si via (TSV) technology in stacked chips, a significant improvement in bandwidth for the communications between the chips has been achieved [1], [2]. Similar concepts have been shown in image sensor development. To avoid the image distortion problem for moving subject, which is mainly caused by limitations in the readout speed in conventional CMOS image sensors (CIS), the 3-layer stacked structure of photodiodes (PD) on dynamic random access memory (DRAM) on logic circuits have demonstrated a very high frame speed rate [3]. Furthermore, TSV-linked stacking is actively used in DRAM development to mitigate the interconnection bottlenecks and achieve higher speeds [4], [5]. However, current chip stacking processes are mainly based on TSV technology, for which the issues of relatively large via dimension, alignment accuracy, and small via density remain unsolved [6]. Therefore, to utilize the ultimate benefits of 3D stacking, a process of monolithic and/or sequential 3D integration should be realized. Monolithic 3D (M3D) provides us with smaller via size and alignment accuracy, as well as dramatically increased via density as suggested in Leti's technology [6], [7].

Therefore, M3D integration has attracted lots of attention for continuing equivalent scaling by vertically stacked transistors [6], [7]. It allows for reduced interconnection delays, resulting in reduced power consumption by the chip, the driving force of M3D integration. Moreover, with

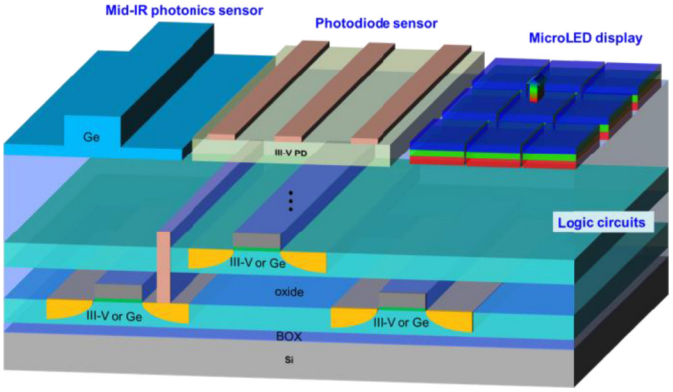

FIGURE 1. **Conceptual schematic image of the 3D heterogeneous integration and implementable applications including CMOS, photonic sensors, and microLED display.**

M3D, many other components such as digital, analog, MEMS, sensors, display, etc. can be heterogeneously integrated in a single chip to provide enhanced functionality. Fig. 1 shows the conceptual schematic image of the 3D heterogeneous integration including CMOS, photonic sensors, and MicroLED display. As shown in the figure, sensing and processing the information and finally displaying the output information will be possible in a single chip. In this context, M3D provides additional benefits by integrating two or more different materials [8]. Heterogeneous integration of different materials combined with M3D is greatly preferred, because processes using different materials do not require the same processing steps and sequence, allowing for greater flexibility in process design. Moreover, it naturally provides many benefits thanks to its advantageous physical properties. For instance, one can consider the introduction of high mobility channel materials such as III-V and Ge, and the use of different surface orientations for ultimate device performance.

On the other hand, one important issue of M3D is the process temperature limitation for stacking of active layers in semiconductors and fabricating top devices. Such limitation is caused by the thermal stability of bottom interconnects and bottom devices, as shown in Fig. 2 [7]. Therefore, to avoid performance degradation in these, the processing temperature of top devices should be kept low. To this end, III-V and Ge are promising materials, because their typical processing temperature are quite low compared to Si. They also have a high carrier mobility and proper bandgap for many photonic devices, such as PDs and displays [9]–[16]. However, there is still the challenging issue of how to stack different materials with high film quality. Therefore, in this paper, we present our recent development: low-temperature material integration technology for III-V and Ge for M3D integration. We also discuss possible applications resulting from III-V/Ge integration, including MOSFETs, PDs, Mid-IR sensing platforms and vertically stacked MicroLED displays.

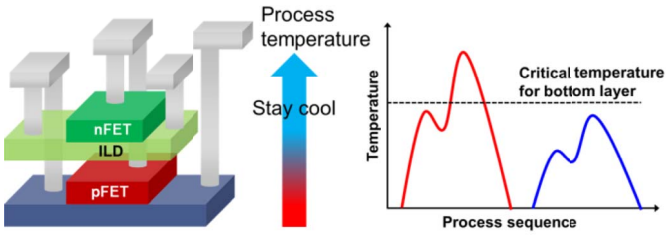

FIGURE 2. **Schematic image of typical process thermal budget issue for M3D integration.**

II. MATERIAL INTEGRATION OF III-V AND GE MATERIALS

Sequential stacking of III-V and Ge on Si substrate is not so simple, because there is a large lattice mismatch between these materials and Si. More importantly, epitaxial growth requires a very high growth temperature, thereby failing the M3D requirement of a low processing temperature. Furthermore, integration costs should always be considered for the real implementation of new materials and processes. To mitigate and overcome these problems, we developed the wafer bonding and epitaxial lift-off (ELO) techniques [17]–[20], through which we can fully utilize the good crystal quality of semiconductors' active layers and re-use the donor substrate, which leads to dramatic cost reduction [17]. Fig. 3 shows the typical process flow of III-V and Ge stacking on other substrates using the wafer bonding and ELO processes. After the epitaxial growth of active and sacrificial layers, a mesa patterning is carried out and a bonding medium (oxide or metal)/active device layer/sacrificial layer/III-V donor substrate and bonding medium/Si substrate are bonded to each other by plasma assisted bonding, which can be done even at room temperature. Here, when we use the Y_2O_3 bonding medium with O_2 plasma treatment, the typical bonding strength was around 0.5-1 J/m^2 according to razor blade cracking measurements. Then, the ELO process was followed by dipping the sample in an HF-based etching solution. Finally, separated III-V/Ge on Si substrates and donor substrates are used for device fabrication and subsequent epitaxial growths, respectively.

As reported so far, wafer bonding can be used to from a high film quality grown on lattice-matched substrates even after the layer transfer onto another substrate [21], [22]. One significant merit of the wafer bonding process would be controllability of the physical parameters of the active layer. All physical parameters such as thickness, homogeneity, composition, and roughness can be controlled during the initial epitaxial growth step, which is attributed to extremely high wet etching selectivity between active and sacrificial layers. Furthermore, non-destructive wafer splitting is possible using ELO, which enables re-use of the donor wafer. However, slow processing speed is the major obstacle utilizing this technique. Therefore, accelerating the ELO process is very important. Fig. 4 shows the possible origins of slow ELO reactions and requirements for fast processing. The possible physical origins are H_2 bubble generation during the ELO

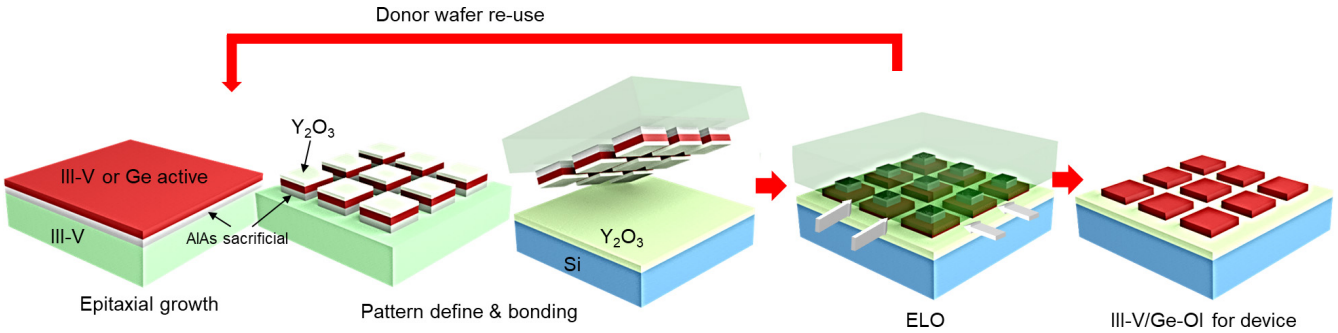

FIGURE 3. Process flow of wafer bonding and ELO to fabricate III-V/Ge on other substrate.

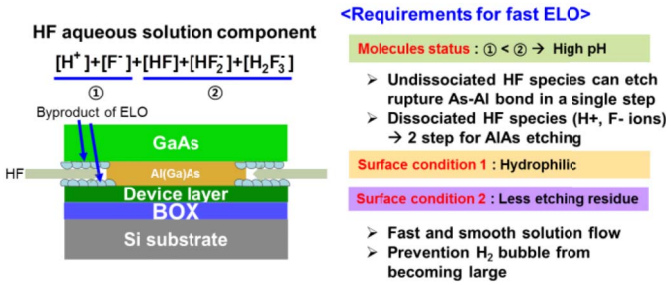

FIGURE 4. Schematic image of the ELO reaction and the requirements for fast ELO process.

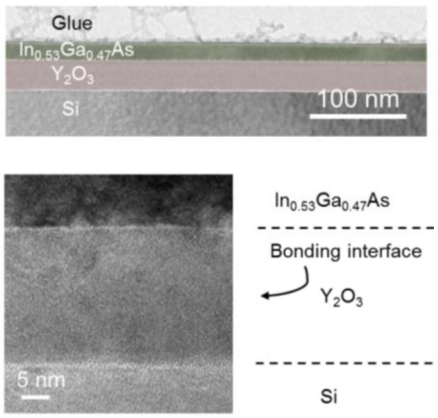

FIGURE 5. Cross-sectional TEM image of the transferred InGaAs-OI on Si substrates.

process, long lateral etching distance, hydrophobic semiconductor surfaces, and reaction residue (byproduct) [17], [19]. With these reasons in mind, to speed up the ELO process, we patterned III-V mesas before the wafer bonding. Patterning step before the wafer bonding, breaking III-V layers into smaller pieces, makes efficient H_2 bubble release and shortened physical etching distance. This pattern seems to limit the chip size, but transferring a larger scale wafer with many mesas is feasible and a long pattern shape with several hundreds of μm and a very long length can be transferred without ELO speed reduction. Furthermore, to make the ELO process faster, a high concentration of undissociated molecules in HF acid, hydrophilic surface, and reducing etching residues are critical [19]. First, an etching reaction of AlAs with undissociated HF is a one-step process, whereas that with dissociated HF takes a two-step process. Therefore, the former reaction gives a faster processing speed. Also, making the surface between the sacrificial layer and the facing semiconductor layer hydrophilic by the insertion of a hydrophilic substance or hydrophilic semiconductor layer (phosphide-based material) are beneficial for ELO processing. Through such engineering, we achieved a fast ELO process time of <1 hour [17]–[19]. Of course, the requirements for fast ELO reactions can be in trade-off relationships between each other. Therefore, a careful process design that properly takes into account each material system (e.g., GaAs, InP, etc.) is required. Additionally, use of ultra/mega-sonic can help to divide the generated hydrogen bubble into smaller ones during the ELO and to make the solution flow smoother, further enhancing the ELO speed.

After splitting of the active device layer and donor wafer, we verified the re-usability of the donor substrate for the cost reduction [17], [18].

III. CMOS INTEGRATION

Using the wafer bonding and ELO techniques, we successfully fabricated III-V-on-insulator (III-V-OI) transistors on Si substrates [17]–[19], [23]. An appropriate choice of the donor substrate and the corresponding active layer design is possible (e.g., GaAs donor substrate → GaAs, In-poor InGaAs channel, InP donor substrate → In-rich InGaAs channel). Here, we discuss about III-V-OI transistor demonstration. First, we fabricated InGaAs-OI substrate by wafer bonding and ELO from an InP donor substrate with a thin AlAs sacrificial layer. Then, using the fabricated InGaAs-OI substrate, we fabricated 20-nm-thick channel InGaAs-OI MOSFETs with a $Pt/Al_2O_3/Y_2O_3/InGaAs$ gate stack and a gate-recessed structure [24]. Here, a maximum processing temperature was below than 300°C, which is much lower than conventional back-end-of-line (BEOL) processes. It would be very beneficial for M3D integration. Fig. 5 shows the cross-sectional transmission electron microscope (TEM) image of the bonded InGaAs-OI layer on Si. It clearly shows the uniform bonding behaviors and absence of visible

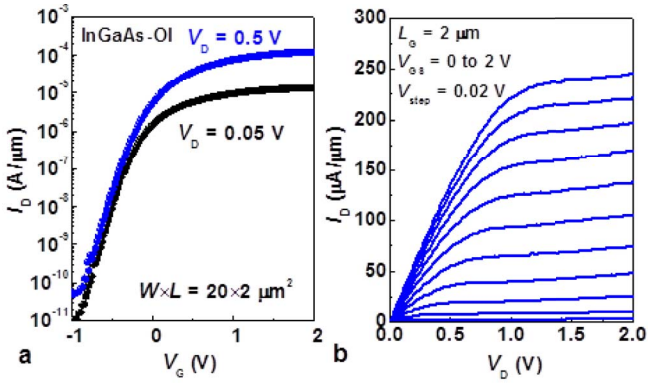

FIGURE 6. (a) Transfer and (b) output characteristics of 20-nm-thick top-gated InGaAs-OI MOSFETs fabricated by wafer bonding and ELO techniques [18].

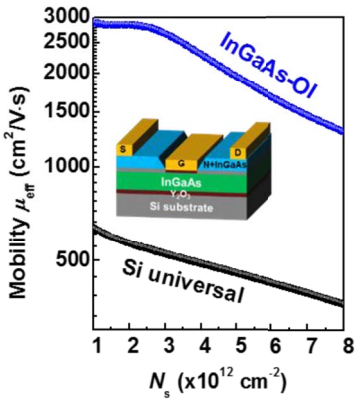

FIGURE 7. The μ_{eff} characteristics of top-gated InGaAs-OI MOSFETs. μ_{eff} characteristics of Si MOSFETs are also shown as a reference [18].

defects. Furthermore, even with this low processing temperature, we achieved very good current (I)–voltage (V) curves. Fig. 6 shows transfer and output curves of the fabricated InGaAs-OI MOSFETs. High on/off ratio of approximately 10^6 and low subthreshold slope ($S.S.$) of 120 mV/dec were obtained. Fig. 7 shows the effective mobility (μ_{eff}) characteristics from the fabricated MOSFETs. The μ_{eff} is remarkably high of $>$ 2,800 cm^2/Vs. This value is roughly 4 times higher than that of Si MOSFETs, as shown in the same graph. Also, it is the highest value at given EOT compared to other surface channel InGaAs MOSFETs [18]. We believe that this would be attributed to the good crystal quality of the channel and MOS interface as well. This μ_{eff} in InGaAs-OI MOSFETs was even higher than that of InGaAs MOSFETs fabricated on InP substrates due to more favorable carrier distribution, which has more carriers in the centroid of the channel layer.

As mentioned in the Introduction, not only III-V, Ge is also a very promising material for M3D integration. Especially, Ge has very good hole transport characteristics than III-V or Si with comparable electron transport characteristics. Ge channel MOSFETs can also be integrated using similar approach, since one can grow a high quality Ge layer

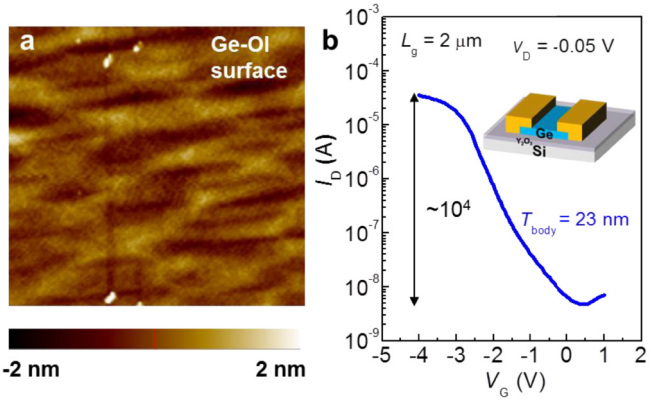

FIGURE 8. (a) AFM image of fabricated 23-nm-thick GOI surface and (b) transfer curve of 23-nm-thick back-gated GOI MOSFET fabricated using epitaxial Ge grown on AlAs.

on GaAs or AlAs due to almost the same lattice constant between them [25]. With a similar approach shown in Fig. 3, we fabricated GOI substrates. Fig. 8(a) shows the surface atomic force microscope (AFM) image of the fabricated GOI surface. It shows very flat and smooth surfaces with a root mean square roughness (R_{rms}) of 0.41 nm. Simple bottom-gated 23-nm-thick GOI MOSFETs using Ge layer grown on AlAs shows a good gate modulation and high on/off ratio of 10^4 in the transfer curve, as shown in Fig. 8(b).

These results strongly suggest that our wafer bonding and ELO can provide very high quality single crystalline III-V-OI or GOI structure at low enough temperature of <400°C for M3D integration.

IV. THIN FILM PD INTEGRATION

Wafer bonding of III-V on Si can be used to fabricate hybrid III-V imagers on Si. By stacking thin film PD layers, co-integration of PD layer and readout integrated circuits (ROICs) is possible. It also allows us to minimize the use of active materials, which leads to the cost reduction. Moreover, lots of combinations of III-V compound semiconductors provide a very broad coverage of detection wavelengths from ultraviolet (UV) to infrared (IR). In terms of the ELO processes, increasing resolutions in the PDs provides another benefit to reduce the ELO processing time, because reduction of mesa size (increase of resolution) naturally reduces ELO time, as shown in Fig. 9 [27]. Here, as a proof-of-concept, we recently demonstrated GaAs pin PD arrays transferred onto Si substrates for visible wavelength detection [27]. Fig. 10 shows a bird-eye view of GaAs pin PD on Si. The PD arrays were uniformly transferred onto Si substrate and electrode formation for each pixel array was clearly seen in the inset image. Photoresponse of the fabricated PD was measured using 635 nm laser. Fig. 11(a) shows the I-V curves of GaAs PD with and without light illumination. Clear photoresponse was obtained in this device. Measured external quantum efficiency (EQE) in Fig. 11(b) confirms a response wavelength band of GaAs.

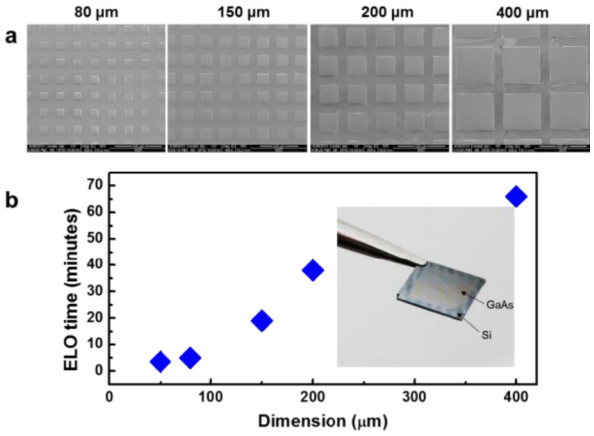

FIGURE 9. (a) Top-view of SEM image of transferred GaAs layer on Si substrate with a different mesa size. (b) Mesa dimension dependence of ELO time.

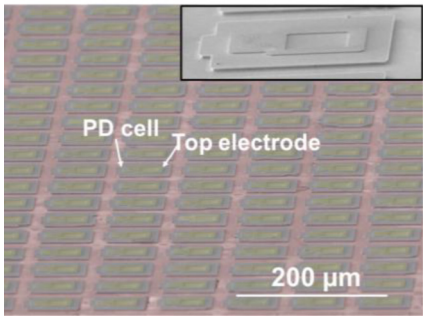

FIGURE 10. Bird-eye view of GaAs PD array on Si fabricated by wafer bonding and ELO. Inset shows the enlarged SEM image of one pixel.

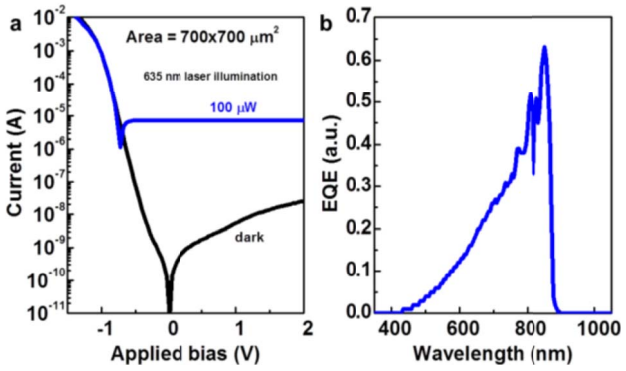

FIGURE 11. (a) The *I-V* characteristics of GaAs PD with and without light illumination. (b) EQE spectra of fabricated GaAs PD, showing absorption band of GaAs.

Furthermore, one of the advantages employing III-V compound semiconductor material system is the IR detection using an intra-band transition of carriers in quantum well (QW) or quantum dot (QD). We recently demonstrated a thin film QD infrared photodetector (QDIP) on Si substrates [13]. Fig. 12(a) shows the schematic cross-section of the fabricated QDIP on Si. Using a metal bonding medium, the enhanced photoresponse was obtained even in

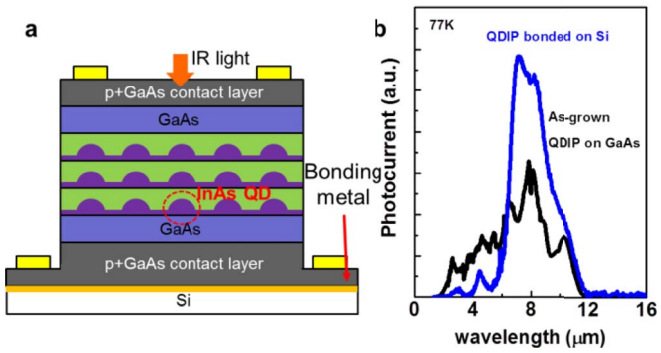

FIGURE 12. (a) Cross-sectional schematic image of the QDIP bonded on Si substrates by metal (Pt/Au) bonding medium. (b) Photocurrent characteristics of QDIP grown on GaAs and QDIP bonded on Si as a function of light wavelength.

thin film structure thanks to the light reflection from the bottom metal. Fig. 12(b) shows the photocurrent characteristics of QDIP grown on GaAs and the QDIP bonded on Si at 77K as a function of the light wavelength. We obtained a clear photoresponse from both samples at long wavelength up to approximately 12 μm. It should be noted that enhanced photoresponse was observed in QDIP bonded on Si at around 8 μm, which corresponds to the cavity resonance.

V. GOI MID-IR PHOTONIC CIRCUITS INTEGRATION

A waveguide with a high refractive index core and low refractive index cladding is an essential building block to form the photonic integrated circuits. Si photonics platform, which is realized by Si core waveguide and SiO_2 cladding, has shown a great possibility and its applicability for data communication and simple sensing applications. However, due to the transmittance range limitation of Si and SiO_2, Si photonics platform is only useful with a target wavelength shorter than 3 μm [28]. On the other hand, Mid-IR wavelength ranges cover the absorption band of various gases and bio-materials. Therefore, a photonics platform applicable to Mid-IR wavelength range is strongly needed to fabricate a compact photonic sensing chip, as described in Fig. 1. Furthermore, this photonics platform should have a low thermal resistance to guarantee the stable operation of the light source and temperature sensitive passive components. Toward this, we suggested GOI photonics platforms with Ge core and Y_2O_3 (or CaF_2) cladding layer [29]. Fig. 13(a) shows the electric field distribution of optical mode in our GOI photonics platform at wavelength of 5 μm. It shows a strong optical confinement in Ge waveguide layer thanks to the large refractive index contrast between Ge core waveguide and Y_2O_3 cladding layer, as shown in Fig. 13(b). Like this, a strong optical confinement is essential property for compact device. Of course, it would be weak point for optical sensing. However, it can be mitigated by co-integrating a slot waveguide in the sensing part to enhance the interaction between the light and target material [30]. Furthermore, we found that materials in this platform are

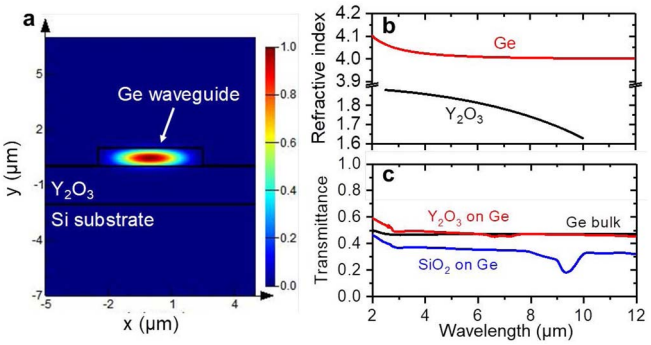

FIGURE 13. **(a) Mode profile of Ge-on-Y_2O_3 waveguide. (b) Refractive index of Ge and Y_2O_3. (c) Transmittance of Ge bulk, Y_2O_3 on Ge and SiO_2 on Ge measured by FTIR.**

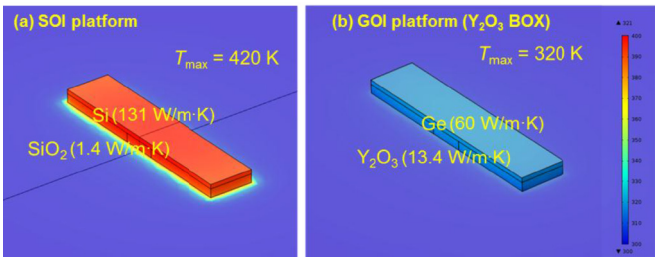

FIGURE 14. **Temperature distribution of (a) conventional SOI platform and (b) our GOI platform with same amount of the heat source on the top.**

optically transparent up to at least 12 μm by measuring the transmittance of 200-nm-thick Y_2O_3 on Ge sample by Fourier-transform infrared spectroscopy (FTIR). On the contrary, SiO_2 shows strong absorption at Mid-IR wavelength range, indicating conventional SOI platform cannot be used in Mid-IR wavelength range.

To investigate the impact of thermal resistance of the suggested platform, we simulated a temperature distribution with a heat source on the top of the waveguide. As a control platform, we also investigated SOI platform. Fig. 14 shows a temperature distribution of conventional SOI platform and suggested GOI platform with same amount (20 mW) of the heat source on the top. It is obvious that maximum temperature (T_{max}) is very different between these two platforms, T_{max} of GOI platform is much lower than that of SOI platform, indicating heat dissipation is strongly enhanced by using Y_2O_3 cladding layer with a large thermal conductivity. We believe that this GOI structure will be a strong technology platform for future compact sensing chips.

VI. MICROLED DISPLAY INTEGRATION

As shown in Fig. 1, one of the final output signals of the ultimate 3D chip would be a display. To overcome material limitations of organic light emitting diode (OLED) display (low brightness, scalability), MicroLED display with an inorganic LED is strongly needed for ultra-small, ultra-high resolution display, which is used in augmented reality (AR), virtual reality (VR), hologram, etc and can be implemented in 3D chip. However, there is no common substrate to emit

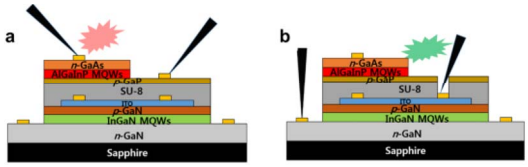

FIGURE 15. **Cross-sectional schematic of fabricated stacked multi-color and its configuration.**

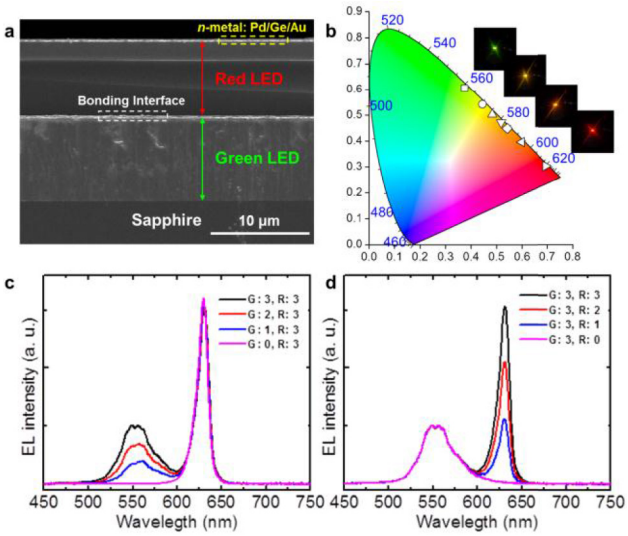

FIGURE 16. **(a) Cross-sectional SEM image of stacked multi-color LED using AlGaInP-based red and InGaN-based green QW layers. (b) CIE 1931 x-y chromaticity diagram of the fabricated device and its (c), (d) EL spectra with changing the bias weight.**

multi-wavelength light (red, green, blue). Therefore, lots of efforts have been devoted to package the RGB pixels one by one with pick-and-place method [31], [32]. However, it is still questionable whether or not this method provides reasonable production yield and pixel resolution for volume-manufacturing. Therefore, to avoid multiple pixel transfer and reduce the pixel footprint, we recently demonstrated vertically stacked multi-color inorganic LED array using the wafer bonding [15], [16]. Fig. 15 shows the schematic image of the fabricated red/green multi-color LEDs and its probing mode for red and green light emission. As a conceptual device, we fabricated red/green LED by stacking AlGaInP-based red multi quantum wells (MQWs) on InGaN-based green MQWs grown on sapphire substrates. This multi-stacking was realized by optically transparent bonding medium of SU-8 layer.

Fig. 16(a) shows the cross-sectional scanning electron microscope (SEM) image of the fabricated red/green multi-color LED. Red MQWs and green MQWs appear with a different contrast in the figure and it clearly shows the uniform bonding behaviors covering large area. We demonstrated very broad coverage of CIE color coordinate in our devices by changing the bias weight ratio for red and green LEDs as shown in Fig. 16(b). Figures 16(c) and 16(d) show the electroluminescence (EL) spectra of the stacked LEDs

with different bias weight. These figures clearly show the independent controllability of each color and its applicability for multi-color operation. Further pixel scaling and optimization will provide the possible solution for low power and high resolution display. Here, green LED used in this work was grown on Sapphire substrate, but it can be replaced by Si substrate for further cost reduction [33], [34].

VII. CONCLUSION

We developed low-temperature material integration technology for III-V/Ge stacking using wafer bonding and ELO techniques for M3D integration. By patterning semiconductor mesas before wafer bonding and making hydrophilic semiconductor surfaces, we realized a fast ELO process of less than an hour. With this bonding-based integration process, we achieved a MOSFET, thin film PD, and GOI Mid-IR photonics platform on Si substrates. Furthermore, we showed the process extendibility of wafer bonding to fabricate next-generation MicroLED displays. Finally, it should be noted that all these results remain limited in regard to III-V and Ge wafer size, but can be still extended for use in recent highly advanced hetero-epitaxial technology, which can provide high-quality III-V or Ge film on Si substrates [35]–[37]. We believe that the use of III-V and Ge materials will provide powerful integration functionality for various applications toward creating the ultimate 3D chip of the future.

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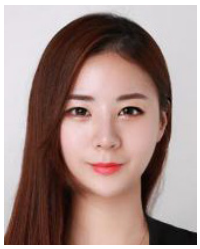

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