Germanium on Insulator Fabrication for Monolithic 3-D Integration

AHMAD ABEDIN, LAURA ZURAUSKAITE , A. ASADOLLAHI, KONSTANTINOS GARIDIS, GANESH JAYAKUMAR, B. GUNNAR MALM (Senior Member, IEEE), PER-ERIK HELLSTRÖM , AND MIKAEL ÖSTLING (Fellow, IEEE)

Department of Electronics, KTH Royal Institute of Technology, 164 40 Stockholm, Sweden

CORRESPONDING AUTHOR: P.-E. HELLSTRÖM (e-mail: pereh@kth.se)

ABSTRACT A low temperature ($T_{max} = 350\,°C$) process for Germanium (Ge) on insulator (GOI) substrate fabrication with thicknesses of less than 25 nm is reported in this paper. The process is based on a single step epitaxial growth of a Ge/SiGe/Ge stack on Si, room temperature wafer bonding and an etch-back process using $Si_{0.5}Ge_{0.5}$ as an etch-stop layer. GOI substrates with surface roughness below 0.5 nm, 0.15% tensile strain, thickness nonuniformity of less than 3 nm and residual p-type doping of less than 10^{16} cm^{-3} were fabricated. Ge pFETs are fabricated ($T_{max} = 600\,°C$) on the GOI wafer with 70% yield. The devices exhibit a negative threshold voltage of -0.18 V and 60% higher mobility than the SOI pFET reference devices.

INDEX TERMS GOI, wafer bonding, selective etching, GOI MOSFET, 3D integration.

I. INTRODUCTION

Monolithic 3D integration has been proposed as a way of increasing device packing density and reducing the length of interconnects [1]. Integration of two tiers of CMOS using fully-depleted (FD) Si MOSFETs has been demonstrated [2]. Improved performance of top tier devices can potentially be achieved by high mobility channel materials such as III-V nFETs and Ge pFETs [3]. The thermal budget for device fabrication at the upper tiers is coupled with the thermal stability limitations of existing devices in the lower tiers. Competitive monolithic 3D integration is feasible within a maximum process temperature of 500 °C - 550 °C for the upper tier devices [4]. Pulsed laser annealing has the potential to activate dopants at temperatures as low as 500 °C [5]. Interconnect thermal stability is yet another challenge. State-of-the-art ultra-low-k dielectrics are suitable for T=500 °C processing [6]. It has also been demonstrated [7] that Cu lines can withstand temperatures up to 525 °C without degradation.

The process temperature budget of Ge pFET fabrication is inherently low compared to Si, making fully depleted Ge channel pFETs a potential candidate for top tier devices. High performance FD Ge pFETs require a thin monocrystalline Ge device layer with a low residual doping concentration which can be challenging using H implantation and Smart Cut [8] or using Ge grown on GaAs [9]. Moreover, GOI pFETs commonly suffer from the off-state leakage and positive threshold voltage which can be potentially attributed to the poor quality Ge/BOX interface [10] or p type residual doping [11]. In this work we demonstrate a low temperature (T=350 °C) GOI process based on Ge Strain Relaxed Buffer (SRB) growth and incorporating a $Si_{0.5}Ge_{0.5}$ etch stop layer to achieve thin Ge device layers. Long channel GOI pFETs are fabricated to validate the substrate quality. The devices demonstrate negative threshold voltage (V_T) of -0.18 V and 60% higher mobility compared to SOI pFET.

In this extended paper Raman spectra were obtained in order to determine the strain in the Ge layer. Additionally with further electrical characterization and analysis, the back interface quality of the Ge channel was investigated. A qualitative explanation of the back gate influence to the device behavior is presented.

II. EXPERIMENTS

The GOI fabrication process is schematically depicted in Fig. 1. 100 mm Si wafers were cleaned in a Piranha (H_2SO_4:H_2O_2 3:1) solution followed by a 5% HF dip. The wafers were immediately loaded in the epitaxial reactor and baked at 1050 °C for 90 s to remove the native
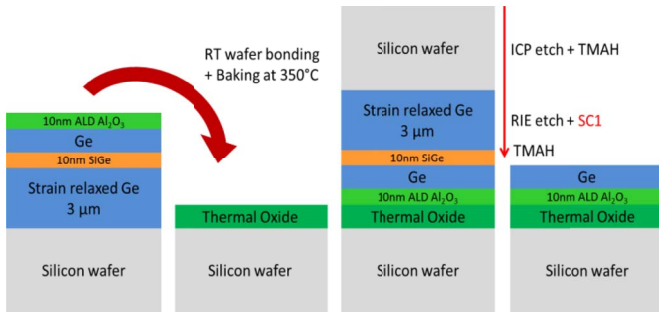
FIGURE 1. Low temperature GOI fabrication process flow through 3 steps: Al_2O_3/Ge(25 nm)/SiGe(10 nm)/Ge(3 μm) stack deposition on Si, room temperature wafer bonding and thermal annealing at 350 °C, removal of Si, Ge and SiGe layers by dry and wet etching.

FIGURE 2. Fabrication process flow for the GOI p-MOSFET and associated process temperatures.

oxide. The epitaxial growth was performed in reduced pressure chemical vapor deposition at 20 Torr using SiH_4/GeH_4 as Si and Ge precursors respectively. Three micrometer thick Ge SRB was grown on Si wafers using a two-step process (T_{Step1}= 400 °C, T_{Step2} = 600 °C) [12] followed by a 10 nm $Si_{0.5}Ge_{0.5}$ growth at 500 °C and a 25 nm Ge device layer grown at 400 °C, all in a single step epitaxy. A 10 nm Al_2O_3 layer was deposited by atomic layer deposition (ALD) at 200 °C and the wafer was bonded at room temperature to a thermally oxidized Si wafer and post annealed at 350 °C for 8 hours. Inductive coupled plasma (ICP) dry etch was used to thin down Si to about 100 μm, which was subsequently removed by TMAH (5%, T= 90 °C) solution with a selectivity >1000:1 towards Ge. The Ge SRB was etched with diluted standard clean 1 (SC-1) (NH_4OH:H_2O_2:H_2O 1:1:100) with a selectivity >400:1 towards $Si_{0.5}Ge_{0.5}$ which acts as an etch stop layer. Finally, the remaining $Si_{0.5}Ge_{0.5}$ etch stop layer is removed by TMAH (5%, T= 80 °C) with a selectivity >5:1 towards the Ge device layer.

Raman Spectra of the GOI layer were obtained using a μ-Raman Spectrometer equipped with a 532 nm Ar laser with initial power of 5 mW. The laser was focused to 1 μm spot using a 100x objective lens, and the power was sufficiently low to eliminate the heating effect. Tapping mode atomic force microscopy (AFM) and spectroscopic ellipsometry (SE) were used for evaluating the surface roughness and the thickness homogeneity of the GOI wafer respectively.

Ge pFETs were fabricated on the GOI wafers for electrical characterization of the transferred layer according to the process flow shown in Fig. 2. Active area was defined by etching the Ge layer down to the BOX. The gate dielectric stack was formed by thermal oxidation (O_2, T=550 °C) and ~5 nm ALD Al_2O_3 (4.3 nm EOT) followed by physical vapor deposition (PVD) of 12 nm TiN and low pressure chemical vapor deposition of 80 nm in-situ phosphorous doped poly-Si (T= 560 °C) as the gate electrode. A hard mask of 40 nm plasma enhanced chemical vapor deposition (PECVD) SiO_2 was used for gate patterning. The source/drain was implanted with BF_2 at 48 keV energy and

10^{15} cm^{-2} dose. Gate spacers were formed by 12 nm ALD SiO_2 followed by 50 nm PECVD SiN. Dopant activation was performed by rapid thermal anneal (RTA) at 600 °C for 1 min in N_2 ambient. An interlayer dielectric of 400 nm SiO_2 was deposited by PECVD and contact holes were etched with a combination of RIE (CHF_3/CF_4) and 1% HF dip. Finally, 100 nm PVD TiW and 500 nm PVD Al was used to form the device contacts.

Reference SOI devices (T_{Si} = 25 nm) were fabricated employing the same process as GOI devices with the following differences. Thermal SiO_2 (4.5 nm EOT) was used as gate dielectric. The source/drain was formed by BF_2 implantation (energy=9 keV, dose=10^{15} cm^{-2}) and activation by RTA in N_2 at 1000 °C for 10 s. After metallization, forming gas anneal was performed at 400 °C for 30 min.
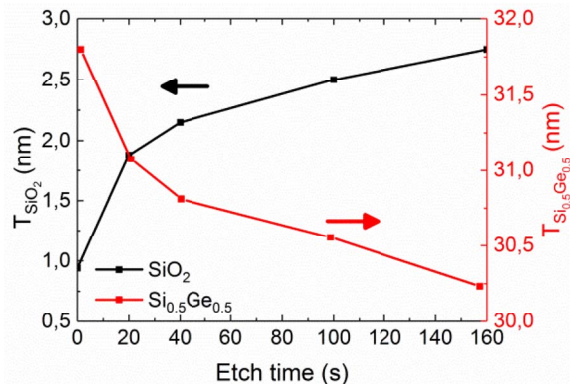

FIGURE 3. Removal of the $Si_{0.5}Ge_{0.5}$ etch stop layer and formation of SiO_2 during diluted SC-1 etch. Due to the presence of SiO_2 the $Si_{0.5}Ge_{0.5}$ etch rate becomes negligible thus achieving selectivity >400:1 towards Ge SRB.

III. RESULTS AND DISCUSSIONS

The etch stop mechanism of $Si_{0.5}Ge_{0.5}$ is depicted in Fig. 3. Initially both Si and Ge atoms are oxidized by SC-1 and the etch rate is ~3 nm/min. A SiO_2 film is formed on the surface which protects the layer from further oxidation, while Ge oxide is soluble in water and is removed from the surface. After removing 2 nm of the $Si_{0.5}Ge_{0.5}$ layer, the etch rate of $Si_{0.5}Ge_{0.5}$ drops significantly due to the formed SiO_2. This film protects the remaining $Si_{0.5}Ge_{0.5}$ and the underlying Ge
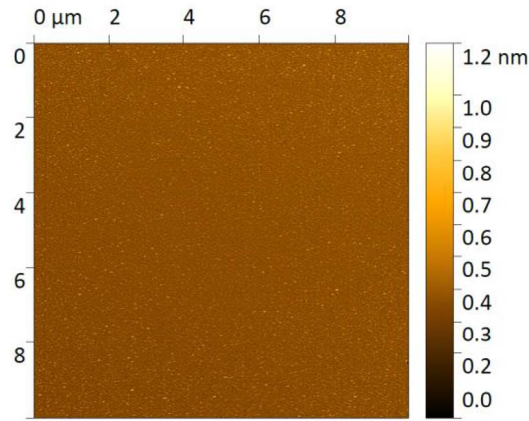
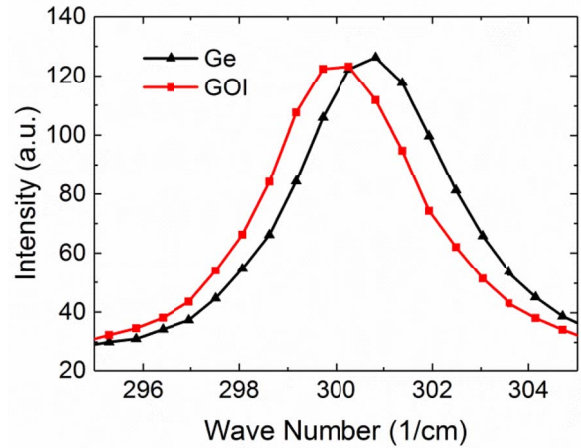**FIGURE 4.** AFM surface morphology of GOI substrate over 10 × 10 μm^2 area showing surface roughness below 0.5nm.
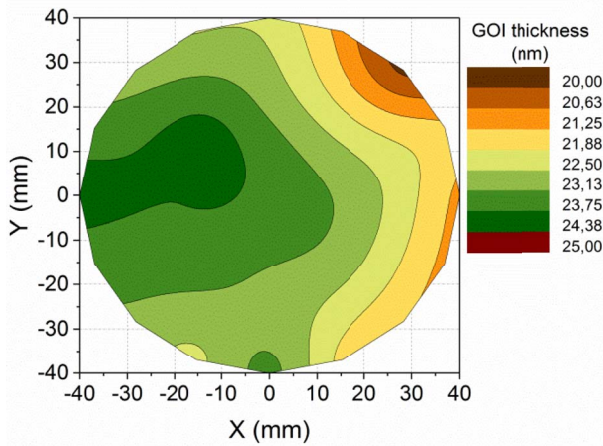
FIGURE 5. Thickness distribution of the top Ge layer in a fabricated 100mm GOI wafer. Only a small non uniformity was observed (T_{Ge} = 22.5±2.5 nm, 10 mm edge of the wafer is not measured).


FIGURE 6. Raman spectra of the GOI layer shows a shift compared to Ge which indicates 0.15% tensile strain in the active GOI layer.

as a result of the thermal expansion coefficient mismatch between Si and Ge.

The cross-section TEM images of a fabricated GOI pFET are shown in Fig. 7. The Ge active layer thickness is in accordance with the ellipsometry data shown in Fig. 5.

The source and drain (SD) regions are completely recrystallized through the post ion implantation annealing step. However, some twining defects stemming from the ion implantation are still present in the SD region.
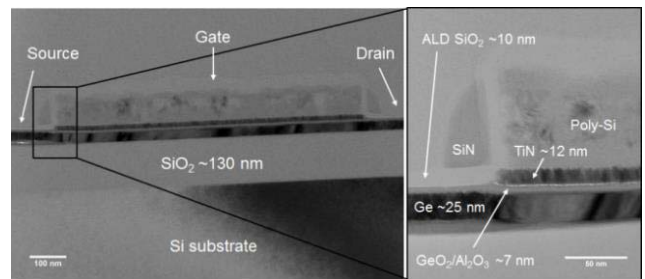
FIGURE 7. TEM image of 0.8 μm gate length GOI p-MOSFET and a close-up of the GeO$_2$/Al$_2$O$_3$/TiN/poly-Si gate indicating the thicknesses of the composing layers.

device layer from the SC-1 etchant. The surface roughness of the GOI wafer was below 0.5 nm as measured by AFM (Fig. 4). The Ge thickness over the wafer was measured by spectroscopic ellipsometry to be 22.5 nm ± 2.5 nm (Fig. 5).

The Ge thickness variation mainly comes from non-uniformity in the TMAH etch of the $Si_{0.5}Ge_{0.5}$ etch stop layer. This non-uniformity can be further reduced by employing single wafer spray etching tool instead of the wet etch bath used in this work. The sheet resistance of the 3.5 μm thick Ge SRB was 300 Ω/Υ indicating an unintentional p-type doping below 10^{16} cm^{-3} in accordance with the residual doping concentration commonly found in epitaxially grown Ge layers [13].

Fig. 6 shows the Raman spectra of both the unstrained Ge and GOI layers. The Ge-Ge peak for the unstrained Ge layer is at 300 cm^{-1} which is aligned with literature data. The small Raman shift for the GOI layer is attributed to 0.15% tensile strain in the layer. This strain is induced in the layer during the cool down step of the Ge SRB epitaxial growth,

Well-behaved I_D-V_G characteristics of a 0.8 μm gate length MOSFET are displayed in Fig. 8 showing the transistor turning on and off at both low and high V_D without back biasing. The GOI MOSFET also exhibits a sub-threshold slope (SS) of ~170 mV/dec that is similar to the results reported in literature (Table 1) as well as 60% higher long channel mobility compared to the reference SOI devices (Fig. 9). The influence of the back bias on the I_D-V_G characteristics, the threshold voltage V_T and the subthreshold slope SS is displayed in Fig. 10 and Fig. 11 respectively. For positive back bias (> 20V), the back interface is in accumulation, V_T does not depend on V_{BG} and SS is slightly degraded from the minimum value. The interface state density of the front gate is $D_{it-front} \approx 4.5 \cdot 10^{12}$ eV^{-1}cm^{-2}
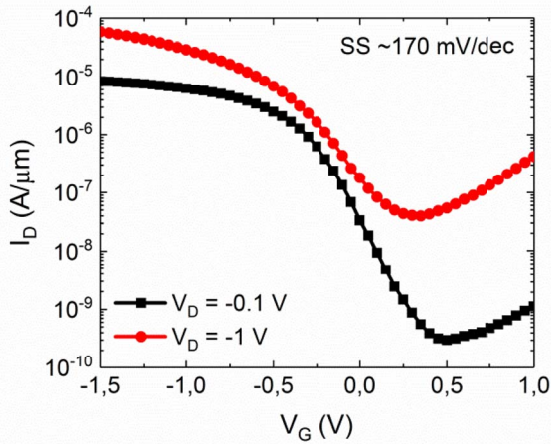
FIGURE 8. Well-behaved transfer characteristics of a p-channel 0.8 μm gate length device fabricated on the GOI. The SS was extracted at $V_D = -0.1$ V.

TABLE 1. Comparison of gate length, body thickness, EOT, subthreshold slope and long channel mobility of GOI MOSFETs.
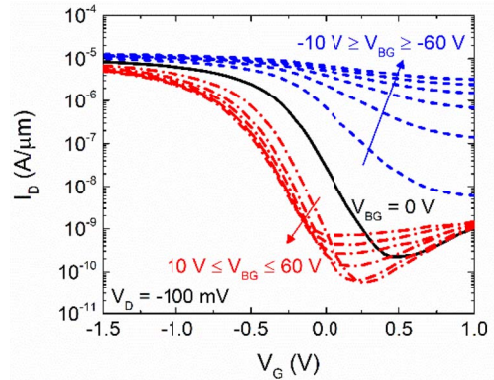
L_G (μm)	T_b (nm)	EOT (nm)	SS (mV/dec)	μ_h (cm^2/Vs)	Reference
0.8	25	4.3	170	170	This work
10	45	-	210	-	[10]
0.07-2.5	60–80	1.8	95-105	110	[11]
9	60	2.1	145	350	[13]
0.1	10	4.5	175	10	[16]
0.17	3	-	116	-	[17]
>100	2-25	-	>190	5-250	[18]
0.1-0.5	25-90	3	165-220	-	[19]
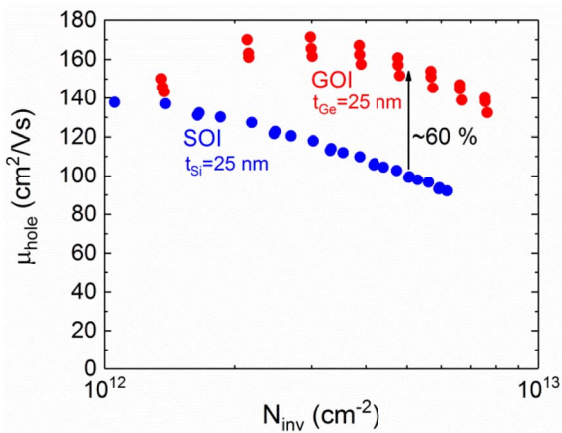
FIGURE 9. A mobility increase of 60% in GOI devices compared to the reference SOI devices is observed.

FIGURE 10. I_D-V_G characteristics of a p-channel 0.8 μm gate length device fabricated on the GOI with the back bias ranging from -60 V to 60 V.
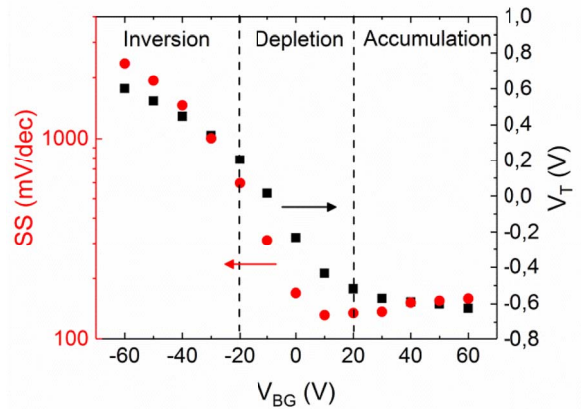
FIGURE 11. Front gate threshold voltage and subthreshold slope dependence of the back bias when the back interface is in inversion, depletion and accumulation.
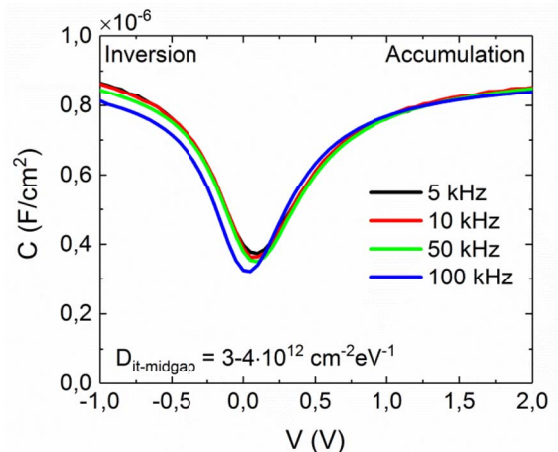
FIGURE 12. CV characteristics of Ge/Al$_2$O$_3$ MOS capacitors with D$_{it}$ of $3 - 4 \cdot 10^{12}$ eV^{-1}cm^{-2} which is in line with MOSFET data.

and was extracted from the SS. When a negative back gate voltage (V_{BG}) is applied, the Ge/BOX interface approaches inversion, the front gate control over the channel is gradually lost thus the subthreshold slope increases and the transistor does not turn off. When the back bias is small (< 20 V) the back interface is depleted, the front V_T depends linearly on the back bias and SS reaches the lowest value [14], [15].

The back interface of the devices is depleted at $V_{BG} = 0$ V confirming the low residual doping of the Ge channel as

well as that the number of fixed charges at the Ge/BOX is small. The interface state density of the Ge/BOX interface is $D_{it-back} \approx 1 - 2 \cdot 10^{12}$ eV^{-1}cm^{-2} and was obtained from the linear part of V_T vs. V_{BG} curve in Fig. 11. This value
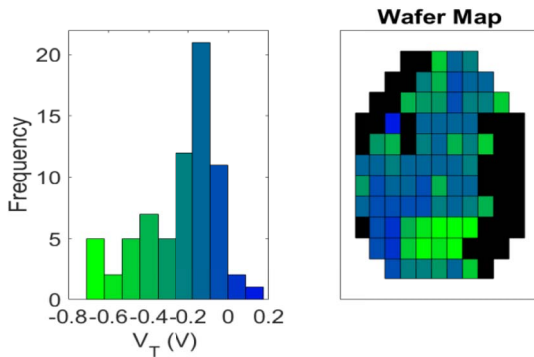
FIGURE 13. Measured V_T data over a wafer of fabricated p-channel GOI devices. The V_T median is -0.18 V. Devices that are either not working or out of the displayed V_T range are marked in black (in those areas, Ge was not perfectly bonded to the oxide and consequently was removed during the etch-back).

is in line with $D_{it-cap} \approx 3 - 4 \cdot 10^{12}$ eV^{-1}cm^{-2} that was extracted from the CV curves of Ge/Al$_2$O$_3$ MOS capacitors displayed in Fig. 12.

A wafer map demonstrating the V_T variation on the wafer is displayed in Fig. 13. The devices that are not working (do not turn on and off) or with V_T out of the presented range are marked in black. A 70% yield was achieved. The devices that failed are in the areas where Ge was not bonded properly and thus was removed during the etch-back process. The median of the V_T is -0.18 V whereas the reference SOI pFETs with TiN gate exhibit V_T of -0.65 V. TCAD simulations that assume no oxide charge and no fixed charge at neither front nor back interface, give a V_T shift of 0.47 V between SOI and GOI devices which is in line with our experimental data.

IV. CONCLUSION

A low temperature ($T_{max} = 350$ °C) GOI process based on Ge SRB growth and a Si$_{0.5}$Ge$_{0.5}$ etch stop layer was demonstrated. Employing a highly selective diluted SC-1 etchant for Ge removal allows a 10 nm Si$_{0.5}$Ge$_{0.5}$ layer to be used as an etch stop. Using this technique, GOI substrates were fabricated with Ge thickness of 22.5 ± 2.5 nm, surface roughness below 0.5 nm and 0.15% tensile strain. The residual p-type dopant concentration was estimated to be below 10^{16} cm^{-3}. Ge pFETs were fabricated ($T_{max} = 600$ °C) on the GOI wafers with 70% yield and the devices exhibited a V_T of -0.18 V and 60% higher mobility compared to the SOI pFET reference.

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AHMAD ABEDIN received the B.Sc. degree in materials and engineering from the Sharif University of Technology, Tehran, Iran, and the M.Sc. degree in nanotechnology from the KTH Royal Institute of Technology, Sweden, in 2013, where he is currently pursuing the Ph.D. degree. He is currently conducting research on group IV semiconductors epitaxial growth and device fabrication.

LAURA ZURAUSKAITE received the B.Sc. degree (*cum laude*) in physics from Vilnius University, Vilnius, Lithuania, in 2014 and the M.Sc. degree in nanotechnology from the KTH Royal Institute of Technology, Stockholm, Sweden, in 2016, where she is currently pursuing the Doctoral degree. She is currently engaged in research of Ge/high-k MOS interfaces and Ge MOSFETs based on them.

A. ASADOLLAHI photograph and biography not available at the time of publication.
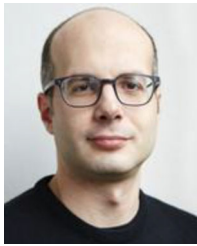
KONSTANTINOS GARIDIS is currently pursuing the Ph.D. degree in nano- and micro-electronics with the Department of Electronics, KTH Royal Institute of Technology, Stockholm, Sweden. His research interests include the design and fabrication of Si and Ge MOSFETs, monolithic 3-D integration and Si1-xGex epitaxy.

GANESH JAYAKUMAR received the M.Sc. degree in electronics design from the University of Glasgow, U.K., in 2011. He is currently pursuing the Ph.D. degree with the Department of Integrated Devices and Circuits, School of EECS, KTH Royal Institute of Technology and with the thesis entitled "Monolithic integration of silicon nanowires with CMOS circuits for biosensing application." His research interests include lab-on-chip sensors for biomedical applications and semiconductor device technology.

B. GUNNAR MALM (M'98–SM'10) was born in Stockholm, Sweden, in 1972. He received the M.S. degree from Uppsala University, Sweden, in 1997 and the Ph.D. degree in solid-state electronics from the Royal Institute of Technology, Stockholm, in 2002, where he has been an Associate Professor with the School of ICT since 2011. His recent work includes silicon carbide technology for extreme environments and spintronics for microwave and logic applications.

PER-ERIK (HELLBERG) HELLSTRÖM received the M.Sc. and Ph.D. degrees in electrical engineering from the KTH Royal Institute of Technology, Stockholm, Sweden, in 1995 and 2000, respectively. His Ph.D. thesis dealt with polycrystalline $Si_{1-x}Ge_x$ as gate material for CMOS technology. Since 2000, he has been a Research Associate with the KTH School of Electrical Engineering and Computer Science and, in 2006, he was appointed as a Docent. He has co-authored over 100 papers in refereed journals and conference proceedings. His current research interests include semiconductor process technology, advanced nano-scaled MOSFETs, and monolithic 3-D integration technology and devices for sensing applications.

MIKAEL ÖSTLING (M'85–SM'97–F'04) received the M.Sc. and Ph.D. degrees from Uppsala University, Sweden. He is currently a Professor of solid-state electronics and a Deputy President with the KTH Royal Institute of Technology, Sweden. His research interests are Si/SiGe devices and process technology for very high frequency, and also device technology for wide bandgap semiconductors with special emphasis on SiC for high power and high temperature applications. Since 2016, he has been the Editor-in-Chief of the IEEE JOURNAL OF THE ELECTRON DEVICES SOCIETY.